A µProcessor Layer for mm-Scale Die-Stacked Sensing Platforms Featuring Ultra-Low Power Sleep Mode at 125˚C

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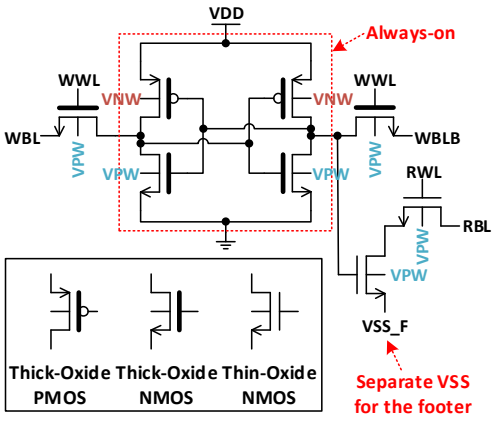
***Abstract*—This paper presents an ultra-low power sleep mode µprocessor layer designed for use in mm-scale die-stacked wireless sensing platforms for high temperature applications. A compact DC-DC converter is incorporated with a 16kB custom SRAM for self-sufficient memory data retention, enabling a platform-level deep sleep mode. The proposed system is fabricated in a USJC 55nm deeply depleted channel (DDC) technology that is deliberately shifted to the slow corner, allowing the complete sensing platform to retain full memory contents with 0.54µW during sleep mode at 125˚C, which is 26× lower than without the proposed techniques.**

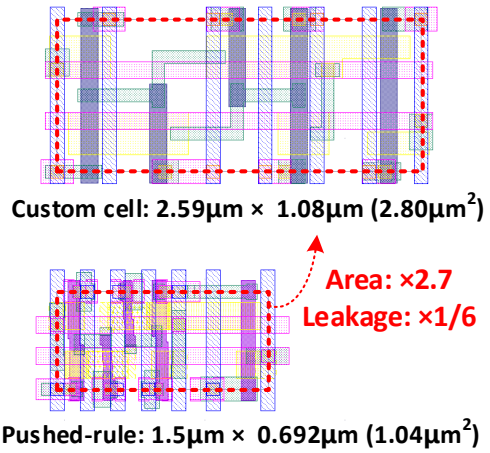
Keywords—low power, sleep mode, µprocessor, mm-scale, wireless sensor, high temperature

I. INTRODUCTION

Miniaturized wireless sensor nodes are inherently energy constrained due to their small form factor batteries, and thus must be designed with ultra-low power consumption to ensure sufficient lifetime [1]-[2]. Recently, mm-scale wireless sensor nodes have become viable for emerging applications that experience high temperatures, such as down-hole sensors for shale oil mining; these devices log temperature and pressure during hydraulic fracturing [3]. High temperatures significantly deteriorate sensor lifetime, largely due to exponential leakage increases. Therefore, it is necessary to improve the energy efficiency of such sensors at high temperature. Leveraging the intermittent data processing in most sensing applications, duty cycling via power gating is typically used to reduce overall energy consumption. In this case, the always-on components, such as program and data memories, will dominate total energy. While embedded non-volatile memories are appealing for their near zero-power retention, they have high write energy and often have low endurance at high temperature such as 125˚C, introducing memory refresh overhead. In the proposed system, therefore, we deploy an always-on custom SRAM that is deliberately shifted to the slow corner by the foundry to minimize memory leakage while maintaining bitcell size. An integrated compact DC-DC converter and negative body-bias charge pump in the SRAM enables the primary power management unit (PMU) for the entire sensor node to be shut down during sleep mode, significantly reducing overall leakage at high temperature.



(a)



(b)

Fig. 1 8T SRAM bitcell: (a) schematic and (b) its layout

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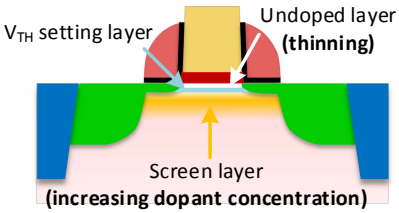


Fig. 2 An adjusted fabrication process in a DDC transistor for leakage reduction [4]

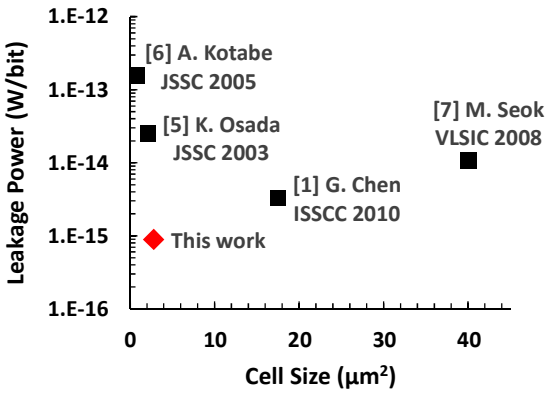


Fig. 3 SRAM bitcell leakage comparison scatter plot with the previous work at 25˚C (measurement)

II. Low-Leakage SRAM

Fig. 1 shows the schematic and layout of the 8T SRAM bit cell deployed in the proposed system. Since the target application has 0.6V and 1.2V supply voltages, the SRAM operates at 0.6V. The cross-coupled inverters that hold data are designed with thick-gate-oxide transistors as the sub-fW leakage targets are infeasible using thin oxide devices due to both their higher subthreshold and gate leakages. On the fabrication side, the wafer is shifted to the slow corner for about 4× leakage reduction by thinning the undoped layer and increasing the dopant concentration of the screen layer in the DDC transistor [4] as described in Fig. 2. The layout is drawn using logic rules rather than pushed rules, sacrificing 2.7× area for 6× lower leakage. The measured SRAM cell leakage is 0.89fW/bit and 1.4pW/bit at 25˚C and 125˚C, respectively. To our knowledge, this represents the first sub-fW SRAM bit cell as shown in Fig. 3. The cell area is also competitive when accounting for the fact that thick-gate-oxide transistors do not scale as well as thin-gate-oxide transistors in advanced technologies.

At high temperature, parasitic BJT leakage shown in Fig. 4 can be triggered by small voltage differences between source/drain and p/n-well bias caused by IR drop. Previous test chips showed that this parasitic BJT leakage current can be significant (~1μA). To avoid this potential leakage, the system

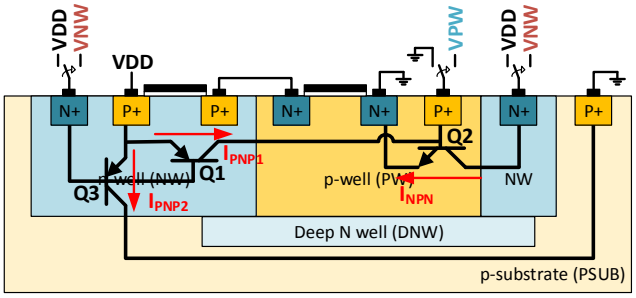


Fig. 4 Body biasing for the SRAM cell array to reduce the leakage through the parasitic BJTs

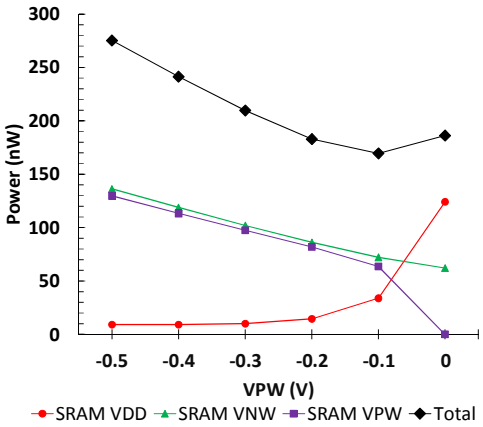
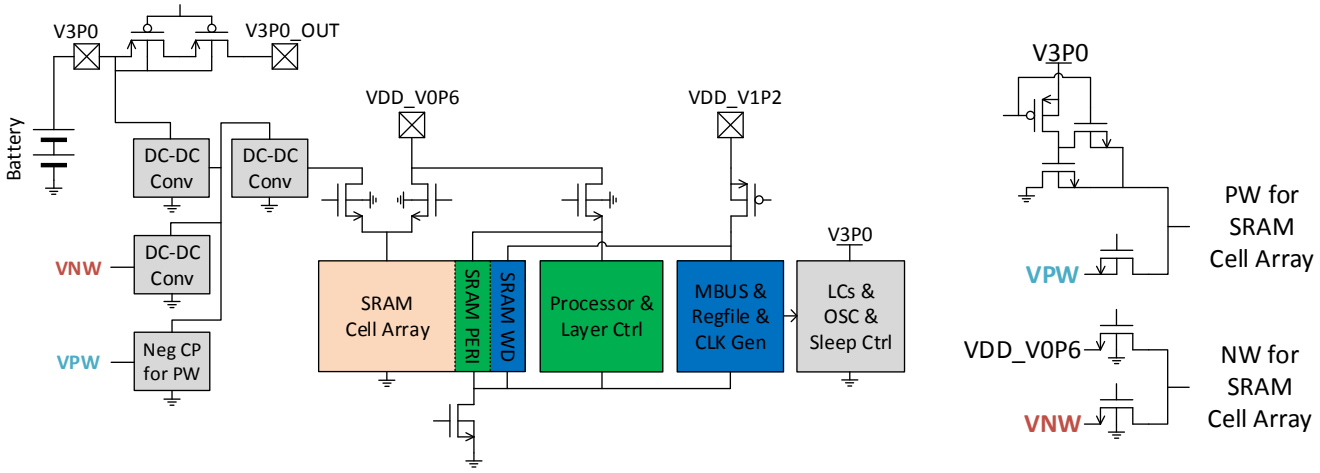


Fig. 5 SRAM leakage power measurement from each node with reverse body biasing at 125˚C (measurement)

generates a negative p-well body bias (VPW) and an n-well body bias (VNW) higher than VDD during the sleep mode. These biases are applied to the SRAM array to ensure the emitter-base junctions remain reverse biased at all times. In addition, according to the measurement results shown in Fig. 5, this reverse body biasing further reduces SRAM sub-threshold leakage, canceling the power overheads of generating the bias voltages. The leakage power from SRAM VPW node in Fig. 5 includes overhead of negative voltage generation. Word-line drivers are boosted using 1.2V supply to compensate for slow transistors. The two thin-gate-oxide read transistors are power-gated by a header and footer and act to accelerate read speed by 30×. Note that a footer is necessary to eliminate junction leakage from p-well to NMOS grounded source in the read transistors, which reduces −0.1V VPW generation power by 39% according to the simulation results.

III. Proposed System

As a master layer for the mm-scale die-stacked sensing platform depicted in Fig. 7, the proposed system in Fig. 6 includes a Cortex-M0 processor with a custom SRAM, a sleep controller, a power gate for the battery, a negative charge-pump, and DC-DC converters. Since the complete stacked system is encapsulated by a metal or epoxy package after die-



(a) (b)

Fig. 6 (a) Overall block diagram of the proposed system, (b) Switches for SRAM cell array body biasing

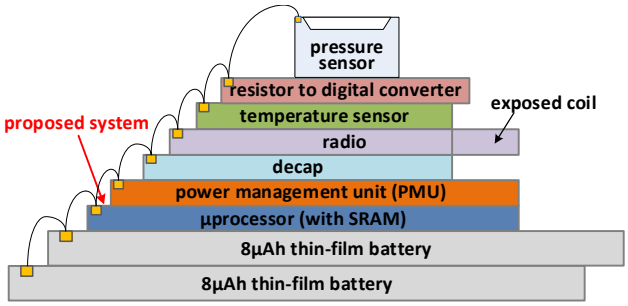


Fig. 7 mm-scale die-stacked wireless sensing platform with the proposed µprocessor layer

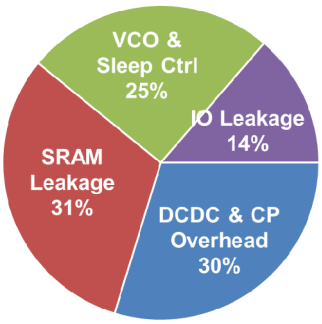


Fig. 8 Sleep power breakdown at 125˚C (measurement)

stacking, each layer has an intentionally reduced ESD circuit since it only needs to protect for stress during wire-bonding. At 125˚C, even small ESD power clamps and IO cells leak significantly (>80nW per each layer). Therefore, the proposed system completely cuts off battery power for all the other layers during the sensor's sleep mode. Consequently, 0.6V and 1.2V layer power from the PMU is not available during the sleep mode. Hence, the proposed system internally generates power for SRAM data retention with a dedicated DC-DC converters which consists of 2:1 switched-capacitor converters with a regulation loop and a negative charge pump. All power gate switches depicted in Fig. 6 are controlled by the sleep controller. The power gates for 0.6V domain are designed with NMOS transistors because the gate control signal comes from the sleep controller powered by the battery (>2.2V). Since the sleep controller is always-on, it is designed with the least leaky IO devices trading off area for power. The sleep controller also controls the reset signals for other blocks. To prevent a current path from the p-well to ground when VPW is at negative voltage, a three-transistor switch is used as depicted in Fig. 6 (b) [8].

Technology	55nm DDC process
Die Size	2600µm x 1080µm
CPU	ARM Cortex M0
On-chip Memory	16KB SRAM
SRAM Bitcell Leakage Power	**0.89fW @ 25°C** **1.4pW @ 125°C**
Supply Voltage	Nominal: From PMU layer: 1.2V, 0.6V Sleep Mode: From Battery: 2.2V~3.3V (SRAM power is internally generated)
Frequency	Processor: 200kHz DC-DC and CP: 1kHz ~ 100kHz
Sleep Power	**0.54µW @ 125°C**

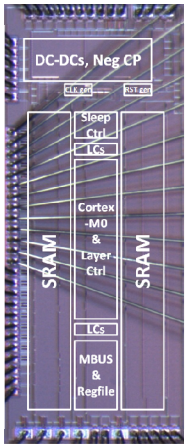


Fig. 9 Die photo and chip summary

The pie chart in Fig. 8 shows the sleep power breakdown at 125˚C; DC-DC converters and a charge-pump supplies the SRAM at around 50% efficiency. As an example of use-case, a program alternates the system between sleep and active mode.

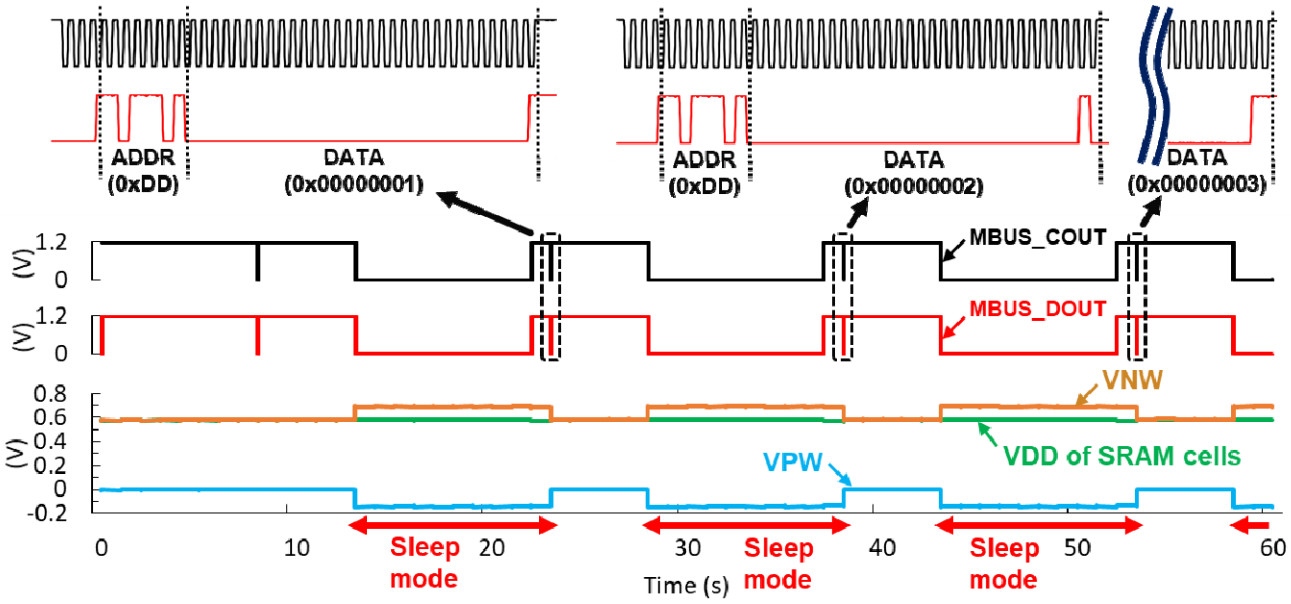


Fig. 10 Measured waveform for monitoring mode change (Wake-up→Sleep→Wake-up→…) at 125˚C; The µprocessor sends a message on Mbus after waking up with the data saved before going to sleep mode, which is an example of use-case of the proposed system (measurement)

Once the processor wakes up from the sleep mode, a variable assigned to the memory initialized during the program loading is increased by 1 and its value is sent out through Mbus [9] to demonstrate correct data retention, as shown in Fig. 10. Fig. 9 shows a die photo and chip summary. The total sleep power of the proposed system is 0.54µW at 125˚C which is 5× better than previously implemented M^{3}HT system [3] while increasing SRAM by 5.3×, marking 26× better sleep power per SRAM bit. Since the sleep controller shuts-off all other layers in the system, it produces a constant standby power, regardless of the number of layers in the system making it applicable to simple and complex systems alike.

IV. Conclusion

Sleep power is critical for the lifetime of sensors with power gates and sleep modes, particularly for high temperature applications where leakage currents dominate. This paper presented a µprocessor system that features ultra-low power sleep mode at high temperature. The proposed system incorporates a 16kB custom SRAM, an internal DC-DC converter and charge-pumps that allow the complete sensing platform to retain full memory contents with 0.54µW during sleep mode at 125˚C, which is 26× lower than without the proposed techniques.

References

[1] G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M. Chen, Z. Foo, D. Sylvester, and D. Blaauw, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2010, pp. 288–289.

[2] S. Oh, Y. Shi, G. Kim, Y. Kim, T. Kang, S. Jeong, D. Sylvester, and D. Blaauw, "A 2.5nJ duty-cycled bridge-to-digital converter integrated in a 13mm^2 pressure-sensing system," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2018, pp. 328–329.

[3] M. Choi, Y. Sui, I. Lee, R. Meredith, Y. Ma, G. Kim, D. Blaauw, Y. Gianchandani, and T. Li, "Autonomous Microsystems for Downhole Applications: Design Challenges, Current State, and Initial Test Results," *Sensors*, vol. 17, no. 10, p.2190, 2017.

[4] D. Kidd, "Process and circuit optimization for power reduction using DDC transistors," *IEEE Micro*, vol. 34, no. 2, pp. 54–62, Mar./Apr. 2014.

[5] K. Osada, Y. Saitoh, E. Ibe, and K. Ishibashi, "16.7-fA/cell tunnel-leakage-suppressed 16-Mb SRAM for handling cosmic-ray-induced multierrors," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1952–1957, Nov. 2003.

[6] A. Kotabe, K. Osada, N. Kitai, M. Fujioka, S. Kamohara, M. Moniwa, S. Morita, and Y. Saitoh, "A low-power four-transistor SRAM cell with a stacked vertical poly-silicon PMOS and a dual-word-voltage scheme," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 870–876, Apr. 2005.

[7] M. Seok, S. Hanson, Y.-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, "The Phoenix processor: A 30 pW platform for sensor applications," in *IEEE Symp. VLSI Circuits (VLISC) Dig.*, 2008, pp. 188–189.

[8] J. Lee, Y. Zhang, Q. Dong, W. Lim, M. Saligane, Y. Kim, S. Jeong, J. Lim, M. Yasuda, S. Miyoshi, M. Kawaminami, D. Blaauw, and D. Sylvester, "A self-tuning IoT processor using leakage-ratio measurement for energy-optimal operation," *IEEE J. Solid-State Circuits*, vol. 55, no. 1, pp.87–97, Jan. 2020.

[9] P. Pannuto, Y. Lee, Y.-S Kuo, Z. Foo, B. Kempke, G. Kim, R. Dreslinski, D. Blaauw, and P. Dutta, "MBus: an ultra-low power interconnect bus for next generation nanopower systems," in *Proc. Int. Symp. Computer Architecture (ISCA)*, 2015, pp.629–641.