

CURRICULUM VITAE

David T. Blaauw

May 2022

I Personal Data

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II Employment History

A. Education

Doctor of Philosophy in Computer Science, University of Illinois, Urbana-Champaign, January 1992.
Thesis: "Functional Abstraction in Switch-Level Simulation."
Advisor: Professor Jacob A. Abraham

Master of Science in Computer Science, University of Illinois, Urbana-Champaign, May 1989.
Thesis: "Automatic Generation of Behavioral Models."
Advisor: Professor Jacob A. Abraham

Bachelor of Science in Physics with a second major in Computer Science, Duke University, May 1986.

B. Present Position

Professor of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.

C. Employment History

- September 2007 - Present: Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan
- August 2001 - September 2007: Associate Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan.
- September 1994 - August 2001: Engineering Manager, Advanced Design Technology, Motorola, Inc., Austin, Texas.
- August 1993 - September 1994: Staff engineer, Semiconductor Systems Design Technology Group, Motorola, Inc., Austin, Texas.
- August 1992 - August 1993: Development Staff Member, IBM Corporation, Endicott, New York.

D. Honors and Awards

- Best Paper Award, Andrea Bejarano-Carbo, Hyochan An, Kyojin Choo, Shiyu Liu, Dennis Sylvester, David Blaauw, Hun Seok Kim, “Millimeter-Scale Ultra-Low-Power Imaging System for Intelligent Edge Monitoring,” TinyML conference, March 2022
- Highlighted paper in Nature Electronics: “Actuating sub-millimetre robots” in Proc. 2022 IEEE Int. Solid-State Circuits Conference, March 2022
- MobiCom 2021 Best Paper award “mSAIL: milligram-scale multi-modal sensor platform for monarch butterfly migration tracking”. Also selected to be highlighted for the combined edition of Fall 2021/Spring 2022 SIGMOBILE Research Highlights
- 2022 Distinguished Academic Achievement Alumni Award from the Department of Computer Science at the University of Illinois at Urbana-Champaign. One award given per year.
- 2022 IEEE Micro Top Picks Special Issue on Top Picks from the 2021 Computer Architecture Conferences, Honorable Mention, “SquiggleFilter: An Accelerator for Portable Virus Detection”
- Test of Time award, “the highest honor an academic paper receives for its impact and recognizes an influential MICRO paper whose influence is still felt 18-22 years after its initial publication” for “Razor: A low-power pipeline based on circuit-level timing speculation,” IEEE/ACM International Symposium on Microarchitecture, 2003, October, 2021
- Winner, 2019 Monarch Butterfly Fund for creating a system to track the flight of individual monarch butterflies on their migration to Mexico
- 2019 Distinguished University Innovator Award given to one team in the university for developing and marketing transformative ideas and technologies
- Named the Kensall D. Wise Collegiate Professor of Electrical Engineering and Computer Science, 2019
- Best Student Paper Award, “A 4×4×4-mm³ Fully Integrated Sensor-to-Sensor Radio using Carrier Frequency Interlocking IF Receiver with -94 dBm Sensitivity,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2019
- 2019 IEEE Micro Top Picks special issue on the Computer Architecture Conferences, “Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks”
- 15 year retrospective most influential paper in ISCA 2002 award for groundbreaking research in power-efficient computing, ACM/IEEE International Conference on Computer Architecture (ISCA), 2017

- Member of University of Illinois Engineering Advisory Panel. 2015 through current.
- Ranked as the top publishing author at IEEE VLSI Circuits Symposium over the last 30 years of the conference with 38 publications. June 2017
- 2016 University Researcher Award, Semiconductor Industry Association (SIA) – Semiconductor Research Corporation (SRC), established by the semiconductor industry association to recognize lifetime research contributions to the U.S. semiconductor industry by university faculty. One award given per year for circuits and technology each.
- 2016 IEEE Micro Top Picks special issue "MBus: The Missing Interconnect that Enables the Modular Millimeter-Scale Computing Class and Connects the World's Smallest Computer,"
- Best Paper Award, "Race-track Converter: A Low Power and Compact Data Converter Using Race-track Spintronic Devices," IEEE International Symposium on Circuits and Systems (ISCAS), May 2015
- 2014 John von Neumann Student Research Award for Excellence in Systems Research – SONIC Annual Review Meeting
- Recognized as top 50 innovator over the last 50 years graduating from the University of Illinois EECS department in 2014
- College of Engineering Innovation Excellence Award for 2013-2014
- Design Automation Conference (DAC) 50th Anniversary award for being the top 10 most cited DAC authors in DAC's 50 year history, June 2013
- Design Automation Conference (DAC) 50th Anniversary award for publishing the most papers in the fifth decade of DAC's history, June 2013
- 2013 University of Michigan Electrical Engineering and Computer Science (EECS) Department Outstanding Achievement Award for innovative research in variation-tolerant and energy efficient integrated circuit design, and exceptional mentoring and teaching in the area of VLSI circuits
- International Solid-State Circuits Conference (ISSCC) 60th Anniversary Special Recognition top 10 contributing author over the last 10 years, February 2013
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award, "Combined Dynamic Voltage Scaling and Adaptive Body biasing for Lower Power Microprocessors under Dynamic Workloads," ICCAD 2002 Conference, November 2012
- Second Prize in the 18th Samsung Human-Tech Thesis Competition for research on millimeter sensor design, February 2012
- IEEE Fellow status, January 2012
- Winner MuSyC Research Consortium annual best poster award, "A Modular 1mm³ Die-Stacked Sensing Platform," Nov 2011
- Winner 11th International VLSI-Symposium Low Power Design Contest, "SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
- Winner Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Design contest, "Design and Implementation of Centip3De, a 7-layer Many-Core System," Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC), Feb/June 2011

- Best Paper Award, “Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs),” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009
- 2008 Ted Kennedy Family Team Excellence Award (award shared with Todd Austin, Scott Mahlke, Trevor Mudge, Marios Papaefthymiou). The Ted Kennedy Family Team Excellence Award is an annual award given by the University of Michigan, College of Engineering that recognizes the production of an extraordinary and significant piece of work from current or recent collaboration in teaching or research to the College of Engineering.
- 2008 Richard Newton GSRC Industrial Impact Award for “development of the Razor technology” (award shared with Professor Todd Austin). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is “at least five years old and has had a significant industrial impact.”
- University of Michigan College of Engineering Research Excellence Award for 2007-2008, January 2008
- Best Paper Nomination, “Energy Efficient Near-threshold Chip Multi-processing,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
- Best Paper Nomination, “Self-timed Regenerators for High-speed and Low-power Interconnect,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
- Microprocessor Review Analysts’ Choice Award in Innovation for “Introducing Speculation on Correctness as a Method for Allowing Circuit Operation Beyond Worst-Case Design,” Microprocessor Review, February 2007
- 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, “Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation”
- University of Michigan Henry Russel Award for “Exceptional Scholarship and Conspicuous Ability as a Teacher,” November 2004
- Best Paper Nomination, “Parametric Yield Estimation Considering Leakage Variability,” ACM/IEEE Design Automation Conference (DAC), June 2004
- Best Paper Award, “Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation,” ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2003
- Best Regular Paper Award, “Noise Analysis Methodology for Partially Depleted SOI Circuits,” IEEE Custom Integrated Circuits Conference (CICC), September 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2003
- Best Paper Award, “Statistical Delay Computation Considering Spatial Correlations,” ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2002
- Best Paper Nomination, “Pre-route Noise Estimation in Deep Submicron Integrated Circuits,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2002
- Best Paper Nomination, “Driver Modeling and Alignment for Worst-Case Delay Noise,” ACM/IEEE Design Automation Conference (DAC), June 2001
- Best Paper Award, “On-Chip Inductance Modeling and Analysis,” ACM/IEEE Design Automation Conference (DAC), June 2000
- Motorola Innovation Award, 1997
- Motorola High Impact Technology Award, 1996

III Research Experience

A. Research Interests

My research interests focus on high-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit design techniques for effective VLSI design in the nano-meter era, in conjunction with efficient and accurate analysis and optimization methods for large, multi-million transistor designs.

B. Doctoral Students Supervised

<u>Student</u>	<u>Thesis Title/Topic</u>	<u>Graduation Date</u>
Alhad Daftardar	High Performance Computing	In Progress
Jungho Lee	Neural Stimulation Inprogress	In Progress
Kuan Yu Chen	Low Power Signal Processing Through Reconfigurable Systolic Arrays	In Progress
Andrea Bejarano	mm-Scale Image Sensing Through Low Power Circuit and Algorithm Co-Design	In Progress
Chien-Wei Tseng	Ultra-Low Power RF-Localization for Asset Management	In Progress
Yichen Gu	Computational Genomics for RNA Velocity Modeling	In Progress
Rohit Rothe	Ultra-Low Power Audio Amplification Through Switch Capacitor T-Ohm Resistance Circuits	In Progress
Zhen Feng	mm-Scale RF Communications	In Progress
Jihwan Seol	PLL Design Through Over Sampling Techniques	In Progress
Zhehong Wang	Application of New Technologies to Neural Networks Processors	December 2021
Xiao Wu	Energy Efficient Circuits and System for Internet of Things and Hardware Accelerator Design for Genome Sequencing	July 2019

Li-Xuan Chuo	Miniaturized Low-Power and Energy-Efficient RF Wireless Communication and Sensing Systems	June 2019
Ziyun Li	Energy-Efficient Mobile Computer Vision and Machine Learning Processors	May 2019
Kyojin Choo	Charge-domain analog/mixed-signal circuits and applications	Sept 2018
Yao Shi	Millimeter-Scale and Energy-Efficient RF Wireless System	Aug 2018
Wootae Lim	Ultra-low Power Circuit Design for Miniaturized IoT Platform	May 2018
Taekwang Jang	Circuit and System Designs for Millimeter Scale IoT and Wireless Neural Recording	Dec 2017
Wanyeong Jung	Low-Power Energy Efficient Circuit Techniques for Small IoT Systems	April 2017
Supreet Jeloka	Cross-point Circuits for Computation, Interconnects, Security and Storage	Jan 2017
Yejoong Kim	Robust Circuit Design for Low-Voltage VLSI	May 2015
Nathaniel Pinckney	Near-Threshold design	July 2015
Dongmin Yoon	Low power timer references	Jan 2015
Inhee Lee	Power management for ultra-low power sensors systems	Oct 2014
Gyouho Kim	Ultra-low power visual monitoring	Aug 2014
Bharan Giridhar	Adaptive Computing	Dec 2013
Zhi Yoong Foo	Low power processor design techniques	Aug 2013
Sudhir Satpathy	Fast and low power interconnect fabrics	Dec 2012
David Fick	Adaptive Low-power design	Aug 2012
Yoonmyung Lee	Ultra Low-Power Memory Design	April 2012

Prashant Singh	Reliability analysis and wear-out detection	April 2010
Nurrachman Liu	Automatic tuning of VLSI circuits	April 2010
Brian Cline	Process variation modeling for advance semiconductor circuits	Feb 2010
Cheng Zhuo	VLSI wearout modeling	Dec 2010
Ravikishore Gandikota	Crosstalk-Noise analysis for nanometer VLSI circuits	Aug 2009
Carlos Tokunaga	Circuits and architectures for secure processing	Sep 2008
Shidhartha Das	Razor: circuit speculation for power and performance efficient design	Oct 2008
Kaviraj Chopra	Statistical timing analysis including spatial correlations	Apr 2008
Eric Karl	Reliable computing on unpredictable silicon	Mar 2008
Sanjay Pant	Power grid analysis and design	Dec 2007
Mini Nanua	Leakage and noise analysis in nano-scale technologies	Apr 2007
Bo Zhai	Dynamic voltage scaling for embedded processor designs	Mar 2007
Rajeev Rao	Modeling and design of low-power VLSI systems under for multiple sources of uncertainty	Jul 2006
Dongwoo Lee	Analysis and minimization of leakage current	May 2005
Aseem Agarwal	Statistical timing analysis for VLSI circuits	Mar 2005

C. Masters Students Supervised

<u>Student</u>	<u>Thesis Title/Topic</u>	<u>Graduation Date</u>
Peijun Hou	Capacitance to Digital Conversion	In Progress
Li Yu Chen	High Voltage Upconversion	May 2021
Hengfei Zhong	Power Circuit Design	May 2020
Ashwin Bhat	Error Tolerant Long-Read Alignment for Genomic Sequencing	April 2020
Hyungjoo Seo	Low Power Energy Harvesting	May 2019
Tim Wesley	Low Power Neural Network Accelerators	May 2019
Yu Zeng	Low Power Crystal Oscillator Circuits	Dec 2017
Dongkwun Kim	Low Power Voltage References	May 2017
Skyler Skrzyniarz	Low Power Correlation Architectures for GPS	June 2015
Junhua Gu	Low Power Circuits for Analog to digital interfaces	May 2015
Ruochen Xie	Energy Reduction of FeRAM Memories for Millimeter Sensors	May 2015
Allen Wang	Low Power Level Conversion	May 2014
Naveen Akesh	Low Power Audio Device for Developing World	May 2014
Zhe Yu	RF Communication for Millimeter Scale Sensors	May 2014
Hsi-Shou Wu	Low Power Word-Spotting	April 2014

Siddharth Saxena	Low power correlation circuits	May 2013
Karan Jain	Low power synchronization using ambient RF signals	April 2012
Jordan LeNoach	pH sensor for millimeter sensors	Dec 2011
Jeffrey Yeh	Chip design for the developing world	April 2011
Nate Robert	Low power LDO	Dec 2010
Vikas Vinay	Low power Class-D amplifier for developing world applications	Dec 2010
Abhishek Madhavan	Low power chip design	Dec 2010
Junsun Park	Intra-cellular chip design	May 2010
Jou-ching (George) Sung	Low power ADC design	Aug 2009
Mao-Ter Chen	Low power sensor node design	Dec 2008
Sudharsen Kalaiselvan	Razor-3: A circuit speculation and SEU tolerant circuit technique	May 2007
Deepesh John	Low power design through typical-case optimization	May 2006
Yueh-Chuan Tzeng	Encryption processor for side channel attack avoidance	May 2006
Meghna Singhal	Low power design using subthreshold operation	May 2006
Amir Borna	Analysis of lithographic variations for chip performance	Aug 2005
Amit Jain	Delay modeling for non-ramp input transitions	Nov 2004
Toan Pham	Clock skew reduction using Razor flip-flops	Dec 2003
Bhavana Thudi	Non-iterative switching window computation for delay noise	May 2003

Wesley Kwong	Efficient circuit-level analysis of gate-oxide tunneling current in VLSI designs	May 2003
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D. Research Grants

- National Science Foundation (NSF), “StiMote: An Ultrasmall, Modular Neurophotonic Stimulator,” PI: James Weiland, \$ 649,130, with \$216,376 to Blaauw, 06/24/2021 – 6/23/2023
- Ministry of Defense, “Low Power Localization,” PI: David Blaauw, \$840,000, with \$420,000 to Blaauw, 3/12/2020 - 3/31/2022
- Intel Corporation, “Valleytronics Circuit Design for Efficient Realization of Computational Logic,” \$555,000 to Blaauw, PI: Blaauw, 6/31/2020-6/30/23
- DARPA “Datalink Applications of DSSoC-DASH (KESTREL),” \$720,000 with \$360,000 to Blaauw, PI: Hun Seok Kim, 1/1/2020-1/17/2023
- Semiconductor Research Corporation (SRC), “Analog and Digital Assist Techniques to Improve Mixed-Signal,” \$130,000 with \$65,000 to Blaauw, PI: Dennis Sylvester, 9/1/2020 - 12/31/2021
- Facebook, “Context-Aware Multi-Sensor Fusion System and SoC Integrated Circuits and Digital Signal Processing,” \$239,752, with \$119,876 to Blaauw, PI: Dennis Sylvester, 1/1/20-12/31/21
- National Geographic Society, “M3 Monarch Migration Study,” \$150,000 with \$75,000 to Blaauw, PI: David Blaauw, 10/11/2019-10/10/2022
- ARM, “ULP Sensor Fusion SoC for Micro Robots and Tiny IoT,” \$320,000 with \$160,000 to Blaauw, PI: David Blaauw, 9/1/19-8/31/21
- Sony Corporation of America, “Ultra Low Power intelligent imaging sensors for the Internet of Things,” \$1,493,433, with \$511,041 to Blaauw, PI: Dennis Sylvester, 9/1/19-8/31/22
- Ministry of Defense “Ultra-Miniature Imager Technical Demonstrator,” \$1,057,762, with \$657,762 to Blaauw, PI: David Blaauw, 7/18/19-3/31/2021
- Ministry of Defense “M3 Audio-Logger,” \$1,204,352, with \$704,352 to Blaauw, PI: David Blaauw, 2/18/19-3/31/2021
- Semiconductor Research Corporation (SRC), “Mixed-Signal Circuits Enabling Ultra-Low Power Wireless Sensors,” \$270,000, with \$139,995 to Blaauw, PI: David Blaauw, 1/1/18-12/31/20
- Advanced Energy Consortium (AEC), “Millimeter Scale Down-hole Sensors,” \$650,000, with \$400,000 to Blaauw, PI: David Blaauw, 3/1/18-02/28/21
- National Science Foundation (NSF), “NCS FR - Elucidating the relationship between motor cortex neural firing rates and dextrous finger movement EMG for use in brain computer interfaces,” \$2,276,395, with \$194,603 to Blaauw, PI: Cindy Chestek, 9/1/19-8/31/23
- DARPA, “Domain-focused Advanced Software-reconfigurable Heterogeneous System-on-Chip (DASH-SoC),” \$2,420,233, with \$1,318,078 to Blaauw, PI: Hun-Seok Kim, 7/18/18-6/30/22
- National Science Foundation (NSF), “SHF: Medium: Compute Caches: Opportunistic Extreme Scale Parallelism In General Purpose Processors,” \$300,000, with \$80,579 to Blaauw, PI: Reetuparna Das, 10/1/18-9/30/20
- Leidos, “Trestle – small acoustic sensors” \$1,882,300, with \$983,104 to Blaauw, PI: David Blaauw, 5/3/19-2/28/2021

- National Institute of Health (NIH), “A 100 μ m Scale Single Unit Neural Recording Probe Using IR-Based Powering and Communication,” \$429,971, with \$224,890 to Blaauw, PI: David Blaauw, 9/1/18-8/31/2021
- DARPA, “Transmuter: A Reconfigurable Computer,” \$5,845,690, with \$1,524,096 to Blaauw, PI: Ron Dreslinski, 8/6/18-3/30/21
- DARPA, “OpenROAD: Foundations and Realization of Open, Accessible Design Integrated Circuits and Digital Signal Processing,” \$1,600,000, with \$248,754 to Blaauw, PI Andre Kahng, 6/1/18-5/31/22
- DARPA, “Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits,” \$3,199,021, with \$482,255 to Blaauw, PI: David Wentzloff, 6/12/18-6/11/20
- Leidos, “NZero Acoustic Switch (Dorado),” 930,000, with \$699,424 to Blaauw, PI: David Blaauw, 11/11/17-6/30/19
- National Institute of Standards and Technology (NIST), United States Department of Commerce (DoC), “Decimeter Accurate, Long Range Non-Line-of-Sight RF Localization Solution for Public Safety Applications,” \$997,873, with \$310,041 to Blaauw, PI: Hun Seok Kim, 6/1/17-5/31/21
- Ministry of Defense, “Highly Size Constrained Logging Sensor Development,” \$2,580,843, with \$1,131,882 to Blaauw, PI: David Blaauw, 10/01/16 – 08/15/18
- Sony Electronics, Inc., “Low Power Motion Detection for the Internet of Things,” 1,193,000, with \$400,000 to Blaauw, PI: Dennis Sylvester, 8/1/2016-12/31/2019
- DARPA, “Support for Porting S2CFF Design and Near-Threshold Voltage (NTV) Design Methodology to 32nm CMOS,” \$310,829 to Blaauw, PI: David Blaauw, 12/8/2015-8/31/2017
- DARPA, “Near Zero-Power, Continuous Acoustic Sensing Microsystem using Active Integrated Circuits and Digital Signal Processing,” \$2,505,000, with \$835,000 to Blaauw, PI: Dennis Sylvester, 9/28/2015-7/31/2019
- Semiconductor Research Corporation (SRC), “Infrared-Based Power Delivery and Communication for Implanted Sensors,” \$375,000 to Blaauw, PI: David Blaauw, 6/1/2015-5/31/2018
- Advanced Energy Consortium (AEC), “An Autonomous Microsystem Test-Bed for Extreme Environments: Strategic Options and Scalability Limits,” \$1,170,000, with \$585,000 to Blaauw, PI: David Blaauw, 1/1/2015-7/1/2017
- ARM Ltd, “ARM III: Research into Low Energy Computer Systems,” \$3,000,148, with \$555,555 to Blaauw, PI: Trevor Mudge, 2015-2018
- National Institute of Health (NIH), “SCH: INT: Wireless Implantable Electronic Biosensors for Tumor Monitoring,” \$1,759,460 with \$849,804 to Blaauw, PI: David Blaauw, 9/22/2014 - 8/31/2018
- Ministry of Defense, “M3 mm scale computing GPS logger,” \$1,352,145, with \$250,000 to Blaauw, PI: David Blaauw, 04/01/14 - 03/31/16
- Ministry of Defense, “Dstl Sensor Development Kits,” \$400,000, with \$112,500 to Blaauw, PI: David Blaauw, 12/13/13 - 3/17/14
- Ministry of Defense, “Architectural Design Study for M3 mm Scale Computing GPS Logger,” \$400,000, with \$175,000 to Blaauw, PI: David Blaauw, 8/15/2013-3/14/2014
- National Science Foundation (NSF), “SHF: Small: Minimally Invasive Error Detection/Correction for Runtime Margin Elimination,” \$450,000, with \$252,750 to Blaauw, PI: David Blaauw, 7/2012-6/2015
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” \$400,000, with \$135,000 to Blaauw, PI: Kamal Sarabandi, 9/2013-8/2016

- DARPA, “The TerraSwarm Research Center,” \$4,234,183, with \$1,624,897 to Blaauw, PI: Edward Lee, 1/15/2013-12/31/2017
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$5,000,000, with \$925,000 to Blaauw, PI: Trevor Mudge, 5/2010-5/2015
- Advanced Energy Consortium (AEC), “An Autonomous Microsystem Test-Bed for Extreme Environments: Integrating Sensor Elements, Electronics, and Packaging,” \$950,000, with \$226,625 to Blaauw, PI: Yogesh Gianchandani, 6/2012-12/2014
- Semiconductor Research Corporation (SRC), “Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors,” \$360,000, with \$180,000 to Blaauw, PI: David Blaauw 8/2012 - 7/2015
- DARPA, “Systems on Nanoscale Information Fabrics (SONIC) Center,” \$7,008,335, with \$1,401,667 to Blaauw PI: Naresh Shanbhag, 1/2013-10/2017
- Ministry of Defense, “MM scale computing for GPS logger,” \$400,000, with \$175,000 to Blaauw, PI: David Blaauw
- Isocline Engineering LLC, “Power Efficient Software Define Radio (SDR) Mobile Architecture Technology for Handheld Devices,” \$220,093 to Blaauw, PI: David Blaauw, 03/01/2013 - 02/28/2015
- Isocline Engineering LLC, “Programmable Microchip for Accelerating Neuromorphic Object Recognition,” \$45,715 to Blaauw, PI: David Blaauw, 07/01/2013 - 12/31/2013
- QUALCOMM, “Near Threshold Computing,” \$100,000, gift, 8/2011-8/2013
- Oracle, “High Performance Razor Architecture” \$80,000, gift, 8/2013-8/2014
- AMD, “*In Situ* Wearout Detection and Mitigation,” \$100,000, gift, with \$50,000 to David Blaauw, 11/2011
- Food and Drug Administration, “Smart Rapid Palatal Expander for Pediatric Cleft and Palate Patients,” \$312,000, with \$136,000 to Blaauw, PI: Jeanne Nervina, 9/2011-8/2013
- National Science Foundation (NSF), “Integrating Circuits, Sensing, and Software to Realize the Cubic-mm Computing Class,” \$2,533,000, with \$519,265 to Blaauw, PI: David Wentzloff, 08/2011 - 7/2016
- Qualcomm, “Near-Threshold Computing,” \$50,000, gift, PI: David Blaauw, 05/2011
- Department of Energy, “Hardware-Software Co-Design for Non-Volatile Memory in Exascale Systems,” \$525,000 with \$202,747 to Blaauw, PI: Trevor Mudge, 1/2011-12/2013
- Intel Corporation, “A Confidence-Driven Model for Predictable Computing in Future Technologies,” \$249,000 with \$65,916 to Blaauw, PI: Zhengya Zhang, 1/2010-10/2010
- QUALCOMM, “Adaptive Design Solutions for VLSI Circuits,” \$50,000, gift, 09/01/09
- National Science Foundation (NSF), “Reclaiming Moore’s Law through Ultra Energy Efficient Computing,” \$2,778,507, with \$643,700 to Blaauw, PI: Prof. David Blaauw, 9/2009-08/2014
- National Science Foundation (NSF), “Probabilistic Wearout in Nanoscale,” \$300,000, with \$150,000 to Blaauw, PI: Dennis Sylvester, 8/2008-7/2011
- IBM Corporation/Defense Advanced Research Projects Agency (DARPA), “Strained Si/SiGe/Ge Heterojunction Tunneling Transistor (HETT) e with Steep Subthreshold Slope for Extremely Low Power Electronics,” \$17,971,252, with \$600,000 to Blaauw, PI: Steve Koester, 1/2008-12/2009
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” \$8,962,200 with \$700,000 to Blaauw, PI: Kamal Sarabandi, 5/2008-5/2013
- Intel Corporation, “Adaptive Digital Design in the Nanometer Regime,” \$100,000, gift, 3/2008-3/2010

- Sun Microsystems, “Robust Low Voltage SRAM Design,” \$150,000, gift, 9/2007-9/2010
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design,” \$40,000, gift, 7/2007
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Elastic: An Adaptive Self-Healing Architecture for Unpredictable Silicon,” \$600,000 to Blaauw, PI: David Blaauw, 9/2006 - 9/2009
- Semiconductor Research Corporation (SRC), “A Design Optimization Framework for Process Variation Tolerance,” \$390,000, with \$195,000 to Blaauw, PI: Dennis Sylvester, 9/2006 - 8/2009
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” \$40,000, gift, 7/2006
- Semiconductor Research Corporation (SRC), “CAD Solutions for Parametric Yield Optimization,” \$321,000, with \$160,000 to Blaauw, PI Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2005-7/2008
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” \$40,000, gift, 7/2005
- NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), “Sub-threshold Processor Design,” \$60,000 to Blaauw, PI: Kenneth Wise, 5/2005-5/2010
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$5,000,000, with approx. \$1,600,000 to Blaauw, PI: Trevor Mudge, 5/2005-5/2010
- Semiconductor Research Corporation (SRC), “Optimization of Lithographic Induced Variability for Improved Circuit Performance,” \$161,029 to Blaauw, PI: David Blaauw, 9/2004-8/2007
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2004
- Photonics, Inc. \$75,000, gift, 6/2004-5/2005
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$240,000, with \$60,000 to Blaauw, PI: Trevor Mudge, 5/2004-5/2005
- National Science Foundation (NSF), Information Technology Research (ITR), “Collaborative Research ITR: Mobile Supercomputing,” \$1,900,000, with \$320,603 to Blaauw, PI: Trevor Mudge, 11/2003-11/2007
- Intel Corporation, “VLSI Design Curriculum,” \$247,292, with \$61,823 to Blaauw, PI: Richard Brown, 10/2003-10/2004
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Power Aware Systems,” \$600,000, PI: David Blaauw, 9/2003-9/2006
- IBM Corporation, Center for Advanced Studies, “Static Performance Analysis under Process and Environment Variations,” \$40,000, Faculty Award, 9/2003
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2003
- Semiconductor Research Corporation (SRC), “Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current,” \$360,000, with \$160,000 to Blaauw, PI: David Blaauw, 7/2003-7/2006
- National Science Foundation (NSF), “Performance Analysis and Optimization for Nanometer Design,” \$375,000, PI: David Blaauw, 6/2003-6/2006
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$240,000, with \$60,000 to Blaauw, PI: Trevor Mudge, 5/2003-5/2004
- IBM Corporation, Center for Advanced Studies, “Leakage Characterization and Analysis,” \$40,000, Faculty Award, 9/2002

- National Science Foundation (NSF), Information Technology Research (ITR), “Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty”, \$1,800,00 with \$450,000 to Blaauw, PI: David Blaauw, 8/2002-8/2006
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2002
- MARCO/DARPA - Giga-Scale Research Center (GSRC), “Power Management for Nanometer design,” \$197,000, PI: David Blaauw, 10/2001-8/2003
- Semiconductor Research Corporation (SRC), “Variability in Chip-Level Performance and Signal Integrity Verification,” \$257,000, PI: David Blaauw, 10/2001-10/2004

IV Teaching Experience

<u>Semester</u>	<u>Class</u>	<u>Course Number</u>	<u>Size</u>	<u>Rating (out of 5) Course/Instructor</u>
Winter 2021	Advanced VLSI Design	EECS 627	27	4.3/4.2
Winter 2020	Advanced VLSI Design	EECS 627	26	4.5/4.3
Winter 2019	Advanced VLSI Design	EECS 627	24	4.5/4.6
Winter 2018	Advanced VLSI Design	EECS 627	18	4.08/4.75
Fall 2016	VLSI Design I	EECS 427	36	4.85/4.91
Fall 2015	Digital Integrated Circuits	EECS 312	35	4.58/4.81
Fall 2014	Advanced VLSI Design II	EECS 628	26	4.86/4.90
Winter 2014	Advanced VLSI Design	EECS 627	38	4.77/4.77
Fall 2013	VLSI Design I	EECS 427	39	4.74/4.78
Winter 2013	Introduction to Electronic Circuits	EECS 215	120	3.56/4.09
Winter 2012	Advanced VLSI Design	EECS 627	37	4.87/4.87
Fall 2011	VLSI Design I (Section 2)	EECS 427	18	4.79/4.79
Fall 2011	VLSI Design I (Section 1)	EECS 427	35	4.83/4.83
Winter 2011	Advanced VLSI Design	EECS 427	9	4.88/4.88
Fall 2010	Advanced VLSI Design II	EECS 628	19	4.81/5.00
Winter 2010	Advanced VLSI Design	EECS 627	19	4.85/4.96
Winter 2009	Advanced VLSI Design	EECS 627	23	4.75/4.75
Fall 2008	VLSI Design I	EECS 427	28	4.67/4.56
Winter 2007	Advanced VLSI Design	EECS 627	20	4.79
Fall 2006	VLSI Design I	EECS 427	31	4.89
Winter 2006	Advanced VLSI Design	EECS 627	22	4.55
Fall 2005	Topics in VLSI Design	EECS 598	12	4.25

Winter 2005	Advanced VLSI Design	EECS 627	20	4.79
Winter 2004	Advanced VLSI Design	EECS 627	35	4.59
Fall 2003	Introduction to Logic Design	EECS 270	87	4.77
Winter 2003	Advanced VLSI Design	EECS 627	36	4.61
Fall 2002	Introduction to Logic Design	EECS 270	109	4.77
Winter 2002	Advanced VLSI Design	EECS 627	40	4.31
Fall 2001	Issues in High-Performance Deep-Submicron Design	EECS 598	11	4.75

V Publications

A. Books

1. Ashish Srivastava, Dennis Sylvester and David Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*, Kluwer Academic Publishers, 2005

B. Book Chapters

1. Tutu Ajayi, Sumanth Kamineni, Morteza Fayazi, Yaswanth K. Cherivirala, Kyumin Kwon, Shourya Gupta, Wenbo Duan, Jeongsup Lee, Chien-Hen Chen, Mehdi Saligane, Dennis Sylvester, David Blaauw, Ronald Dreslinski Jr, Benton Calhoun, David D. Wentzloff, "Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation," in *IFIP/IEEE International Conference on Very Large Scale Integration - System on a Chip*, K. A. A. Makinwa, A. Baschiroto, and P. Harpe, Eds. Springer International Publishing, 2021
2. Sechang Oh, Yao Shi, Gyouho Kim, Yejoong Kim, Taewook Kang, Seok Hyeon Jeong, Dennis Sylvester, David Blaauw, "Low-Power Resistive Bridge Readout Circuit Integrated in Two Millimeter-Scale Pressure-Sensing Systems," in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers: Advances in Analog Circuit Design 2018*, K. A. A. Makinwa, A. Baschiroto, and P. Harpe, Eds. Springer International Publishing, 2019
3. Sechang Oh, Wanyeong Jung, Hyunsoo Ha, Jae-Yoon Sim, David Blaauw, "Energy-Efficient CDCs for Millimeter Sensor Nodes," in *Efficient Sensor Interfaces, Advanced Amplifiers and Low Power RF Systems: Advances in Analog Circuit Design 2015*, K. A. A. Makinwa, A. Baschiroto, and P. Harpe, Eds. Springer International Publishing, 2016
4. Shidhartha Das, David Roberts, David Blaauw, David Bull, Trevor Mudge, "Architectural Techniques for Adaptive Computing", Chapter in *Adaptive Techniques for Dynamic Processor Optimization: Theory and Practice*, Alice Wang and Sam Naffziger, editors, Springer Publishing Company, 2008
5. David Blaauw, Sanjay Pant, Rajat Chaudhry and Rajendran Panda, "Design and Analysis of Power Supply Networks," Chapter in *Electronic Design Automation for Integrated Circuits Handbook*, Louise Sheffer, Luciano Lavagno and Grant Martin, editors, CRC Press, 2005
6. Sarvesh Kulkarni, Ashish Srivastava, Dennis Sylvester, David Blaauw, "Power Optimization Techniques using Multiple Supply Voltages," Chapter in *Closing the Power Gap between ASIC and Custom*, David Chinnery and Kurt Keutzer, editors, Kluwer Academic Publishers, 2005
7. Dongwoo Lee, Bo Zhai, David Blaauw, Dennis Sylvester, "Static Leakage Reduction through Simultaneous V_{t}/T_{ox} and State Assignment," Chapter in *Ultra Low-Power Electronics and Design*, Enrico Macii, editor, Kluwer Academic Publishers, 2004
8. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, "Design and Analysis of Power Distribution Networks for Processor Design," Chapter in *IEEE Design of High Performance Microprocessors Circuits*, Anantha Chandrakasan, William Bowhill, and Frank Fox, editors, IEEE Press, 2000
9. Abhijit Dharchoudhury, Shantanu Ganguly, David Blaauw, "Timing and Signal Integrity Analysis," Chapter in *Handbook for VLSI Design*, Wai Kai Chen, editor, IEEE Press, 2000

C. Invited Articles

1. Li Xu, David Blaauw and Dennis Sylvester, "Ultra-Low Power 32kHz Crystal Oscillators: Fundamentals and Design Techniques," *Open Journal of the Solid-State Circuits Society*, Vol. 1, September 2021, pgs. 79-93

2. Li Xu, Jeongsup Lee, Mehdi Saligane, David Blaauw, Dennis Sylvester, "Design Techniques of Integrated Power Management Circuits for Low Power Edge Devices," IEEE Custom Integrated Circuits Conference (CICC), April 2021
3. Sechang Oh, Minchang Cho, Xiao Wu, Yejoong Kim, Li-Xuan Chuo, Wootae Lim, Pat Pannuto, Suyoung Bang, Kaiyuan Yang, Hun-Seok Kim, Dennis Sylvester, David Blaauw, "IoT2 — the Internet of Tiny Things: Realizing mm-Scale Sensors through 3D Die Stacking," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2019, pgs. 686-691
4. David Blaauw, "Unlocking New IoT Application Domains Through Ultra-Low Power mm-Scale Sensor Node Design," Keynote Address at ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), July 2018
5. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyong Foo, Hyeongseok Kim, Anthony Grbic, Dennis Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor Nodes with illustration in a miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 64, No. 9, September 2017, pgs. 2237-2249
6. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyong Foo, Hyeongseok Kim, Anthony Grbic, Dennis Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor nodes with Illustration in a Miniaturized GNSS Logger for Position Tracking: Part II—Data Communication, Energy Harvesting, Power Management and Digital Circuits," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 64, No. 9, September 2017, pgs. 2250-2262
7. Wanyeong Jung, Dennis Sylvester, David Blaauw, "Low-Power Switched-Capacitor Converter Techniques for Small IoT Systems," European Conference on Circuit Theory and Design (ECTD), September 2017
8. Taekwang Jang, Myungjoon Choi, Yao Shi, Inhee Lee, Dennis Sylvester and David Blaauw, "Millimeter-Scale Computing Platform for Next Generation of Internet of Things," IEEE International Conference on RFID (RFID), May 2016
9. Taekwang Jang, Seokhyeon Jeong, Myungjoon Choi, Wanyeong Jung, Gyouho Kim, Yen-Po Chen, Yejoong Kim, Wootae Lim, Dennis Sylvester, David Blaauw, "Key Building Blocks and Integration Strategy of a Miniaturized Wireless Sensor Node," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2015
10. Nathaniel Pinckney, David Blaauw, Dennis Sylvester, "Low Power Near-Threshold Design," IEEE Solid-State Circuits Magazine, June 2015
11. Inhee Lee, Yejoong Kim, Suyoung Bang, Gyouho Kim, Hyunsoo Ha, Yen-Po Chen, Dongsuk Jeon, Seokhyun Jeong, Wanyeong Jung, Mohammad Hassan Ghaed, Zhiyong Foo, Yoonmyung Lee, Jae-Yoon Sim, Dennis Sylvester, and David Blaauw, "Circuit Techniques for Miniaturized Bio-medical Sensors," IEEE Custom Integrated Circuits Conference (CICC), September 2014
12. David Blaauw, Dennis Sylvester, Prabal Dutta, Yoonmyung Lee, Inhee Lee, Sechang Bang, Yejoong Kim, Gyouho Kim, Pat Pannuto, Ye-Shang Kuo, Dongmin Yoon, Wanyeong Jung, Zhiyong Foo, Yen-Po Chen, Seok Hyeon Jeong, Myungjoon Choi, "IoT Design Space Challenges: Circuits and Systems" 2014 IEEE Symposium on VLSI Technology, June 2014
13. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Circuits for Ultra-Low Power Millimeter-Scale Sensor Nodes," 2012 Asilomar Conference on Signals, Systems and Computers (Asilomar), November 2012

14. David Blaauw, Dennis Sylvester, Yoonmyung Lee, Inhee Lee, Suyoung Bang, Yejoong Kim, Gyouho Kim, Hassan Ghaed, "From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design," **Invited paper** to the IEEE Subthreshold Microelectronics Conference (SubVt), Plenary Keynote, October 2012
15. Nathaniel Pinckney, Korey Sewell, Ronald Dreslinski, Dave Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Assessing the Performance of Parallelized Near-Threshold Computing," ACM/IEEE Design Automation Conference (DAC), June 2012
16. Yoonmyung Lee, YeJoong Kim, Dongmin Yoon, David Blaauw, Dennis Sylvester, "Circuit and System Design Guidelines for Ultra-Low Power Sensor Nodes," ACM/IEEE Design Automation conference (DAC), June 2012
17. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Synchronization of Ultra-Low Power Wireless Sensor Nodes", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2011
18. Gregory Chen, Scott Hanson, David Blaauw, Dennis Sylvester, "Circuit Design Advances for Wireless Sensing Applications," Proceedings of the IEEE, Special Issue on Wireless Sensor Networks, Vol. 98, No. 11, November 2010, pg. 1808 - 1827
19. Prashant Singh, Dennis Sylvester, David Blaauw, "Adaptive Sensing and Design for Reliability," IEEE International Reliability Physics Symposium, May 2010
20. Ronald G. Dreslinski, Michael Wieckowski, David Blaauw, Dennis Sylvester, Trevor Mudge, "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," Proceedings of the IEEE, Special Issue on Ultra-Low Power Circuit Technology, Vol. 98, No. 2, February 2010, pg. 253 - 266
21. Prashant Singh, Cheng Zhuo, Eric Karl, David Blaauw, Dennis Sylvester, "Sensor Driven Reliability and Wearout Management," *IEEE Design and Test of Computers (D&T)*, Vol. 26, No. 6, November/December 2009, pg. 40 - 49
22. David Blaauw, Shidhartha Das, "CPU, Heal Thyself," IEEE Spectrum, August 2009
23. Shidhartha Das, David Blaauw, David Bull, Krisztian Flautner, Rob Aitken, "Addressing Design Margins through Error-tolerant Circuits," ACM/IEEE Design Automation Conference (DAC), July 2009
24. Shidhartha Das, David Blaauw, "Adaptive Design for Nanometer Technology," IEEE International Symposium on Circuits and Systems (ISCAS), May 2009
25. Dennis Sylvester, Scott Hanson, Seok, Yu-Shiang Lin, David Blaauw, "Designing Robust Ultra-Low Power Circuits," International Electron Devices Meeting (IEDM), December 2008
26. David Blaauw, Kaviraj Chopra, Ashish Srivastava, Lou Sheffer, "Statistical Timing Analysis: Basic Principles to State-of-the-Art," *Transactions on Computer-Aided Design of Integrated Circuits and Systems (T-CAD)*, invited review article, Vol. 27, No. 4, April 2008, pg. 589-607
27. Scott Hanson, Bo Zhai, David Blaauw, Dennis Sylvester, "Energy-Optimal Circuit Design," IEEE International SoC Design Conference, November 2007
28. Sanjay Pant, Eli Chiprout, David Blaauw, "Power Grid Physics and Implications for CAD," *IEEE Design and Test of Computers (D & T)*, Vol. 24, No. 3, May-June 2007, pg. 246-254
29. Dennis Sylvester, Scott Hanson, Bo Zhai, and David Blaauw, "Design strategies for ultra-low voltage circuits," IEEE International SoC Design Conference, September 2006

30. Scott Hanson, Bo Zhai, David Blaauw, Dennis Sylvester, Andres Bryant, Xinlin Wang, "Energy Optimality and Variability in Subthreshold Design," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
31. Shidhartha Das, David Roberts, Seokwoo Lee, Sanjay Pant, David Blaauw, Todd Austin, Trevor Mudge, Krisztián Flautner, "A Self-Tuning Dynamic Voltage Scaled Processor Using Delay-Error Detection and Correction," IEEE International Conference on Integrated Circuit Design & Technology (ICICDT), May 2006
32. David Blaauw and Bo Zhai, "Energy Efficient Design for Subthreshold Supply Voltage Operation," IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
33. Rajeev R. Rao, David Blaauw, Dennis Sylvester, Anirudh Devgan, "Modeling and Analysis of Parametric Yield Under Power and Performance Constraints," *IEEE Design and Test of Computers (D&T)*, Vol. 22, No. 4, July-August 2005, pg. 376-385
34. Todd Austin, Valeria Bertacco, David Blaauw, Trevor Mudge, "Opportunities and Challenges for Better Than Worst-Case Design," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005, pg. I-2
35. Bo Zhai, David Blaauw, Dennis Sylvester, Krisztián Flautner, "Extended Dynamic Voltage Scaling for Low Power Design," IEEE International SOC Conference, September 2004, pg. 389-394
36. Todd Austin, David Blaauw, Trevor Mudge, Krisztián Flautner, "Making Typical Silicon Matter with Razor" *IEEE Computer*, March 2004, pg. 57-65
37. David Blaauw, Kaushik Gala, "Inductance: Implications and Solutions for High-Speed Digital Circuits - Inductance Extraction and Modeling," IEEE International Solid-State Circuits Conference (ISSCC), February 2002, pg. 548-553
38. David Blaauw, "Signal Integrity Issues in High Performance Design," IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (Patmos), September 2001, pg. 5.1.1-5.1.4
39. Kaushik Gala, David Blaauw, Junfeng Wang, Vladimir Zolotov, Min Zhao, "Inductance 101: Analysis and Design Issues," ACM/IEEE Design Automation Conference (DAC), June 2001, pg. 329-334
40. David Blaauw, Kaushik Gala, Vladimir Zolotov, Rajendran Panda, Junfeng Wang, "On-Chip Inductance Modeling," ACM/IEEE Great Lake Symposium on VLSI Design (GLSVLSI), March 2000, pg. 75-80
41. David Blaauw, "Power Management Issues in High Performance Processor Design," IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2
42. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, Supamas Sirichotiyakul, Chanhee Oh, Tim Edwards, "Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 1998, pg. 143-148
43. Abhijit Dharchoudhury, Rajendran Panda, David Blaauw, Ravi Vaidyanathan, Bogdan Tutuianu, David Bearden, "Methodology for the Design and Analysis of Power Distribution Networks on the PowerPC Microprocessor," ACM/IEEE Design Automation Conference (DAC), June 1998, pg. 738-743

D. Journals

1. Hyochan An, Samuel R. Nason-Tomaszewski, Jongyup Lim, Kyumin Kwon, Matthew S. Willsey, Parag G. Patil, Hun-Seok Kim, Dennis Sylvester, Cynthia A. Chestek, and David Blaauw "A

- Power-Efficient Brain-Machine Interface System with a Sub-mW Feature Extraction and Decoding ASIC Demonstrated in Nonhuman Primates,” *IEEE Transactions on Biomedical Circuits and Systems*, accepted
2. Jack Wadden, Brandon Newell, Joshua Bugbee, Vishal John, Amy K. Bruzek, Robert P. Dickson, Carl Koschmann, David Blaauw, Satish Narayanasamy, Reetuparna Das, “Ultra-Rapid Somatic Variant Detection via Real-Time Targeted Amplicon Sequencing,” *Communications Biology*
 3. Joseph T. Costello, Samuel R. Nason-Tomaszewski, Hyochan An, Jungho Lee, Matthew J. Mender, Hisham Temmar, Dylan M. Wallace, Jongyup Lim, Matthew S. Willsey, Parag G. Patil, Taekwang Jang, Jamie D. Phillips, Hun-Seok Kim, David Blaauw, Cynthia A. Chestek, “A low-power communication scheme for wireless, 1000 channel brain-machine interfaces,” *Journal of Neural Engineering*, accepted
 4. Jongyup Lim, Jungho Lee, Eunseong Moon, Michael Barrow, Gabriele Atzeni, Joseph G. Letner, Joseph T. Costello, Samuel R. Nason, Paras R. Patel, Yi Sun, Parag G. Patil, Hun-Seok Kim, Cynthia A. Chestek, Jamie Phillips, David Blaauw, Dennis Sylvester, Taekwang Jang, “A Light Tolerant Wireless Neural Recording IC for Motor Prediction with Near-Infrared-based Power and Data telemetry,” *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, January 2022
 5. Sujin Park, Ji-Hwan Seol, Li Xu, SeongHwan Cho, Dennis Sylvester, David Blaauw, “A 43nW, 32kHz, ± 4.2 ppm Piece-Wise Linear Temperature Compensated Crystal Oscillator with $\Delta\Sigma$ Modulated Load Capacitance,” *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, January 2022
 6. Sung Kim, Morteza Fayazi, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor Mudge, Chaitali Chakrabarti, David Blaauw, Ronald Dreslinski, Hun-Seok Kim, “Versa: A 36-Core Systolic Multiprocessor with Dynamically-Reconfigurable Interconnect and Memory,” *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, Vol. 57, No. 4, January 2022, pgs. 986-998
 7. Ji-Hwan Seol, Kyojin Choo, David Blaauw, Dennis Sylvester, Taekwang Jang, “A Reference Oversampling PLL achieving -256 -dB FoM and -78 -dBc Reference Spur,” *IEEE Journal of Solid-State Circuits (JSSC)*, **Invited Paper** to the *Special Issue on ASSCC 2020*, Vol. 56, No. 10, October 2021, pgs. 2993-3007
 8. Li Xu, Kyojin Choo, David Blaauw, Dennis Sylvester, “An Analog-Assisted Digital LDO with Single Subthreshold Output PMOS Achieving 1.44fs FOM,” *IEEE Solid-State Circuits Letters*, August 2021, pgs. 154 - 157
 9. Li Xu, Taekwang Jang, Jongyup Lim, Kyojin Choo, David Blaauw, and Dennis Sylvester, “A 510pW 32kHz Crystal Oscillator with High Energy-to-Noise-Ratio Pulse Injection,” *IEEE Journal of Solid-State Circuits (JSSC)*, July 2021
 10. Cindy S. Bick, Inhee Lee, David Blaauw, Trevor Coote, Amanda E. Haponski, and Diarmaid Ó Foighil, “Millimeter-sized smart sensors reveal that a solar refuge protects tree snail *Partula hyalina* from extirpation,” *Communications Biology*, June 2021
 11. Jongyup Lim, Jungho Lee, Eunseong Moon, Michael Barrow, Gabriele Atzeni Joseph Letner, Joseph Costello, Samuel R. Nason, Paras R. Patel, Parag G. Patil, Hun-Seok Kim, Cynthia A. Chestek, Jamie Phillips, David Blaauw, Dennis Sylvester, Taekwang Jang, “A Light Tolerant Neural Recording IC for Near-Infrared-Powered Free Floating Motes,” *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, June 2021
 12. Rohit Rothe, Minchang Cho, Kyojin Choo, Seokhyeon Jeong, Sechang Oh, Dennis Sylvester, David Blaauw, “A 192 nW 0.02 Hz High Pass Corner Acoustic Analog Front-End with Automatic

- Saturation Detection and Recovery,” *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, June 2021
13. Najme Ebrahimi, Hun Seok Kim, David Blaauw, “Physical Layer Secret Key Generation Using Joint Interference and Phase-Shift Keying Modulation” *IEEE Transaction on Microwave Theory and Techniques (TMTT)*, Vol. 69, No. 5, May 2021, pgs. 2673-2685
 14. Eunseong Moon, Michael Barrow, Jongyup Lim, Jungho Lee, Samuel Nason, Joseph Costello, Hun Seok Kim, Cynthia Chestek, Taekwang Jang, David Blaauw, Jamie Phillips, “Bridging the Last Millimeter Gap of Brain-Machine Interfaces via Near-Infrared Wireless Power Transfer and Data Communications,” *ACS Photonics*, Vol. 8, No. 5, April 2021, pgs. 1430–1438
 15. Xiao Wu, Arun Subramaniyan, Zhehong Wang, Satish Narayanasamy, Reetuparna Das, David Blaauw, “A High-Throughput Pruning-based Pair-Hidden-Markov-Model Hardware Accelerator for Next-Generation DNA Sequencing,” *IEEE Solid-State Circuits Letters*, **Invited Paper** to the *Special Issue on VLSI 2020*, Vol. 4, 2021, pgs. 31-35
 16. Ziyun Li, Zhehong Wang, Li Xu, Qing Dong, Bowen Liu, Chin-I Su, Wen-Ting Chu, George Tsou, Yu-Der Chih, Tsung-Yung Jonathan Chang, Dennis Sylvester, Hun-Seok Kim, David Blaauw, “RRAM-DNN: An RRAM and Model-Compression Empowered All-Weights-on-Chip DNN Accelerator,” *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2020*, Vol. 56, No. 4, April 2021, pgs. 1105-1115
 17. Jingcheng Wang, Hyochan An, Qirui Zhang, Hun Seok Kim, David Blaauw, Dennis Sylvester, “A 40nm Ultra-low Leakage Voltage-Stacked SRAM for Intelligent IoT Sensors,” *IEEE Solid-State Circuits Letters*, **Invited Paper** to the *Special Issue on VLSI 2020*, April 2021, Vol. 4, 2021, pgs. 14-17
 18. Hyochan An, Sam Schiferl, Siddharth Venkatesan, Tim Wesley, Qirui Zhang, Jingcheng Wang, Kyojin Choo, Shiyu Liu, Bowen Liu, Ziyun Li, Luyao Gong, Hengfei Zhong, David Blaauw, Ronald Dreslinski, Hun Seok Kim, Dennis Sylvester, “An Ultra-low-power Image Signal Processor for Hierarchical Image Recognition with Deep Neural Networks,” *IEEE Journal of Solid-State Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2020*, Vol. 56, No. 4, April 2021, pgs. 1071-1081
 19. Zhehong Wang, Tianjun Zhang, Daichi Fujiki, Arun Subramaniyan, Xiao Wu, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, Reetuparna Das, Satish Narayanasamy, David Blaauw, “A 2.46M reads/s Seed-Extension Accelerator for Next-Generation-Sequencing using a String-Independent PE Array,” *IEEE Solid-State Circuits Letters*, **Invited Paper** to the *Special Issue on CICC 2020*, Vol. 56, No. 3, March 2021, pgs. 824-833
 20. Eunseong Moon, Michael Barrow, Jongyup Lim, David Blaauw, Jamie D. Phillips, “Dual-Junction GaAs Photovoltaics for Low Irradiance Wireless Power Transfer in Sub Millimeter-scale Sensor Nodes,” *IEEE Journal of Photovoltaics*, Vol. 10, No. 6, November 2020, pg. 1721-1726
 21. Ji-Hwan Seol, Kyojin Choo, David Blaauw, Dennis Sylvester, Taekwang Jang, “A 67-fs_{rms} Jitter, –130 dBc/Hz In-Band Phase Noise, –256-dB FoM Reference Oversampling Digital PLL With Proportional Path Timing Control,” *IEEE Solid-State Circuits Letters*, **Invited Paper** to the *Special Issue on ASSCC 2020*, Vol. 3, September 2020, pg. 430-433
 22. Samuel R. Nason, Alex K. Vaskov, Matthew S. Willsey, Elissa J. Welle, Hyochan An, Philip P. Vu, Autumn J. Bullard, Chrono S. Nu, Jonathan C. Kao, Krishna V. Shenoy, Taekwang Jang, Hun-Seok Kim, David Blaauw, Parag G. Patil, Cynthia A. Chestek, “A low-power band of neuronal spiking activity dominated by local single units improves the performance of brain–machine interfaces,” *Nature Biomedical Engineering*, Vol. 4, July 2020, pg. 973-983

23. Jeongsup Lee, Mehdi Saligane, David Blaauw and Dennis Sylvester, "A 0.3V to 1.8–3.3V Leakage-Biased Synchronous Level Converter for ULP SoCs," *IEEE Solid-State Circuits Letters*, Vol. 3, July 2020, pg. 130 - 133
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E. Conference Papers

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2. Qirui Zhang, Hyochan An, Zichen Fan, Zhehong Wang, Ziyun Li, Guanru Wang, Hun-Seok Kim, David Blaauw and Dennis Sylvester, "A 22nm 3.5TOPS/W Flexible Micro-Robotic Vision SoC with 2MB eMRAM for Fully-on-Chip Intelligence," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2022
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44. Daksh Lenther, Satya Pallela, David Blaauw, Shantanu Ganguly, "Hierarchical Clock-network Optimization," ACM Physical Design Workshop, April 1996, pg. 49-54
45. John Willis, Rob Newshutz, Lance Thompson, Jeff Graves, Tom Dillinger, Jeff Snyder, Nimish Radia, Joe Skovira, David Blaauw, Sidhartha Mohanty, Zhiyuan Li, Sandra Samelson, Matt Lin, "MinSim: Optimized, Compiled VHDL Simulation Using Networked & Parallel Computers," IEEE VHDL International User Forum, October 1993, pg. 137-144

G. Patents Issued

1. "Millimeter-Scale Bluetooth Low Energy transmitter with dual purpose loop antenna," Patent number 10,911,078, issued February 2, 2021
2. "Low-Power, Long-Range RF Localization System and Method," Patent number 10,746,844, issued August 18, 2020

3. "Analog-To-Digital Conversion Circuit and Image Sensor Including the Same," Patent Number 10,594,333, issued March 17, 2020
4. "Variation-tolerant voltage reference," Patent number 10310537, issued June 4, 2019
5. "Intraocular pressure sensor with improved voltage reference circuit," Patent number 10,285,590, issued May 14, 2019
6. "Self-oscillating switched-capacitor DC-DC converter," Patent number 9,979,284, issued May 22, 2018
7. "Floating-gate transistor array for performing weighted sum computation," Patent number 9,760,533, issued September 12, 2017
8. "Electrostatic discharge clamp circuit for ultra-low power applications," Patent number 9,716,381, issued July 25, 2017
9. "Measurement circuitry and method for measuring a clock node to output node delay of a flip-flop," Patent number 9,638,752, issued May 2, 2017
10. "Ultra Low Power Temperature Insensitive Current Source With Line and Load Regulation," Patent Number 9,639,107, issued May 2, 2017
11. "Protocol for an electronic device to receive a data packet from an external device," Patent number 9,635,147, issued April 25, 2017
12. "Integrated circuit using topology configurations," Patent Number 9,589,601 issued March 7, 2017
13. "Single Cycle Arbitration Within an Interconnect," Patent Number 9,514,074 B2 issued December 6, 2016
14. "Error recovery within integrated circuit," Patent Number 9,448,875, issued September 20, 2016
15. "Storage Device Supporting Logical Operations, Methods and Storage Medium," Patent Number 9,396,795, issued July 19, 2016.
16. "Low Power Oscillator with Charge Subtraction Scheme," Patent Number 9,385,692, July 5, 2016
17. "True random number generator," Patent Number 9,335,972, May 10, 2016
18. "Memory Circuit Including Read Voltage Boost," Patent Number 9,275,702 issued March 1, 2016
19. "Error Recovery Within Integrated Circuit," Patent Number 9,164,842 issued October 20, 2015
20. "Low Power Reference Current Generator with Tunable Temperature," Patent Number 9,147,443 issued September 29, 2015
21. "Randomized Value Generation," Patent Number 8,930,427 issued January 6, 2015
22. "Crossbar circuitry for applying an adaptive priority scheme," Patent Number 8,868,817 issued October 21, 2014
23. "Apparatus and Method for Transferring a Data Signal Propagated Along a Bidirectional Communication Path Within a Data Processing Apparatus," Patent Number 8,713,232 issued April 29, 2014
24. "Error Recovery Within Integrated Circuit" Patent Number 8,650,470 issued February 11, 2014
25. "Reference voltage generator having a two transistor design," Patent Number 8,564,275 issued October 22, 2013
26. "Crossbar circuitry for applying an adaptive priority scheme and method of operation of such crossbar circuitry," Patent Number 8,549,207 issued October 1, 2013
27. "Integrated circuit memory power supply," Patent Number 8,526,261 issued September 3, 2013

28. "Vertical interconnect patterns in multi-layer integrated circuits," Patent Number 8,381,155 issued February 19, 2013
29. "Random Number Generator," Patent Number 8,346,832 issued January 1, 2013
30. "Cache memory system for a data processing apparatus," Patent Number 8,335,122 issued December 18, 2012
31. "Stalling synchronization circuits in response to a late data signal," Patent Number 8,276,014 issued September 25, 2012
32. "Crossbar circuitry for applying a pre-selection prior to arbitration between transmission requests and method of operation of such crossbar circuitry," Patent Number 8,255,610, issued August 28, 2012
33. "Crossbar circuitry and method of operation of such crossbar," Patent Number 8,230,152, issued July 24, 2012
34. "Single Event Upset Error Detection Within an Integrated Circuit," Patent Number 8,185,812, issued May 22, 2012
35. "Error Recovery Within Processing Stages of an Integrated Circuit," Patent Number 8,185,786, issued May 22, 2012
36. "Memory Cell Structure, a Memory Device Employing Such a Memo," Patent Number 8,107,290, issued January 31, 2012
37. "Crossbar Circuitry and Method of Operation of Such Crossbar" Patent Number 8,108,585, issued on January 31, 2012
38. "Error Detection in Precharged Logic," Patent Number 8,103,922, issued on January 24, 2012
39. "Error Detection in Precharged Logic," Patent Number 8,006,147, issued on August 23, 2011
40. "Isolation Circuitry and Method for Hiding a Power Consumption Characteristic of an Associated Processing Circuit," Patent Number 7,880,339, issued on February 1, 2011
41. "Integrated Circuit Memory Access Mechanisms," Patent Number 7,864,562, issued on January 4, 2011
42. "On-chip Power Supply Voltage Regulation," Patent Number 7,839,129, issued on November 23, 2010
43. "Integrated Circuit with Error Correction Mechanisms to Offset Narrow Tolerancing," Patent Number 7,701,204, issued on April 20, 2010
44. "Error Detection and Recovery Within Processing Stages of an Integrated Circuit," Patent Number 7,650,551, issued on January 19, 2010
45. "Data Processor Memory Circuit," Patent Number 7,533, 226, issued on May 12, 2009
46. "Systematic and Random Error Detection and Recovery Within Processing Stages of An Integrated Circuit," Patent Number 7,337,356, issued on February 26, 2008
47. "Error Recovery Within Processing Stages of an Integrated Circuit," Patent Number 7,320,091, issued on January 15, 2008
48. "Data Retention Latch Provision Within Integrated Circuits," Patent Number 7,310,755, issued on December 18, 2007
49. "Error detection and recovery within processing stages of an integrated circuit," Patent Number 7,278,080, issued on October 2, 2007
50. "Address Decoding," Patent Number 7,263,015, issued on August 28, 2007

51. "Systematic and random error detection and recovery within processing stages of an integrated circuit," Patent Number 7,162,661, issued on January 9, 2007
52. "Methods for analyzing integrated circuits and apparatus therefor," Patent Number 7,149,674, issued on December 12, 2006
53. "Noise analysis for an integrated circuit model," Patent Number 7,093,223, issued on August 15, 2006
54. "Memory System having Fast and Slow Data Reading Mechanisms," Patent Number 7,072,229, issued on July 4, 2006
55. "Data Processor Memory Circuit," Patent Number 7,055,007, issued on May 30, 2006
56. "Memory System Having Fast and Slow Data Reading Mechanisms," Patent Number 6,944,067, issued on September 13, 2005
57. "Actively-Shielded Signal Wires," Patent Number 6,919,619, issued on July 19, 2005
58. "Method and Apparatus for Controlling Current Demand in an Integrated Circuit", Patent Number 6,819,538, issued on November 16, 2004
59. "Cross Coupling Delay Characterization for Integrated Circuits," Patent Number 6,799,153, issued on September 28, 2004
60. "Iterative, Noise-Sensitive Method of Routing Semiconductor Nets," Patent Number 6,480,998, issued on November 12, 2002
61. "Waveform Manipulation in Time Warp Simulation," Patent Number 6,195,628, issued on February 27, 2001
62. "Optimizing Combinational Circuit Layout through Iterative Restructuring," Patent Number 6,074,429, issued on June 13, 2000
63. "In-Transit Message Detection for Global Virtual Time Calculation in Parallel Time Warp Simulation," Patent Number 5,956,261, issued on September 21, 1999
64. "Method for Optimizing Element Sizes in a Semiconductor Device," Patent Number 5,903,471, issued on May 11, 1999
65. "Updating Hierarchical DAG Representations through a Bottom up Method," Patent Number 5,790,416, issued on August 4, 1998
66. "Complementary Network Reduction for Load Modeling," Patent Number 5,790,415, issued on August 4, 1998
67. "Simulation Corrected Sensitivity," Patent Number 5,787,008, issued on July 28, 1998
68. "Accurate Delay Prediction Based on Multi-Model Analysis," Patent Number 5,751,593, issued on May 12, 1998
69. "Apparatus and Method for the Automatic Determination of a Standard Library Height within an Integrated Circuit Design," Patent Number 5,737,236, issued April 7, 1998
70. "Integrated Circuit Design and Manufacturing Method and an Apparatus for Designing an Integrated Circuit in Accordance with the Method," Patent Number 5,689,432, issued on November 18, 1997
71. "Method and Apparatus for Designing an Integrated Circuit," Patent Number 5,666,288, issued on September 9, 1997
72. "Logic Gate Size Optimization Process for an Integrated Circuit Whereby Circuit Speed is Improved While Circuit Areas is Optimized," Patent Number 5,619,418, issued on April 8, 1997

73. "Message Sequence Number Control in a Virtual Time System," Patent Number 5,617,561, issued on April 1, 1997

VI Scholarly Addresses

A. Conference Keynote Addresses and Invited Presentations

1. Invited presentation, “The Internet of Tiny Things - IoT²: Challenges and Opportunities in mm-Scale Computing,” ECE Distinguished Lecture Series, George Washington University, December 2018
2. Plenary Keynote Address, “Unlocking New IoT Application Domains Through Ultra-Low Power mm-Scale Sensor Node Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), July 2018
3. Invited presentation, “Low-Power Circuit Techniques for IoT Energy Harvesting,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2016
4. Plenary Keynote Address, “From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design,” IEEE Subthreshold Microelectronics Conference (SubVt), October 2012
5. Invited presentation, “Adaptive Sensing and Design for Reliability,” IEEE International Reliability Physics Symposium, May 2010
6. Invited presentation, “Architectural Techniques for Self-Adaptive Computing,” IEEE International Solid-State Circuits Conference (ISSCC), February 2007
7. Invited presentation, “Energy Optimality and Variability in Subthreshold Design,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
8. Invited presentation, “Energy Efficient Design for Subthreshold Supply Voltage Operation,” IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
9. Invited presentation, “Extended Dynamic Voltage Scaling for Low Power Design,” IEEE International SOC Conference, September 2004
10. Invited presentation, “Signal Integrity Issues in High Performance Design,” IEEE International Workshop-Power and Timing Modeling, Optimization and Simulation (Patmos), Switzerland, September 2001
11. Invited presentation, “Inductance 101: Analysis and Design,” ACM/IEEE Design Automation Conference, June 2001
12. Invited presentation, “Inductance Extraction and Modeling,” ACM/IEEE Great Lakes Symposium on VLSI Design (GLSVLSI), March 2000
13. Keynote address, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), Italy, March 1999
14. Keynote address, “Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 1998

VII Professional Activities

A. Professional Societies

- Fellow of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

B. Editor, Co-Editor, and Associate Editor Positions

- Associate editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, December 2003 - January 2006
- Co-guest editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Design and Test of Computers*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Transactions on Very Large Scale Integration Systems (T-VLSI)*, special issue on Low Power Electronics, 1999

C. Conference and Workshop Organization

- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2018 - current
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2006 – 2009
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2004 - 2007
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999 - 2006
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1997, 2005 – 2006
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2002 - 2004
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2001 - 2003
- Panel Chair, ACM/IEEE Design Automation Conference (DAC), 2003
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2001 - 2002
- General Co-Chair, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2000
- Co-Chair, technical program committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999

D. Consulting & Advisory Boards

- **Technical Consulting and Advisory boards**
 - Member of University of Illinois at Urbana – Champaign Advisory Panel 2013 – current

- Gear Inc. 2013 – 2015
- Apache Design Automation – member of advisory board
- Nascentric, Technical Consulting, 2008
- CLK Design Automation (CLK-DA), Technical Consulting, 2005 – 2008
- **Legal Consulting**
 - Parkins Coie LLP, 2014 – 2015
 - WilmerHale, 2012 – 2013
 - Alston & Bird, 2010 – 2011
 - Weil, Gotshal & Manges, 2008 – 2010
 - WilmerHale, 2007
- F. Refereeing and Reviewing**
 - NSF, SRC, Natural Science and Engineering Research Council of Canada (NSERC)
 - IEEE, IEEE T-VLSI, ACM TODAES, IEEE D&T
 - DAC, ICCAD, ISLPED, ICCD, ISPD, TAU, DATE, ISCAS, ISQED, PACS