Analysis of Noise Avoidance Techniques in DSM Interconnects using a Complete Crosstalk Noise Model

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Abstract

Noise estimation and avoidance are becoming critical, 'must have' capabilities in today's high performance IC design. An accurate yet efficient crosstalk noise model which contains as many driver/interconnect parameters as possible, is neccesary for any sensitivity based noise avoidance approach. In this paper, we present a complete analytical crosstalk noise model which incorporates all physical properties including victim and aggressor drivers, distributed RC characteristics of interconnects and coupling locations in both victim and aggressor lines. We present closed-form analytical expressions for peak noise and noise width as well as sensitivities to all model parameters. We then use these model parameter sensitivities to analyze and evaluate various noise avoidance techniques such as driver sizing, wire sizing, wire spacing and layer assignment. Both our model and noise avoidance evaluations are verified using realistic circuits in 0.13μ *technology. We also present effectiveness of discussed noise avoidance techniques on a high performance microprocessor core.*

1. Introduction

Coupling capacitance between neighboring nets is a dominant component in today's deep submicron designs as taller and narrower lines are being laid out closer to each other [2]. This trend is causing the ratio of crosstalk capacitance to the total capacitance of a wire to increase. On top of these interconnect related trends, more aggressive and less noise immune circuit structures such as dynamic logic are being employed more commonly due to performance requirements. As a result, a significant crosstalk noise problem exists in today's high performance designs. The net on which noise is being induced is called the *victim* net whereas the net that induces this noise is called the *aggressor* net. Crosstalk noise not only leads to modified delays [5, 10] but also to potential logic malfunctions [1, 9].

To be able to deal with the challenges brought by this recently emerging phenomenon, techniques and tools to estimate and avoid crosstalk noise problems should be incorporated into the IC design cycle from the early stages. Any such tool requires fast yet accurate crosstalk noise models both to estimate noise and also to see the effects of various interconnect and driver parameters on noise.

Several papers, which propose crosstalk models, can be found in recent literature. In [8], telegraph equations are solved directly to find a set of analytical formulae for peak noise in capacitively coupled bus lines. [12] derives bounds for crosstalk noise using a lumped model but assuming a step input for aggressor driver. The peak noise expression in [12] is extended by [11, 6] to consider a saturated ramp input and a π circuit to represent the interconnect. These models fail to represent the distributed nature of the interconnect. In [4], an Elmore delay like peak noise model is obtained for general RC trees but it assumes an infinite ramp input. This assumption causes the model to significantly overestimate peak noise, especially for small aggressor slews, which is very likely to occur in today's deep submicron designs. Devgan's metric has been improved in [7]. In another recent work [3], an improved 2π model is introduced which takes into account the coupling location at victim net and distributed RC characteristics for victim net. Authors derive closed-form expressions for peak noise and noise width and demonstrate that the accuracy of the 2π model is superior to the models proposed by Devgan [4] and Vittal [11].

In this paper, we construct a 4π model based on the approach in [3]. Our model overcomes the lack of aggressor driver and interconnect representation in [3], where the victim line has been modeled by a 2π circuit and aggressor voltage at coupling node is assumed to be available. As stated by the authors, aggressor net RC characteristics and its driver/load information are incorporated in the slew t_r at the coupling location. But this kind of an approach requires the use of some pre-processing on the aggressor line, such as employing slew models or getting this information from timing analysis tools. One other drawback of representing the aggressor line only with the slew t_r at coupling location is that such a model does not let one analytically estimate the effects of aggressor driver/load and interconnect parameters on crosstalk noise. A complete crosstalk noise model should

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be composed of all the parameters that can be varied for noise avoidance purposes. Our model incorporates the aggressor driver, load and distributed RC characteristics for aggressor line. Using our model, coupling location can be modeled not only with the location on victim line (near-victim-driver or near-victim-receiver) but also with the location on aggressor line (near-aggressor-driver or near-aggressor-receiver). We will present closed-form expressions for both peak noise and noise width.

In the second part of the paper, we will define and investigate various noise avoidance techniques and their effectiveness, using the analytical sensitivity expressions obtained from our model. Sensitivity expressions with respect to all model parameters will be derived and presented. The validity of these observations will be evaluated using a practical test case in 0.13μ technology. We will also present the effectiveness of discussed noise avoidance techniques on a high performance microprocessor core.

The paper is organized as follows. Section 2 presents our model and its analytical solutions for peak noise and noise width. We will also extend our model to general RC trees and show accuracy with respect to SPICE simulations in this section. Section 3 defines various noise avoidance techniques and their physical interpretations. In this section, we will evaluate these noise avoidance techniques using parameter sensitivities derived from our analyical model. In section 4, we verify these evaluations using a practical test case in 0.13μ technology and present effectiveness of these techniques on a microprocessor core. Section 5 contains some closing remarks.

2. A Complete Crosstalk Noise Model

In this section, we present our crosstalk noise model and derive analytical formulas for its time-domain waveform, peak noise and noise width. We then extend our model to handle general RC trees and verify the derived analytical equations against SPICE simulations.

A general case for two coupled lines is shown in Figure 1. Both aggressor and victim lines are divided into 3 regions: interconnect segment before coupling location, coupling location and interconnect segment after coupling location. These regions of aggressor and victim lines are represented by L_{al}, L_c, L_{ar}, L_{vl} and L_{vr} as seen in the figure.

We propose the linear model shown in Figure 2 to compute crosstalk noise at the receiver of victim net. Victim driver is modeled by effective holding resistance R_h whereas aggressor driver is modeled by an effective Thevennin model consisting of a saturated ramp voltage source with a slew rate of t_r and the Thevennin resistance R_{th}. Other components of our model are computed based on the technology and geometrical information obtained from Figure 1. Coupling node (node 2 in aggressor net and node 5 in victim net) is defined to be the middle of coupling location for both nets, i.e. $L_{al} + L_c/2$ away from aggressor driver and $L_{vl} + L_c/2$

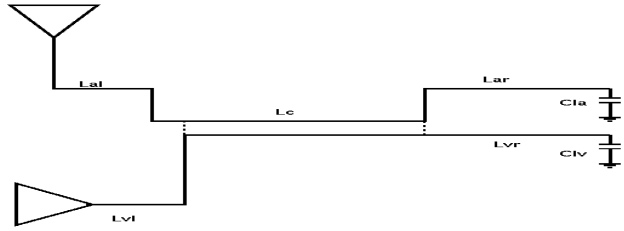

Figure 1. A general case for two coupled nets

away from the victim driver. For the aggressor net, let the upstream and downstream resistance-capacitance at node 2 be $R_{a1} - C_{au}$ and $R_{a2} - C_{ad}$ respectively. Then, $C_{a1} = C_{au}/2$, $C_{a2} = (C_{au} + C_{ad})/2$ and $C_{a3} = C_{ad}/2 + C_{la}$. Similarly for the victim net, let the upstream and downstream resistance-capacitance pair at node 5 be $R_{v1} - C_{vu}$ and $R_{v2} - C_{vd}$ respectively. Then, $C_{v1} = C_{vu}/2$, $C_{v2} = (C_{vu} + C_{vd})/2$ and $C_{v3} = C_{vd}/2 + C_{lv}$.

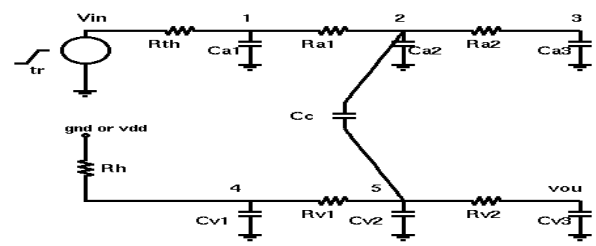

Figure 2. Linear crosstalk noise model

To simplify the analytical calculation of transfer function $H(s)$ from V_{in} to V_{out}, we initially decouple the aggressor line from victim line (Figure 3 (a)), and compute the transfer function from V_{in} to V_2. We then apply $V_2(s)$ to the victim line as seen in Figure 3 (b). This assumption is valid when victim line is not loading aggressor line at node 2 significantly. Introduced error will be presented at the end of this section. From Figure 3(a),

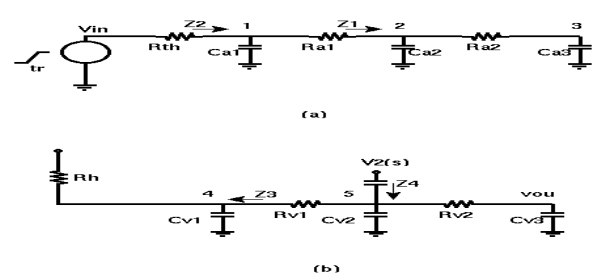

Figure 3. Decoupled model to calculate transfer function

$$\frac{1}{Z_1} = sC_{a2} + \frac{1}{R_{a2} + \frac{1}{sC_{a3}}} \quad (1)$$

and

$$\frac{1}{Z_2} = sC_{a1} + \frac{1}{R_{a1} + Z_1} \quad (2)$$

We have,

$$\begin{aligned} V_1(s) &= V_{in}(s)\frac{Z_2}{R_{th} + Z_2} \\ V_2(s) &= V_1(s)\frac{Z_1}{R_{a1} + Z_1} \end{aligned} \quad (3)$$

and thus,

$$V_2(s) = V_{in}(s)\frac{Z_2}{R_{th} + Z_2}\frac{Z_1}{R_{a1} + Z_1} \quad (4)$$

When we then look at the victim line (Figure 3(b)),

$$\frac{1}{Z_3} = \frac{1}{R_h} + sC_{v1} \quad (5)$$

and

$$\frac{1}{Z_4} = \frac{1}{Z_3 + R_{v1}} + sC_{v2} + \frac{1}{R_{v2} + \frac{1}{sC_{v3}}} \quad (6)$$

We have,

$$V_5(s) = \frac{Z_4}{Z_4 + \frac{1}{sC_c}}V_2(s) \quad (7)$$

and

$$V_{out}(s) = V_5(s)\frac{\frac{1}{sC_{v3}}}{R_{v2} + \frac{1}{sC_{v3}}} \quad (8)$$

Finally, putting it all together,

$$V_{out}(s) = \frac{Z_4}{Z_4 + \frac{1}{sC_c}}\frac{\frac{1}{sC_{v3}}}{R_{v2} + \frac{1}{sC_{v3}}}\frac{Z_2}{R_{th} + Z_2}\frac{Z_1}{R_{a1} + Z_1}V_{in}(s) \quad (9)$$

Equation (9) is the transfer function $H(s)$ from V_{in} to V_{out} and can be written as:

$$H(s) = \frac{a_5 s^5 + \ldots + a_1 s + a_0}{s^8 + b_7 s^7 + \ldots + b_2 s^2 + b_1 s + b_0} \quad (10)$$

The normalized saturated ramp input source v_{in} in time domain is

$$v_{in}(t) = \begin{cases} t/t_r & t \le t_r \\ 1 & t > t_r \end{cases} \quad (11)$$

with a Laplace transform of

$$V_{in}(s) = \frac{1 - e^{-st_r}}{t_r s^2} \quad (12)$$

To find the time-domain waveform using our model, one can transform $H(s)$ to pole/residue form using standard mathematical techniques and thus obtain

$$H(s) = \sum_{i=1}^{8} \frac{r_i}{s - p_i}. \quad (13)$$

Then for each pole/residue pair, time-domain voltage waveform v_{out_i} can be found by taking the inverse Laplace transform of $\frac{r_i}{s-p_i}V_{in}(s)$.:

$$v_{out_i}(t) = \begin{cases} -\frac{r_i(1+p_i t)}{t_r p_i^2} + \frac{r_i e^{p_i t}}{t_r p_i^2} & t \le t_r \\ -\frac{r_i e^{p_i(t-t_r)}}{t_r p_i^2} + \frac{r_i e^{p_i t}}{t_r p_i^2} - \frac{r_i}{p_i} & t > t_r \end{cases} \quad (14)$$

As a result, crosstalk noise time-domain waveform is the summation of the voltages from each pole/residue pair in the transfer function $H(s)$. In this work, we will not be using the time-domain noise waveform derived above explicitly. Our goal is to be able to obtain simple analytical expressions for important design metrics such as peak noise and noise width. Such analytical expressions will let us observe the effects of various interconnect and driver parameters on crosstalk noise and eventually form the basis of evaluating several noise avoidance techniques.

Transfer function $H(s)$ in Equation(10) can be simplified using dominant-pole approximation method as in [3]. In this case, the output voltage in Laplace domain reduces to

$$V_{out}(s) \approx \frac{a_1 s + a_0}{b_1 s + b_0}V_{in}(s) = \frac{t_x(1 - e^{-t_r s})}{t_r s(t_v s + 1)} \quad (15)$$

where the coefficients are

$$t_x = (R_h + R_{v1})C_c \quad (16)$$

$$\begin{aligned} t_v = \; & (R_h + R_{v1})(C_c + C_{v2} + C_{v3}) + (R_{v2}C_{v3} + R_h C_{v1}) + \\ & C_{a1}R_{th} + C_{a2}(2R_{a1} + R_{th}) + \\ & C_{a3}(2R_{a1} + 2R_{a2} + R_{th}) \end{aligned} \quad (17)$$

It can be seen that t_x represents the RC delay term for upstream resistance of the victim line due to C_c. On the other hand, t_v in Equation(17) is composed of two parts. First line represents the Elmore delay of the victim line, wheras the rest is due to the aggressor line parameters.

Inverse Laplace transform of Equation(15) gives the following time-domain waveform.

$$v_{out}(t) = \begin{cases} \frac{t_x}{t_r}(1 - e^{-t/t_v}) & t \le t_r \\ \frac{t_x}{t_r}(e^{-(t-t_r)/t_v} - e^{-t/t_v}) & t > t_r \end{cases} \quad (18)$$

We can see that $\delta v_{out}/\delta t$ when $t \le t_r$ is always positive and $\delta v_{out}/\delta t$ when $t > t_r$ is always negative. So the peak noise is $v_{out}(t_r)$.

$$v_{peak} = \frac{t_x}{t_r}(1 - e^{t_r/t_v}) \quad (19)$$

Peak noise metric can be used to decide whether a net has sufficient noise induced on it, based on some global threshold peak noise. However in practice, gates have different susceptibilities to noise. Thus, one should set a noise threshold at the output of net's receiver to take into account the reduction of a noise pulse as it propagates through the receiver

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gate. This makes noise width at receiver input another important metric. In recent advanced noise analysis tools [1], this phenomenon is represented by the concept of noise rejection curves as seen in Figure 4. Only if the noise-peak/noise-width pair at the receiver input is in the failing region of noise rejection curve, then this net is flagged as failing. This pre-characterization method is also compliant with standard cell ASIC flow. From our model, we compute noise width as the

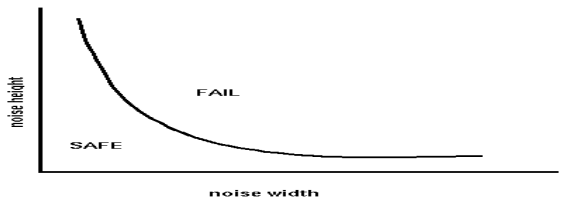

Figure 4. A sample Noise Rejection Curve

time interval during which noise pulse is greater than or equal to a certain threshold voltage v_t. If we choose this value to be $v_{peak}/2$ to simplify the analytical t_{width} expression, we get

$$t_{width} = t_r + t_v ln\left(\frac{1-e^{-2t_r/t_v}}{1-e^{-t_r/t_v}}\right) \tag{20}$$

The extension of our model to general RC trees naturally follows our model generation for simple lines. The upstream and downstream resistances stay the same, whereas the lumped branch capacitances in aggressor and victim trees are added to model capacitances as follows. If a victim (aggressor) branch with a lumped capacitance of C_b is between the victim (aggressor) driver and coupling center, with α percent of the corresponding length to its upstream and β percent of the corresponding length to its downstream ($\alpha + \beta = 100\%$), then $\alpha\%$ of C_b is added to C_{v1} (C_{a1}) and $\beta\%$ of C_b is added to C_{v2} (C_{a2}). Same kind of argument also applies if a branch is between the receiver and coupling center.

We have tested our model extensively and verified its accuracy compared to SPICE simulations. To test a wide range of practical scenarios, we generated 10000 random circuits and ran our model as well as SPICE, using realistic parameters in a 0.13μ technology. In the test circuits the parameter ranges were as follows. $R_h : 10-1500\Omega$, $R_{th} : 10-1500\Omega$, load capacitances for aggressor and victim lines: $5-50fF$, victim and aggressor lengths: $10-2000\mu$, coupling length and coupling locations in aggressor and victim lines $10\mu-$ maximum length, $t_r : 10-500ps$. Figure 5 shows the percentage errors (v_{peak} model - v_{peak} SPICE) for these 10000 test circuits. Average error is 10% and 85% of the test cases are within 20% error. The tendency of our model to over estimate peak noise in some cases is due to our decoupling approach to calculate $V_2(s)$ and then use this to find the transfer function $H(s)$. This assumption loses its validity as victim line becomes a significant load on node 2. Noise width errors are also similar, our model with a tendency to underestimate noise width in some cases. The source of width underestimation is again not taking victim line as a load on the aggressor line when $V_2(s)$ is calculated. Nevertheless, these are acceptable results for a model that exposes as many driver/interconnect paramerets as possible.

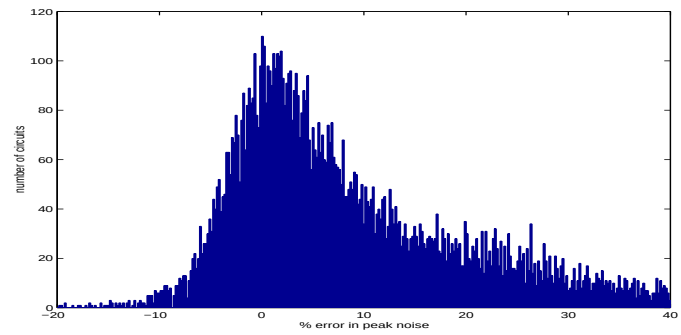

Figure 5.

3. Noise Avoidance Techniques

In this section, we will investigate several noise avoidance techniques and evaluate their effects using our model.

3.1. Driver Sizing

We will look at driver sizing both from the point of view of victim driver sizing and aggressor driver sizing. Intuitively, if a victim driver is sized up, its effective conductance increases thus it becomes stronger to hold a net at a steady voltage (v_{dd} or ground). On the other hand, if an aggressor driver is sized down, its effective conductance decreases thus it cannot transition as fast and as a result noise amount that it can induce on a victim net decreases. Using our model, we have calculated the sensitivity of peak noise to R_h and R_{th} which represent victim and aggressor driver sizes, respectively.

$$\frac{\delta v_{peak}}{\delta R_h} = \frac{C_c}{t_r}(1-e^{-t_r/t_v}) - (R_h+R_{v1})\frac{C_c(C_c+C_{v1}+C_{v2}+C_{v3})}{t_v^2}e^{-t_r/t_v} \tag{21}$$

$$\frac{\delta v_{peak}}{\delta R_{th}} = \frac{-(R_h+R_{v1})C_c(C_{a1}+C_{a2}+C_{a3})}{t_v^2}e^{-t_r/t_v} \tag{22}$$

Since Equation (22) is always negative, sizing down the aggressor driver (i.e., sizing up R_{th}) will always reduce peak noise. But how effective a reduction it will be, depends on the parameters of Equation (22). Increasing R_{th} will be more effective on noise reduction if the numerator of Equation (22) is greater than its denominator. If the equation parameters are carefully observed, this mathematical condition translates

to the following circuit condition. Noise reduction effect of increasing R_{th} is more, when we have a strong aggressor (strong aggressor driver, wide/short aggressor line).

The effects of sizing up victim driver (i.e. sizing down R_h) is more complicated. In terms of peak noise reduction, victim driver sizing becomes a more effective noise avoidance tool as the RC time costant of victim line decreases. Figure 6(a) shows the effects of victim driver sizing on a short victim line. Note that peak noise voltage is reduced by $75mV/38.5\%$ whereas noise width is reduced by $22ps/9.6\%$ when victim driver size is doubled. As RC time constant of victim line increases, victim driver sizing becomess less effective in terms of peak noise reduction but it is important to notice the effects on noise width. As seen in Figure 6(b), victim driver sizing on a long victim line reduces noise width by $550ps/24\%$ while peak noise is reduced by $0.4mV/1\%$ when victim driver size is doubled. One other important observation about victim driver sizing is the diminishing returns effect. Figure 7 shows change in $\delta v_{peak}/\delta(1/R_h)$ as victim driver is sized up, for a range of victim line lengths. As can be seen, the effect of driver sizing diminishes as victim driver is sized up. A driver sizing tool should take this effect into account to be able to steer away from non-optimal sizes and to make sure that the area trade-off is worth while.

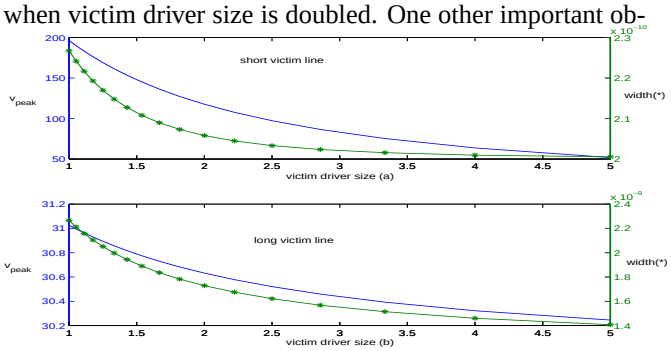

Figure 6. Sensitivity of victim driver sizing effects to victim line properties

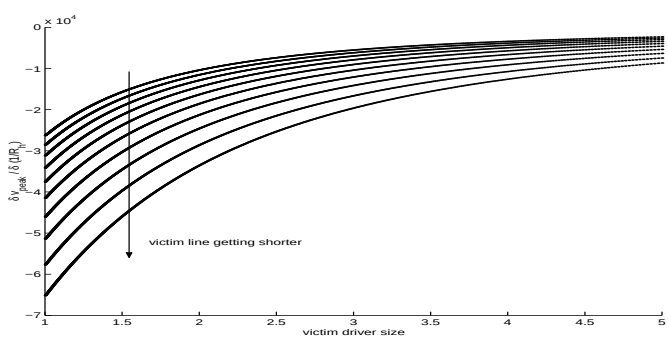

Figure 7. Diminishing returns effect in victim driver sizing

3.2. Wire Spacing

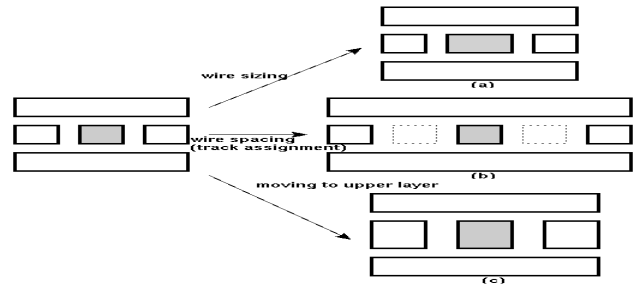

Figure 8. Crosssection of victim line and surroundings

For a wire of fixed width, its coupling capacitance decreases while its ground capacitance increases, as its spacing to a neighbor wire increases. The decreasing of coupling capacitance is easly explained by the inverse relation between capacitance and distance. Increasing of ground capacitance is due to the fact that as spacing between two wires increases, some of the field lines contributing to coupling capacitance fail reaching the neighbor wire and start contributing to ground capacitance (Figure 8(b)). From our model,

$$\frac{\delta v_{peak}}{\delta C_c} = (\frac{R_h + R_{v1}}{t_r})(1-e^{-t_r/t_v}) - \frac{(R_h + R_{v2})^2 C_c}{t_v^2} e^{-t_r/t_v} \quad (23)$$

$$\frac{\delta v_{peak}}{\delta C_{v1}} = \frac{-(R_h + R_{v1}) C_c R_h}{t_v^2} e^{-t_r/t_v} \quad (24)$$

$$\frac{\delta v_{peak}}{\delta C_{v2}} = \frac{-(R_h + R_{v1})^2 C_c}{t_v^2} e^{-t_r/t_v} \quad (25)$$

$$\frac{\delta v_{peak}}{\delta C_{v3}} = \frac{-(R_h + R_{v1}) C_c (R_h + R_{v1} + R_{v2})}{t_v^2} e^{-t_r/t_v} \quad (26)$$

$$\frac{\delta v_{peak}}{\delta C_{a1}} = \frac{-(R_h + R_{v1}) C_c R_{th}}{t_v^2} e^{-t_r/t_v} \quad (27)$$

$$\frac{\delta v_{peak}}{\delta C_{a2}} = \frac{-(R_h + R_{v1}) C_c (2R_{a1} + R_{th})}{t_v^2} e^{-t_r/t_v} \quad (28)$$

$$\frac{\delta v_{peak}}{\delta C_{a3}} = \frac{-(R_h + R_{v1}) C_c (2R_{a1} + 2R_{a2} + R_{th})}{t_v^2} e^{-t_r/t_v} \quad (29)$$

From Equation (23), $\delta v_{peak}/\delta C_c$ is positive but diminishes when $t_v >> t_r$ in which case reduction in coupling capacitance doesn't help peak noise reduction. Equations (24,25,26,27,28,29) show that an increase in the ground caps of both victim and aggressor lines help reduce noise on the victim net. Their relative effectivennesses are as follows.

$$\frac{\delta v_{peak}}{\delta C_{v3}} < \frac{\delta v_{peak}}{\delta C_{v2}} < \frac{\delta v_{peak}}{\delta C_{v1}} < 0 \quad (30)$$

$$\frac{\delta v_{peak}}{\delta C_{a3}} < \frac{\delta v_{peak}}{\delta C_{a2}} < \frac{\delta v_{peak}}{\delta C_{a1}} < 0 \quad (31)$$

As can be seen from (30 - 31), for the same amount of increase in ground capacitance, peak noise reduction is most effected from near sink capacitances in both victim and aggressor lines.

3.3. Wire Sizing

As a wire's width is increased, its resistance decreases and its ground capacitance increases (Figure 8(a)). We have looked at the effects of ground capacitance increase in previous subsection. If we look at how noise peak is affected by changes in interconnect resistances, we get the following sensitivities from our model.

$$\frac{\delta v_{peak}}{\delta R_{v1}} = \frac{C_c}{t_r}(1 - e^{-t_r/t_v}) - (R_h + R_{v1})\frac{C_c(C_c + C_{v2} + C_{v3})}{t_v^2}e^{-t_r/t_v} \quad (32)$$

$$\frac{\delta v_{peak}}{\delta R_{v2}} = \frac{-(R_h + R_{v1})C_c C_{v3}}{t_v^2}e^{-t_r/t_v} \quad (33)$$

$$\frac{\delta v_{peak}}{\delta R_{a1}} = \frac{-2(R_h + R_{v1})C_c(C_{a2} + C_{a3})}{t_v^2}e^{-t_r/t_v} \quad (34)$$

$$\frac{\delta v_{peak}}{\delta R_{a2}} = \frac{-2(R_h + R_{v1})C_c C_{a3}}{t_v^2}e^{-t_r/t_v} \quad (35)$$

Equation (32) shows that the effect of R_{v1} on noise reduction is very similar to that of R_h. On the other hand, from Equations (33, 34, 35), the effects of R_{v2}, R_{a1} and R_{a2} are opposite. Peak noise increases as these resistances are decreased. As a result, when a victim wire's width is increased, the change in peak noise depends on Equations (24, 25, 26, 32, 33). Equations (32 and 33) show the importance of coupling location on how effective wire sizing will be. If the coupling location is close to victim driver, Equation(33) will be more effective than Equation (32) and thus effect of wire sizing on noise reduction will diminish. Wire sizing will be most effective when coupling location is close to victim receiver. On the other hand, the effect of increasing an aggressor wire's width depends on relative magnitudes of $\delta v_{peak}/\delta C_{ai}$ and $\delta v_{peak}/\delta R_{ai}$. By looking at Equations (27, 28, 29, 34, 35), it can be seen that the capacitance sensitivities are greater in magnitude than resistance sensitivities. Thus if R_{ai} decrease as much as C_{ai} increase as a result of width increase, this will help reduce noise on the victim receiver input.

3.4. Coupling Location

One other parameter that changes the values of our model wire resistance and capacitance values is coupling location. As coupling location on victim line gets closer to the sink, R_{v2} decreases as R_{v1} increases. Both of these cause noise peak to increase at victim receiver as seen in Equations (32, 33). This also causes C_{v1} to increase and C_{v3} to decrease. Since $|\delta v_{peak}/\delta C_{v3}| > |\delta v_{peak}/\delta C_{v1}|$, this trend will also cause noise to increase. As a result, noise at victim receiver input increases as coupling location on victim line gets closer to it. On the other hand, as coupling location on aggressor line changes, the effect in noise depends on the relative magnitudes of Equations (34, 35, 27, 28). As these sensitivities work against each other, effects on noise at receiver input will vary based on the particular situation.

3.5. Layer and Track Assignment

A practical noise avoidance tool can use layer and track assignment directives for noise avoidance purposes. Different track assignments, i.e. single spacing, double spacing etc., will translate as changes in coupling capacitance C_c and ground capacitances as explained in subsection 3.2. Figure 8(b) shows the case of double track assignment. Layer assignments on the other hand, will lead to changes in all interconnect parameters. Minimum width and spacing of a wire may change as it is moved to a different metal layer. In today's interconnect technologies, moving a net to an upper metal, close to last metal, usually helps in terms of noise as wire width increases. But one should be careful since the metals also tend to get thicker in upper layers (Figure 8(c)). This causes an increase in coupling capacitance which may overcome the decrease in resistance and increase in ground capacitance due to increased width. Particular technology parameters should be investigated to make informed decisions. As demonstrated, our model can be used to evaluate various options once these parameters are extracted.

4. Results

In this section, we compare the sensitivity of noise peak with respect to all model parameters and verify our observations on a practical circuit. We then investigate, on a high performance microprocessor core, the effectiveness of discussed noise avoidance techniques.

We generated 100000 random circuits using the parameter ranges presented in Section 2 and looked at the sensitivity of noise peak to each model parameter. Figure 9 shows the average of these sensitivities for 13 model parameters, calculated from 100000 circuits. The units are mV/fF for capacitances and mV/Ω for resistances. The second plot in Figure 9 is the same as the first one with C_c sensitivity suppressed to be able to see others more clearly. .

4.1. A Sample Circuit

In this subsection, we will look at effects of driver/interconnect parameters on a practical test case in 0.13μ technology to verify our model sensitivity observations in Figure 9. In our test case, victim driver is a 2

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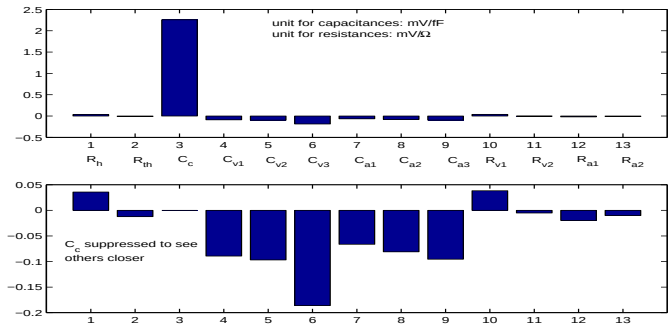

Figure 9. Sensitivity of peak noise on model parameters

input NOR gate which has 9 versions in a library. Victim interconnect is a general RC tree with a silicon length of 1100μ. Aggressor driver is a strong inverter whereas the aggressor interconnect is short and minimum width. Table 1 presents the 9 versions of NOR-2 gate in the library along with n-type transistor sizes and effective holding resistances for high to low transition on the aggressor net. Please refer to [1] for a detailed explanation of how holding resistances are calculated. We also list noise height and noise width.

Power	n-mos size (normalized μm)	holding R (Ω)	height (mV)	width (ps)
e	1	2475.18	281.03	3122.91
g	1.36	1732.51	275.43	2345.03
h	1.99	1221.86	266.90	1799.80
i	2.79	872.81	257.27	1392.51
k	3.98	615.10	245.37	1108.61
l	5.58	439.24	230.93	923.15
o	7.95	309.28	218.95	775.04
p	11.95	211.55	208.35	657.54
r	16.91	129.18	191.27	572.18

Table 1. Noise height and width for various powers of nor-2 gate

From Table 1, we can see that if we go from power e to power k (i.e. increase victim driver size approximately 4x), noise peak reduction is $35.66mV/13\%$ and width reduction is $2014.3ps/65\%$. Table 2 shows noise heights and widths for the same range of victim drivers but this time RC time constant of victim line is doubled.

By comparing tables 1 and 2, we can see the effects of driver sizing when the RC time constant of victim line increases. If we go from power e to power k again, noise peak reduction is $10.02mV/6\%$ and width reduction is $3554.12ps/67\%$. Although effect of driver sizing is reduced on noise height considerably, its effect on width reduction is quite strong as suggested earlier in section 3. One interesting observation in these results is that we do not see diminishing returns effect as victim driver is sized up. This is due to

Power	height (mV)	width (ps)
e	164.03	5320.35
g	162.62	3971.62
h	160.63	2957.23
i	152.97	2342.01
k	154.01	1766.22
l	145.22	1468.04
o	140.79	1205.36
p	140.20	977.16
r	133.54	819.58

Table 2. Noise height and width for various powers of nor-2 gate (RC time const doubled)

the fact that, pin capacitance of the driver is increasing as it is sized up. This is acting as added ground capacitance for victim line and thus compensating for the reduced effect of holding resistance.

We now evaluate how noise changes when interconnect parameters are varied. For this purpose we take NOR-2 gate, power k. Originally noise height is $245.37mV$. When we change coupling capacitance, ground capacitance and wire resistance by the same amount, we get the following results. If coupling capacitance is decreased by $60fF$, noise height is reduced to $133.12mV$ (by 46%). If the ground capacitance is increased by $60fF$, noise height is reduced to $226.66mV$ (by 8%). If the wire resistance is decreased by 60Ω, noise height is reduced to $244.20mV$. These results for a realistic test case are in compliance with our average model predictions on 100000 test circuits presented in Figure 9.

4.2. Noise Avoidance Techniques on a Microprocessor

After verifying the accuracy of our model sensitivities on a wide range of physical parameters, we will now present results on effectiveness of discussed noise avoidance techiques on a high performance microprocessor core. Table 3 shows how ground and coupling capacitances scale when we employ wire sizing, wire spacing (double track) and moving up to higher metal layer, based on a field simulator in a 0.13μ technology. We also present the effects of thick vs. not-thick upper metal layer. As can be seen in this particular technology, coupling capacitance increases when the upper metal layer is thick. Although metal width and spacing is increas-

Method	size	space	up (thick)	up (not-thick)
C_c	1	0.22	1.54	0.54
C_g	1.17	1.57	1.17	1.48

Table 3. Capacitance scales for noise avoidance techniques

ing when moved to upper layer, increase in thickness is more dominant. Also note that interconnect resistances scale down in the above techniques except for wire spacing. Resistance scales depend on sheet resistances and widths of metals. Figure 10 shows the average percentage noise reduction on the 48000 longer interconnects of a high performance microprocessor core, when various noise avoidance techniques are applied to all victim nets.

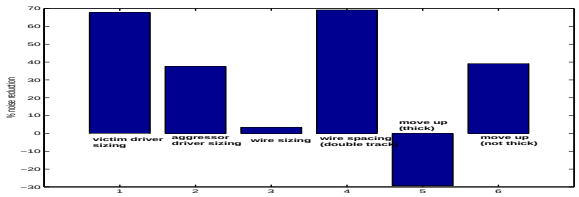

Figure 10. Average noise reduction on a microprocessor core

Note that in this experiment, victim driver sizing corresponds to sizing the victim driver by $4x$ and aggressor driver sizing corresponds to sizing the aggressor driver by $0.25x$. These are atainable numbers in a typical standard cell library. Although the effectiveness of a particular noise avoidance technique depends on the particular interconnect/driver characteristics of a net, few general remarks can be made based on our observations on this microprocessor core: Wire spacing is the most effective noise avoidance technique but also very costly. Victim driver sizing is quite effective in this example which shows us that most of the nets considered are satisfying the optimality condition discussed in Section 3. As discussed earlier, metal thickness plays a big role on the effectiveness of layer assignment. Moving a net to a thick layer, without employing any other noise avoidance technique, actually increases noise due to increased coupling capacitance. Sizing down the aggressor driver also reduced noise significantly hinting the initial strength of aggressor drivers. Wire sizing proved to be the least effective noise avoidance technique in this example. These observations show the relative effectivenesses of discussed noise avoidance techniques on a real microprocessor core. A good noise avoidance tool should be able to choose effective noise avoidance techniques based on the specific situation and combine various techniques to obtain effective results. Our model and sensitivity equations presented in this paper can serve as the driving engine of such a noise avoidance methodology.

5. Conclusion

In this paper, we presented a complete crosstalk noise model which incorporates all victim and aggressor driver/interconnect physical parameters including coupling locations on both victim and aggressor nets. We derived analytical expressions for the important metrics of crosstalk noise height and width using our model. The validity of these expressions against SPICE has been demonstrated. Compared to existing models, our model has a good trade-off between accuracy and completeness, having an average error of 10% with respect to SPICE while not failing to represent any important parameter. We then derived analytical expressions for sensitivity of noise to all model parameters and used these expressions to evaluate several noise avoidance techniques. Mathematical observations and experimental results presented based on our sensitivity equations provide a good understanding of effects of aggressor and victim driver/interconnect parameters on noise. We also presented relative effects of discussed noise avoidance techniques on a real microprocessor core.

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