A Library Compatible Driving Point Model for On-Chip RLC Interconnects

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ABSTRACT

This paper presents a new library compatible approach to gate-level timing characterization in the presence of RLC interconnect loads. We describe a two-ramp model based on transmission line theory that accurately predicts both the 50% delay and waveform shape (slew rate) at the driver output when inductive effects are significant. The approach does not rely on piecewise linear Thevenin voltage sources. It is compatible with existing library characterization methods and is computationally efficient. Results are compared with SPICE and demonstrate typical errors under 10% for both delay and slew rate.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Performance, Design

1. INTRODUCTION

With higher clocking frequencies, longer and wider global interconnects and faster signal rise times, on-chip inductive effects are becoming more significant in today's high-performance deep-submicron designs. These inductive effects are concerns for signal integrity and overall interconnect performance and must be accounted for in interconnect timing analysis.

Existing gate-level static timing analyzers break down the path delay into gate delay and interconnect delay. Gate delays are pre-characterized in terms of input transition time and output load capacitance using detailed circuit simulators such as SPICE. The inherent incompatibility that exists between pre-characterized look-up tables and RC/RLC loads is resolved by finding an effective capacitive loading. This requires synthesizing a reduced order driving point model, which is then mapped to an "*effective capacitance*" value. O'Brien and Savarino [9] synthesized a pi-model for RC loads by matching the first three moments of the driving point admittance and Pillage et al. [11] presented an effective capacitance model for this pi-load. It has been shown that, with the introduction of inductance, the pi model cannot be synthesized [6]. A ladder type model is presented in [6], which assures the realizability of a reduced order circuit by introducing a realizability parameter *k*. However, no physical explanation is given for *k* and also there is no approach to map this model to an effective capacitance.

Another issue with inductance is that the driver output waveform may be non-monotonic and exhibits inflection points. Traditionally, static timing analysis tools compute delay and rise time at the output of a gate and approximate it with a saturated ramp. This ramp is then used to derive the far end response of the interconnect. While this approach usually works well for RC lines, it fails for RLC lines because the output waveform of the driving gate cannot always be well modeled by a single ramp [7].

In this paper, these issues are addressed by proposing an approach, which computes the effective capacitance for RLC interconnects by using their driving point admittance moments. The idea of using driving point admittance moments was introduced in [1]. However, unlike their approach, our methodology is compatible with existing cell characterizations and does not require modeling of cells with piecewise linear Thevenin voltage sources. Also, our approach models the driver output waveform directly as compared to the approach in [1], which requires a SPICE or PRIMA run (with a piecewise linear Thevenin voltage and series resistance driving an RLC line) to compute the response at the driver output. We also show that with dominant inductive effects, a single ramp cannot model the entire driving point waveform accurately and at least two ramps should be computed to capture both the delay and slew. It must be noted here that with significant resistive shielding, even RC line cannot be modeled as single ramp and a gate resistor model is used to capture its long exponential tail [11]. However, the case with inductance is different because the output waveform of the driver exhibits a kink (and sometimes a flat plateau) due to transmission line effects. This kink, which causes a clear slope change, occurs in all inductively dominated lines and can be captured by proposed two-ramp model based on transmission line theory. We synthesize this two-ramp waveform by finding two effective capacitances. In the process, we propose a new method for evaluating the importance of on-chip inductance. Our method compares rise time at the driver output with the time of flight instead of simply taking the rise time at the input to the driver [5].

The paper is organized as follows. We begin by reviewing some basic properties of the inductive lines and the transmission line theory in the following section. Sections 3 and 4 present our modeling approach to capture the inductive waveforms at the

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driver output. Section 5 summarizes our modeling flow. Section 6 shows the experimental results and we conclude in section 7.

2. DRIVER OUTPUT WAVEFORM WITH INDUCTANCE

We know that with significant inductance, the driver output waveform is no longer smooth as in RC cases, exhibiting inflection points. Figure 1 shows the driver output waveforms of an RLC line driven by different sized inverters. The figure shows that the waveforms rise sharply to a voltage level and then flatten out, changing the slope of the transition.

This behavior of the waveforms can be explained by transmission line theory. We know that for fast drivers, transmission line effects become significant since the rise time of the signal is less than or comparable to the signal time of flight delay. The ratio of signal rise time to time of flight delay can be related to the ratio of the source resistance of the driver to the characteristic impedance of the line [2]. It is shown in [2] that when the source impedance of the driver is less than or comparable to the characteristic line impedance, reflections and other transmission line phenomena become important.

At the driver end the transmission line can be modeled as a source resistance in series with characteristic line impedance. In this case, we have a simple voltage divider and the ratio of the source resistance to the line impedance determines the size of the initial step generated on the line. It also determines the number of round trips required for the output to reach its final value. For weak drivers, the driver resistance is much larger than the line impedance, the initial step is small, and many trips are required. In fact, in this case the reflections may come back to the source end before the output has risen to the initial step. Thus the waveform resembles an RC line and the transmission line properties are hidden in the staircase-like waveform. However, for fast drivers, the initial step is high and a clear kink is seen in the waveform. For very fast drivers, the waveform rises to the initial step and flattens out while waiting for the reflection to come back. In these cases, a *plateau* is observed in the waveforms.

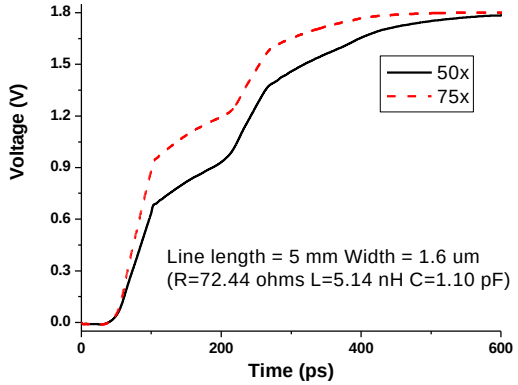

Figure 1. Driver output waveforms of a 5 mm RLC line driven by 50x and 75x inverters[1]

[1] Driver size 50x means width of NMOS in the inverter is 50 times the minimum width (=2*L_{min}=0.36μ). PMOS is twice as wide as NMOS.

From the above discussion, it is clear that modeling the driver output waveform as a single ramp or even an exponential wave can lead to serious errors in delay and slew prediction at the near as well as far end. When the wires are driven by strong buffers and the inductive effects are significant, the waveforms are non monotonic and exhibit inflection points and a better model of the driver output waveform is necessary for accurate timing analysis.

3. MODELING DRIVER OUTPUT WAVEFORM

Ideally, non-monotonic driver output waveforms should be modeled as multi-piecewise linear waveforms. In order to model the plateau accurately, one would assume that the waveforms should be modeled as a linear ramp, then a flat step, followed by another linear ramp. However, we have seen that the plateau can be far from flat and often it smears out so it is almost unnoticeable. This leads us to conclude that the driver output can be modeled accurately by two ramps. These two ramps can be chosen to give a good fit for the entire transition. Modeling this waveform with more pieces may be more accurate but adds to the computational cost and does not achieve noticeably better accuracy at the far end of the line. However, as mentioned earlier, in cases with weak drivers and insignificant inductive effects, a single ramp may be sufficient for the entire transition.

Some important considerations in two-ramp modeling are choosing the slopes of the ramps and finding the breakpoint during the transition. The breakpoint is defined as the point at which the first ramp ends and the second ramp starts. The slopes can be found by an effective capacitance based approach discussed later in this paper and the breakpoint can be obtained by using a transmission line interpretation of the driver output waveform. As discussed in section 2, the driver output waveform has an initial step and then flattens; the slope of the waveform after this point is different than for the first part of the transition. We model this initial step by a first ramp and model the remaining transition as second ramp. The height of the initial step and hence the breakpoint is obtained by modeling the driver end as a source resistance in series with characteristic line impedance. This voltage divider circuit determines the initial step (or the breakpoint) at the driver output.

If the driver resistance is R_s and the line impedance is Z_0, then the height of the initial step during transition is obtained by following expression

$$Breakpoint = V_{DD}.f \text{ , where } f = \frac{Z_0}{Z_0 + R_S} \quad (1)$$

Here V_{DD} is the supply voltage. With this breakpoint, the driver output can be modeled as a two-ramp waveform shown in Figure 2. The slope of the first ramp is (V_{DD}/T_{r1}) and the slope of the second ramp is (V_{DD}/T_{r2}). The two-ramp expression is given by

$$V(t) = V_{DD}\frac{t}{T_{r1}} \qquad 0 < t < fT_{r1}$$

$$V(t) = V_{DD}\frac{t}{T_{r2}} + kfV_{DD} \qquad fT_{r1} < t < fT_{r1} + (1-f)T_{r2}$$

where, $k = (1 - \frac{T_{r1}}{T_{r2}})$ (2)

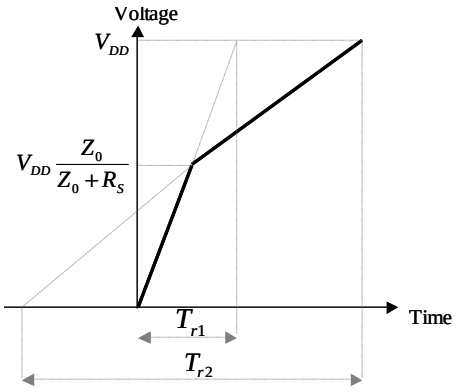

Figure 2. Two-ramp model of driver output waveform

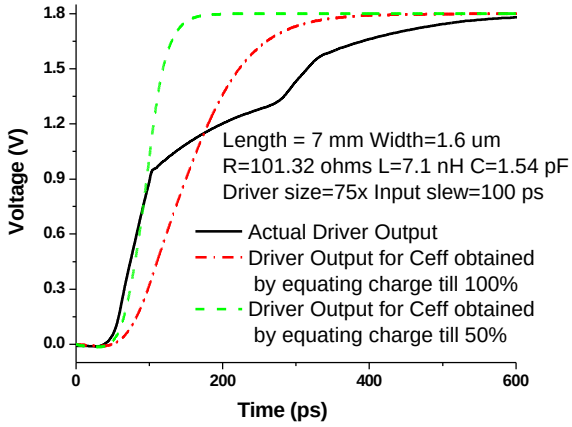

Figure 3. Driver output waveform and C_{eff} approximations

We use the above driver output model in this paper. Our modeling approach is summarized below. The details are discussed in the following sections.

1. Find breakpoint using equation 1.
2. Find two effective capacitances (one for each portion of the transition).
3. Model driver output with two-ramp (first effective capacitance models first ramp and second effective capacitance models second ramp).
4. Replace the driver with a voltage source consisting of two-ramps and then convolve the ramps with the transfer function to get far-end response.

The above flow is compatible with existing pre-characterized cell tables, which store only 50% delay and output transition time for each input slew and output capacitive load. Our model uses only this information and obtains the double-ramp waveforms at the driver output. The next section discusses the computation of the effective capacitances and the two-ramp modeling in detail.

4. EFFECTIVE CAPACITANCE(S)

The underlying principle of our effective capacitance methodology is similar to the approach described in [11]. We calculate effective capacitance by equating the charge transfer required by a single capacitance to that required by the original RLC load. It has been shown in [11] that equating the charge up to 50% point captures delay accurately, but fails in modeling the tail portion of the transition. We have found that in RLC loads with dominant inductive effects, we see a flattened second half (long tail) regularly. Thus integrating up to the 50% point is always inaccurate because it gives unacceptably large errors in slew (although it may model delay well). Also, equating the charge over the entire region of the transition will not address this problem, since this approach yields an *averaged* curve where both the delay and slew may be inaccurate. Figure 3 shows how equating charge up to the 50% or 100% point can cause significant errors in modeling driver output waveforms. The equations used to calculate the effective capacitance in this figure are derived later in the section.

This leads us to conclude that a single effective capacitance cannot model the entire transition accurately. The key idea we use in our approach is to model driver output as a two-ramp waveform as described in section 3. We then find two effective capacitances, where the first effective capacitance models the first ramp and is obtained by equating average charge during the transition of the first ramp. The second effective capacitance models the second ramp and is calculated by equating average charge during the interval when the second ramp is in transition.

The driving point RLC interconnect is modeled as reduced order approximation, obtained from matching the moments of the input admittance of the interconnect. We model the driving point admittance as the following rational function:

$$Y(s) = \frac{a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2} \quad (3)$$

The above expression is similar to the admittance of a RLC Π load. The coefficients in equation 3 can be easily obtained by matching first five moments of the driving point admittance.

4.1 C_{eff1} Calculation

For the first ramp of the two-ramp waveform described in Equation 2:

$$V(s) = \frac{V_{DD}}{T_{r1}} \frac{1}{s^2}$$

The current delivered to the interconnect is given by

$$I(s) = V(s)Y(s) = \frac{V_{DD}}{T_{r1}} \frac{1}{s^2} \left(\frac{a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2} \right)$$

We need to consider the cases of real and imaginary poles. Let us first assume that the roots of $s^2 + \frac{b_1}{b_2} s + \frac{1}{b_2} = 0$ are real. Let the roots be s_1 and s_2. Using inverse Laplace transform, we obtain

$$I(t) = \frac{V_{DD}}{T_{r1}} \left(a_1 + \frac{a_1 + a_2 s_1 + a_3 s_1^2}{b_2 s_1 (s_1 - s_2)} e^{s_1 t} + \frac{a_1 + a_2 s_2 + a_3 s_2^2}{b_2 s_2 (s_2 - s_1)} e^{s_2 t} \right)$$

We define C_{eff1} to be the capacitance that requires the same charge transfer as that required by the RLC moments during the interval when the first ramp is in transition. From Figure 2 we know that the first ramp is in transition from $t=0$ to $t=fT_{r1}$, where f can be calculated from equation 1. Charge transferred to the moments

can be calculated by integrating I(t) from 0 to fT_{r1}. Also, the charge transfer associated with charging the effective capacitance for this interval is given by $C_{eff1}fV_{DD}$.

$$\int_0^{fT_{r1}} I(t)dt = C_{eff1} fV_{DD}$$

Solving the above equation for C_{eff1}

$$C_{eff1} = a_1 + \frac{a_1 + a_2 s_1 + a_3 s_1^2}{T_{r1} f b_2 s_1^2 (s_1 - s_2)}(e^{s_1 T_{r1} f} - 1) + \frac{a_1 + a_2 s_2 + a_3 s_2^2}{T_{r1} f b_2 s_2^2 (s_2 - s_1)}(e^{s_2 T_{r1} f} - 1) \quad (4)$$

Now let us assume that the roots of $s^2 + \frac{b_1}{b_2}s + \frac{1}{b_2} = 0$ are imaginary. Let the roots be α+jβ and α-jβ.

$$I(t) = \frac{V_{DD}}{T_{r1}}\left(a_1 + e^{at}\cos bt(\frac{a_3}{b_2} - a_1) + e^{at}\sin bt(\frac{a_1 b_2 a + a_2 + a_3 a}{b_2 b})\right)$$

By equating the charge in a similar way as done for real roots, we have

$$C_{eff1} = a_1 + \frac{1}{fT_{r1}}(\frac{a_3}{b_2} - a_1)\int_0^{fT_{r1}}(e^{at}\cos bt)dt + (\frac{a_1 b_2 a + a_2 + a_3 a}{fT_{r1} b_2 b})\int_0^{fT_{r1}}(e^{at}\sin bt)dt$$

$$\int (e^{at}\cos bt)dt = \frac{e^{at}(a\cos bt + b\sin bt)}{a^2 + b^2}$$

$$\int (e^{at}\sin bt)dt = \frac{e^{at}(a\sin bt - b\cos bt)}{a^2 + b^2} \quad (5)$$

C_{eff1} can be obtained by iterating on T_{r1}. We start with an initial guess of C_{eff1}=total capacitance and iteratively improve effective capacitance until the value converges. T_{r1} at each step can be obtained from pre-characterized cell information and T_{r1} corresponding to the final C_{eff1} is used to model the first ramp. We now need to derive expressions for C_{eff2} to completely model the driving point waveform.

4.2 C_{eff2} Calculation

For the second part of the two-ramp waveform described in equation 2:

$$V(s) = \frac{V_{DD}}{T_{r2}}\frac{1}{s^2} + \frac{kfV_{DD}}{s}$$

We define C_{eff2} to be the capacitance that requires the same charge transfer as that required by RLC moments during the interval when the second ramp is in transition. From Figure 2 we see that the second ramp is transitioning from $t=fT_{r1}$ *to* $t=fT_{r1}+(1-f)T_{r2}$. The charge transfer for charging the effective capacitance for this interval is given by $C_{eff2}(1-f)V_{DD}$.

$$\int_{fT_{r1}}^{fT_{r1}+(1-f)T_{r2}} I(t)dt = C_{eff2}(1-f)V_{DD}$$

By using a similar approach as C_{eff1} and considering the case of real and imaginary roots separately, we have:

For real roots,

$$C_{eff2} = a_1 + Ae^{s_1 fT_{r1}}(e^{s_1(1-f)T_{r2}} - 1) + Be^{s_2 fT_{r1}}(e^{s_2(1-f)T_{r2}} - 1)$$

$$A = \frac{(a_1 + a_2 s_1 + a_3 s_1^2)(kfs_1 T_{r2} + 1)}{(1-f)b_2 s_1^2 (s_1 - s_2)T_{r2}}$$

$$B = \frac{(a_1 + a_2 s_2 + a_3 s_2^2)(kfs_2 T_{r2} + 1)}{(1-f)b_2 s_2^2 (s_2 - s_1)T_{r2}} \quad (6)$$

For imaginary roots,

$$C_{eff2} = a_1 + A\int_{fT_{r1}}^{fT_{r1}+(1-f)T_{r2}}(e^{at}\cos bt)dt + B\int_{fT_{r1}}^{fT_{r1}+(1-f)T_{r2}}(e^{at}\cos bt)dt$$

$$A = \frac{1}{(1-f)}\left(\frac{a_3 - a_1 b_2}{b_2 T_{r2}} + \frac{kf(2a_3 a + a_2)}{b_2}\right)$$

$$B = \frac{1}{(1-f)}\left(\frac{a_1 b_2 a + a_2 + a_3 a}{b_2 b T_{r2}} + \frac{kf(a_1 + a_2 a + a_3 a^2 - a_3 b^2)}{b_2 b}\right) \quad (7)$$

C_{eff2} is obtained by iterating on T_{r2}. Final value of T_{r2} corresponding to the converged C_{eff2} is then used to model the second ramp. However, this value of T_{r2} should be modified to capture the plateau effect. The plateau is hard to model because it is not flat, and hence the intuitive approach of modeling driver output by linear ramp, flat step, then another ramp, is often inaccurate. We incorporate the effect of plateau by modifying the second ramp as shown in Figure 4. The point where the second ramp meets V_{DD} is shifted by the plateau time and a new ramp is fitted as shown in the figure. The new T_{r2} can be obtained by equation 8.

$$T_{r2\_new} = T_{r2} + \frac{2t_f - T_{r1}}{(1-f)} \quad (8)$$

In this equation, t_f is the time of flight and $2t_f$-T_{r1} is the duration of the plateau. The idea behind this approach is that there is no charge transfer during plateau time ($2t_f$-T_{r1}). Hence when we calculate C_{eff2} by equating the charge during the second portion of

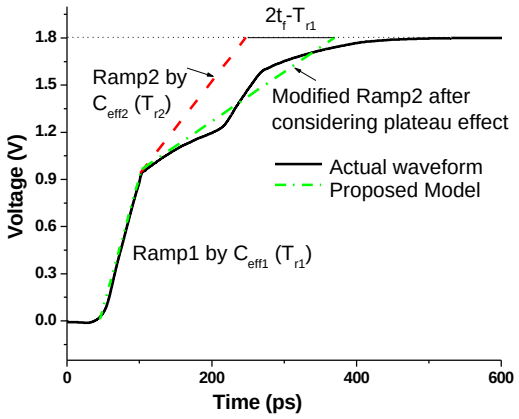

Figure 4. Proposed two-ramp

transition, we consider charge transfer after plateau but we fail to capture the delay due to the plateau effect. One solution to account for this effect is to have a flat plateau step for time $2t_f$-T_{r1} between the two ramps. Another solution is to modify T_{r2} as equation 8, where plateau delay is accounted for by shifting the second ramp by the plateau time. The first solution is more accurate when a clear flat plateau exists and the second solution works better when plateau is not flat and it smears out so much that it is almost unnoticeable. Experimentally, we have found that the second case occurs more often than flat case and hence modifying T_{r2} works better for most cases.

5. MODELING FLOW

The two-ramp modeling of the driver output waveform requires finding the breakpoint (equation 1) and computing two effective capacitances, one for each portion of transition. T_{r1} (C_{eff1}) gives the slope of the initial ramp and T_{r2_new} (C_{eff2}) gives the slope of the transition after reflection has come back to the output of the driver. In order to model the breakpoint, we need to find the on-resistance R_s of the driver. We model on-resistance by a similar approach as adopted by Thevenin models [3]. We observe the delay between 50% and 90% points of the output waveform and fit an exponential between these points. The on-resistance calculated in this way depends on the load capacitance. Ideally, one should find an effective capacitance and then calculate on-resistance of the driver for this value of the load capacitance. However, we have seen that the resistance value and more importantly, the breakpoint, do not change significantly by using total capacitance instead of the effective capacitance. Since using the effective capacitance makes this an iterative process, we use total capacitance to find on-resistance of the driver without loss of accuracy.

When the inductive effects are insignificant; the driver output waveform looks like an RC waveform. In this case, one effective capacitance is sufficient to model the entire transition accurately. This effective capacitance can be calculated by equating the charge over the entire region of transition. We have already derived equations to calculate C_{eff1}; the same equations can be used with f = 1 to calculate this single effective capacitance. Usually a single ramp obtained by this capacitance can model such waveforms very well but if there is significant resistive shielding, then the gate resistor model [11] can be used to model the exponential tail of the transition.

We use the following criteria from [4], [5] to determine the significance of inductive effects:

$$\begin{aligned} &C_L << Cl \\ &Rl \le 2Z_0 \\ &R_s < Z_0 \\ &T_r < 2t_f \end{aligned} \qquad (9)$$

Here R and C are line resistance and capacitance per unit length, l is line length, C_L is load capacitance (contributed by fan-out input capacitance), T_r is the rise time at the output of the driver, and t_f is the time of flight. If the above criteria are satisfied, then the inductive effects are significant and we use the two-ramp modeling approach. Otherwise, a single effective capacitance is used to model the driving point waveform.

The criterion in equation 9 is the same as that in [4] but with an extra condition, which compares rise time with the time of flight. This condition is important for screening short lines. These lines rarely exhibit inductive behavior because their time of flight is normally smaller than their transition time. Reference [5] considers this by comparing rise time with the time of flight but it uses transition time at the input of the driver. Inductance effects have little dependence on the input transition times but are heavily dependent on driver's output transition times [8]**.** Hence we use output transition times in our criteria. We have seen that with inductive effects, the driver output waveform rises sharply to a certain level and then flattens before meeting the reflections. While comparing the rise time with the time of flight, it is the initial ramp that is important. We compute this initial ramp (T_{r1}) using C_{eff1} iterations and use it in our inductance criteria.

The outline for our modeling flow is as follows:

Given the following information:

1. Line parasitics (R,L,C).
2. The characterized output delay table for the driver.

Perform these steps for driver output modeling:

1. Find driving point admittance moments and compute a_1 a_2 a_3 b_1 b_2.
2. Find driver on-resistance (R_s) and compute breakpoint (f) using equation (1).
3. Perform C_{eff1} iterations using equation (4) or (5) and compute $T_{r1.}$
4. Check inductance criteria using equation (9).

   If inductance is significant:

   - Perform C_{eff2} iterations using equation (6) or (7) and compute T_{r2}.
   - Modify T_{r2} to T_{r2_new} using equation (8).
   - Use $T_{r1,}$ T_{r2_new} and breakpoint to model driver output as two ramp.

   If inductance is non-significant:

   - Perform C_{eff} iterations using equation (4) or (5) with f=1 and compute T_r.
   - Model output as single ramp. If significant resistive shielding, then model exponential tail using approach in [11].

6. RESULTS

We tested the new two-ramp approach for varying line lengths, widths, and driver strengths. All the experiments were performed using a commercial 1.8V 0.18µm CMOS technology.

First, we compare the driving point waveforms obtained by our model with HSPICE simulations. Figure 5 shows two such comparisons for RLC lines driven by inverters. The inputs to the inverters are ramp signals having 100ps and 75ps transition times respectively. Although the two-ramp model cannot capture all inductive behavior (such as oscillations after the breakpoint), the overall shape, including the breakpoint and key delay points, matches well with SPICE.

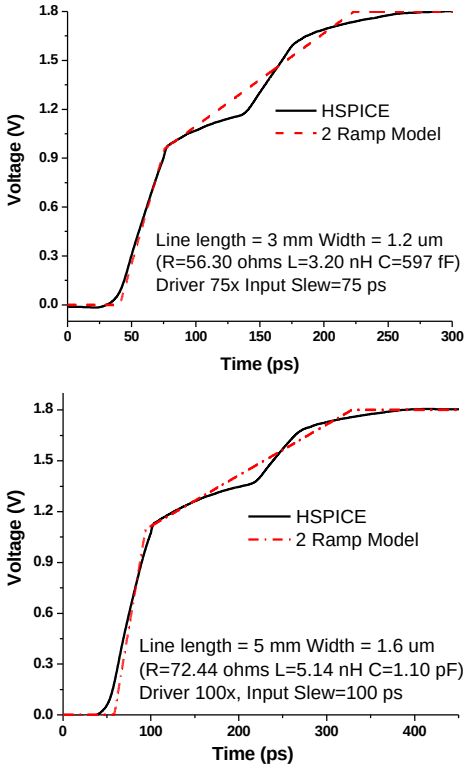

Figure 5. HSPICE and two-ramp model of driver output

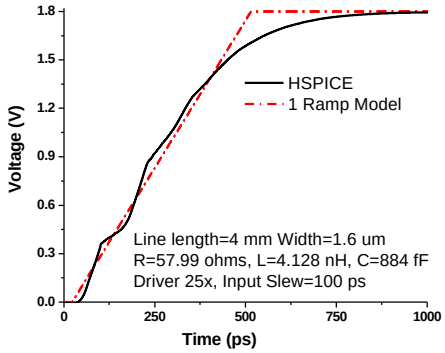

Figure 6. HSPICE and one-ramp model of driver output

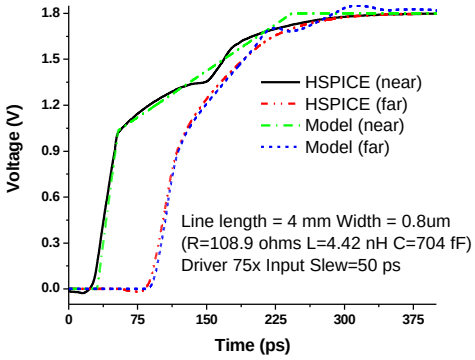

Figure 7. Near and far-end response with HSPICE and two-ramp model of driver output

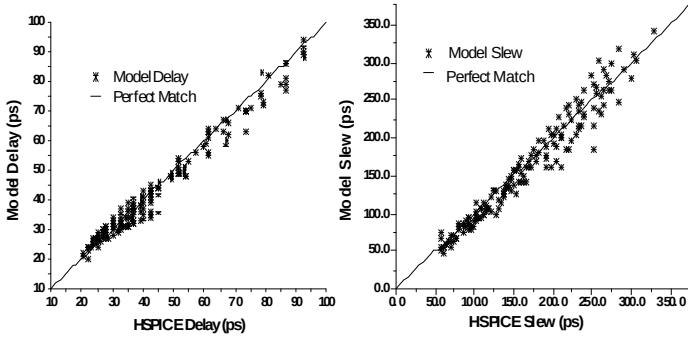

Figure 8. Two-ramp model results compared to HSPICE

Next, we compare the waveforms of a 4mm line driven by a 25x inverter (Figure 6). In this case, driver resistance was much higher than the line impedance. Inductance criteria (equation 9) were not satisfied and a single C_{eff} model was used. We see that single ramp is sufficient to model the entire transition in this case.

We also observed the far-end waveforms by applying the modeled two-ramp input waveform to an RLC line within HSPICE. These waveforms were compared with the actual far-end response. A good match was seen at the far end waveforms (Figure 7), thus validating the two-ramp assumption at the near end[2].

We tested the new model by sweeping line lengths from 1mm to 7mm and line widths from 0.8µm to 3.5µm. Driver strengths were also swept from 25x to 125x. Input transition was varied from 50ps to 200ps. The line parasitics were extracted using Raphael. With 0.18µm technology, we found that inductive effects were particularly significant in long (≥ 3mm) and wider wires (≥ 1.6µm) driven by fast inverters (75x and larger). When inductive effects were dominant, the single ramp assumption was highly inaccurate and the two-ramp model provided good results. The two-ramp model results for 165 inductive cases are shown in Figure 8. The average error in the delay was 6% and the average error in the slew, times was 11.1%. For delay, 48% of the cases had less than 5% error and 83% of the cases had less than 10% error. For slew rate, 31% of the cases showed less than 5% error and 61% of the cases showed less than 10% error. Table 1 shows a sample of cases with significant inductive effects. HSPICE delay and slew numbers are compared with the single ramp and two-ramp modeling results. It is clear from the table that, as line width increases, inductive effects become more and more significant, and the delay values from one ramp assumption become more inaccurate. The slew numbers for one ramp modeling exhibits substantial error since it cannot capture the long tail of the inductive waveform.

[2] The far-end waveforms from the model show higher overshoot due to the ramp approximation at the near end.

7. CONCLUSIONS

In this paper, we presented a new approach to model the driving point waveform in the presence of RLC interconnect loads. Our approach is compatible with existing pre-characterized cell delay

Table 1. HSPICE, one-ramp and two-ramp model comparison results

Len/Wid mm/mm	Line Parasitics R(W)/L(nH)/C(pF)	Driver Size	Input Slew (ps)	Delay (ps)			Slew (ps)		
				HSPICE	2 ramp (%error)	1 ramp (%error)	HSPICE	2 ramp (%error)	1 ramp (%error)
3/0.8	81.8/3.3/0.52	75x	50	25.01	24.2 (-3.2%)	41.3 (65.1%)	124.1	129.9 (4.6%)	61.5 (-50.4%)
3/1.2	56.3/3.2/0.59	75x	50	26.44	25.6 (-3.1%)	56.3 (112.9%)	128.9	141.1 (9.4%)	91.8 (-28.7%)
3/1.6	43.5/3.1/0.66	75x	50	32.15	29.9 (-6.9%)	66.1 (105.5%)	135.4	148.8 (9.8%)	112.1 (-17.2%)
4/0.8	108.9/4.4/0.7	75x	50	25.02	25.7 (2.7%)	39.1 (56.2%)	157.3	163.1 (3.6%)	57.3 (-63.5%)
4/1.2	75/4.2/0.8	75x	50	26.51	27.7 (4.4%)	59.1 (122.9%)	164.4	179.0 (8.8%)	97.6 (-40.6%)
4/1.6	58/4.1/0.88	75x	50	32.69	30.2 (-7.6%)	74.9 (129.1%)	175.0	196.0 (12.0%)	130.5 (-25.3%)
5/1.2	93.7/5.3/1	100x	100	36.43	35.6 (-2.2%)	46.4 (27.3%)	192.8	173.7 (-9.9%)	60.0 (-68.8%)
5/1.6	72.4/5.1/1.11	100x	100	39.56	37.7 (-4.7%)	53.0 (33.9%)	200.3	204.0 (1.85%)	71.8 (-64.1%)
5/2.0	59.7/5/1.22	100x	100	42.53	39.5 (-7.1%)	63.1 (48.3%)	207.6	226.3 (9.0%)	90.9 (-56.2%)
5/2.5	49.5/4.8/1.31	100x	100	45.26	42.4 (-6.3%)	78.2 (72.7%)	212.2	231.8 (9.2%)	121.1 (-42.9%)
6/1.2	112.4/6.3/1.19	100x	100	36.44	37.0 (1.5%)	46.5 (27.6%)	222.7	203.7 (-8.5%)	60.1 (-73.0%)
6/1.6	86.9/6.2/1.33	100x	100	39.58	39.3 (-0.7%)	52.4 (32.3%)	232.0	235.5 (1.5%)	70.7 (-69.5%)
6/2.0	71.6/6/1.46	100x	100	42.55	41.4 (-2.7%)	60.8 (42.8%)	240.9	254.7 (5.7%)	86.4 (-64.1%)
6/2.5	59.3/5.8/1.58	100x	100	45.29	45.9 (1.3%)	75.1 (65.9%)	246.3	276.9 (12.4%)	114.2 (-53.6%)
6/3.0	51.2/5.6/1.80	100x	100	49.41	47.8 (-3.2%)	101.4 (105.2%)	261.7	299.1 (14.2%)	168.4 (-35.6%)

tables. We proposed a two-ramp model based on transmission line theory that accurately predicts delay and slew at the driver output when inductive effects are significant. Results show that our two-ramp model significantly reduces the error incurred due to a simple one-ramp assumption.

8. REFERENCES

[1] Arunachalam, R., Dartu, F., and Pillage, L. T. CMOS gate delay models for general RLC loading. Int. Conf. Computer Aided Design, 1997, 224-229.

[2] Bakoglu, H. B. Circuits, Interconnections and Packaging for VLSI. Addison-Wesley, 1990.

[3] Dartu, F., Menezes, N., and Pillage, L. T. Performance computation for pre-characterized CMOS gates with RC loads. IEEE Trans. CAD, 15, (May 1996), 544-553.

[4] Deutsch, A. et al. When are transmission line effects important for on-chip interconnections? IEEE Trans. on Microwave Theory and Techniques, 45, (Oct. 1997), 1836-1846.

[5] Ismail, Y., Friedman, E., and Neves, J. Performance criteria for evaluating the importance of on-chip inductance. Int. Symp. Circuits and Systems, 1998, 244-247.

[6] Kashyap, C. V., and Krauter, B. L. A realizable driving point model for on-chip interconnect with inductance. Design Automation Conference, 2000, 190-195.

[7] Krauter, B., Mehrotra, S., and Chandramouli, V. Including inductive effects in interconnect timing analysis. Custom Integrated Circuits, 1999, 445 -452.

[8] Lin, S., Chang, N., and Nakagawa, S. Quick on-chip self and mutual inductance screen. Int. Symp. Quality Electronic Design, 2000, 513-520.

[9] O'Brien, P. R., and Savarino, T. L. Modeling the driving point characteristic of resistive interconnect for accurate delay estimation. Int. Conf. Computer Aided Design, Nov. 1989, 512-515.

[10] Pillage, L. T., and Rohrer, R. Asymptotic waveform evaluation for timing analysis. IEEE Trans. CAD, 9, (April 1990), 352-366.

[11] Qian, J., Pullela, S., and Pillage, L. T. Modeling the effective capacitance for the RC interconnect of CMOS gates. IEEE Trans. CAD, 13, (Dec 1994), 1526-1535.