Analysis and Reduction of On-Chip Inductance Effects in Power Supply Grids

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Abstract

Power supply integrity has become a critical concern in modern chip design. To date, analysis of so-called LdI/dt drop in supply networks has mostly focused inductance of the package, which is the predominant factor in inductive voltage drop. However, with increased clock frequencies and power supply demands, on-chip inductance has become a significant factor in the total LdI/dt drop. In this paper, we analyze the impact of on-chip inductance on power supply integrity and propose methods that significantly reduce the voltage drop caused by on-chip inductance. We develop a detailed model of a flip-chip supply network based on an industrial design. The model includes an accurate package model, a PEEC-based model of the on-chip supply interconnects and both intrinsic and explicit on-chip decoupling capacitance. We show that on-chip inductance can account for up to 30% of the total voltage drop in the Giga Hertz processor domain and propose two new on-chip power supply topologies that reduce the on-chip LdI/dt drop by around 70%.

1. Introduction

As process technology has continued to scale to smaller dimensions, power supply integrity has become an increasingly pressing concern. This is due to the increased power consumption of modern processors which, combined with reduced supply voltage has lead to dramatic increases in supply current demand. In particular, the inductance voltage drop in supply networks, referred to as LdI/dt drop, has become a critical issue since it is also aggravated by the continual increase in clock frequency. Since supply voltage fluctuations can impact circuit delay and signal integrity, as well as oxide reliability, they must be tightly controlled and significant effort and silicon resources are devoted to the power supply design in modern processors.

Traditionally, inductance voltage drops have focused on the package inductance, which forms the predominant component of the inductance in a supply network [1-3]. A number of methods to analyze supply networks in the presence of package inductance has hence been proposed [1-3]. However, as the operating frequency increases and the currents in on-chip supply wires becomes higher, on-chip inductance must be incorporated in the total inductance analysis as well.

One method to suppress excessive voltage fluctuations is to add on-chip decoupling capacitance to a design. Typically, it is possible to add explicit on-chip decoupling capacitance that doubles or triples the total decoupling capacitance that is inherently present in a design due to the MOSFET capacitance of non-switching gates in the circuit. However, to significantly increase the total decoupling capacitance in a design using explicit decoupling structures often results in increased die size and is therefore costly. Also, since inductance voltage drop reduces as the square-root of the added decoupling capacitance, significant increased in decoupling capacitance are needed to address inductance voltage drops [4]. Finally, it should also be noted that resistive voltage drops, referred to as IR-drop, can be fairly easily addressed by allocating more metal resource to the supply grid, hence reducing the interconnect resistance. On the other hand, reducing on-chip inductive voltage drops is more difficult, since inductance is a function of the current return loops, and hence requires not simply additional metal resources, but also new power grid topologies.

In this paper, we study the impact of on-chip inductance on power supply integrity. We develop a detailed model of the supply network, where the package interconnect is extracted using a commercial inductance extraction tool and on-chip interconnect is modeled using a detailed PEEC (Partial Electrical Equivalent Circuit) model [5]. The model includes on-chip decoupling capacitance and distributed current sources that model the current demand characteristics of a processor that is rapidly switching from low power to high power instructions. The supply grid topology is based on a industrial processor using a flip-chip packaging technology. In order to allow for reasonable simulation run times, we utilize block diagonal sparsification of the mutual inductances in the PEEC model. We demonstrate the accuracy of the proposed model and study the impact of inductance at different layers of the on-chip supply network. We show that the on-chip inductance can account for up to 15% of the total

voltage drop. We also propose two alternate power grid topologies that reduce the on-chip inductive supply drop by 70% while posing minimal impact on the routability of the design.

The remainder of this paper is organized as follows. Section 2 discusses the proposed power grid topology and model. Section 3 studies the impact of on-chip inductance on the supply voltage integrity. Section 4 presents new on-chip topologies that significantly reduce the on-chip LdI/dt drop. Finally, section 5 presents our conclusions.

2. Power distribution topology and model

The power grid topology is based on an industrial processor using flip-chip package technology and is shown in Figure 1 using a 3D graph. The power lines between adjacent layers are connected with vias. The power grid structure is regular with C4 [6] locations arranged in a checker-board fashion. Due to this regularity, it is not necessary to model the supply grid for the entire chip, and simulation can be restricted to a small area representative of the repeated structure. In our simulations, we model the region defined by a 3 X 3 array of power and ground pads. The specific widths and pitches of the power supply wires are given in Table 1.

As shown the Figure 1, the top 4 layers were implemented in the power supply model. The simulation results presented in Section 3 demonstrate that the top 2 layers incur by far the most significant voltage drops due to on-chip inductance. Therefore, modeling the top 4 layers was found to be sufficient to examine the effect of on-chip inductance on power supply integrity.

We used a PEEC-based model which represents the power supply layout with RLC circuit elements. In this model, each metal line is represented with a circuit model that consists of resistance, self inductance, mutual inductance to other wires, and grounded and coupling capacitance. To extract the interconnect RLC element values, several known methods were applied. The resistance was calculated as a function of length, width and sheet resistance. The segment capacitance to ground and the coupling capacitance between each pair of adjacent metal lines was computed using Wong's model [7]. The partial self and mutual inductances were computed based on the geometry of the wire segments using a closed form solution of the double volume integral over the two conductors as discussed in [8].

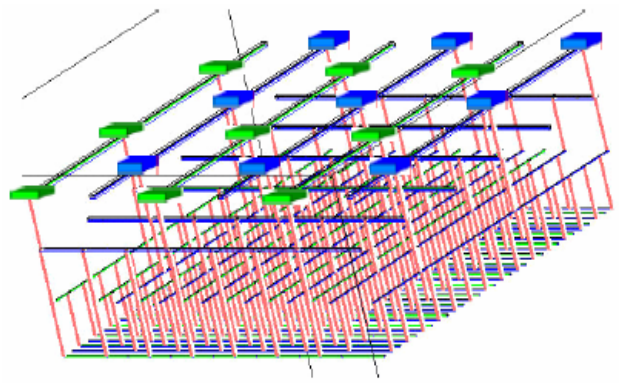

Figure 1. Power distribution grid topology with top 4 layers.

Table 1. Specification of metal lines in power distribution grid.

Metal Layer	Pitch (vdd to vdd)	Width
9	600μm	24μm
8	600μm	9μm
7	200μm	3μm
6	85μm	1μm

For decoupling capacitance, three sources were considered: explicit decoupling structures, n-well capacitance, and device decoupling capacitance. We applied a statistical model for device decoupling capacitance which represents the average decoupling capacitance during the operation of the chip as discussed in [1]. In addition, explicit decoupling capacitances were added to model explicit decoupling capacitance structures.

The package supply interconnect was modeled with an equivalent circuit model representing parasitic resistances, inductances and capacitances of the package. This model was generated from detailed package geometry information using a commercial extraction tool. Compared with wire bond packages, the flip chip bump technology represents significantly reduce package resistance and inductances.

3. Analysis of on-chip inductance of power supply grid

Using the constructed power supply network, we simulated the voltage response under worst-case current conditions. The applied current waveform for Vdd to Gnd

is shown in Figure 2. In this waveform, the low current in the first portion of the waveform represents execution of low power instructions, such as no-op instructions, and the high current in the second portion represents high power instruction, such as multiply or vector instructions. The transition from low to high power instructions takes place in 5 instructions, and represents an dI/dt event that generates a worst-case LdI/dt response. In addition to the transition from low to high power instructions, each cycle has a 5% variation in current demand to model the fluctuation of current within a single clock cycle.

Figure 3. shows the SPICE simulation results of the supply grid model. In addition to the full interconnect model, including package and on-chip inductance, we also show the response when only on-chip inductance is modeled, when only package inductance is modeled, and when neither is modeled. In the later case, only IR-drop will be present. The worst-case voltage drop in each scenario is also shown in Table 2. As expected, the largest voltage drop occurs in the presence of both package and on-chip inductance. From the results, it is clear that on-chip inductance has a significant impact on the power supply integrity and represents approximately 15% of the total voltage drop and 25% of the LdI/dt voltage drop. It can also be seen that the resonance frequency of the response with on-chip inductance is lower than that without on-chip inductance due to the extra inductance that the on-chip interconnect adds to the system. Finally, it should be noted that the simulator and the steady state behavior of the circuit due to a mismatch between the initial conditions determine the initial fluctuations at the start of the simulation. However, these artificial fluctuations quickly die out in the simulation and do not affect the worst-case voltage drop results.

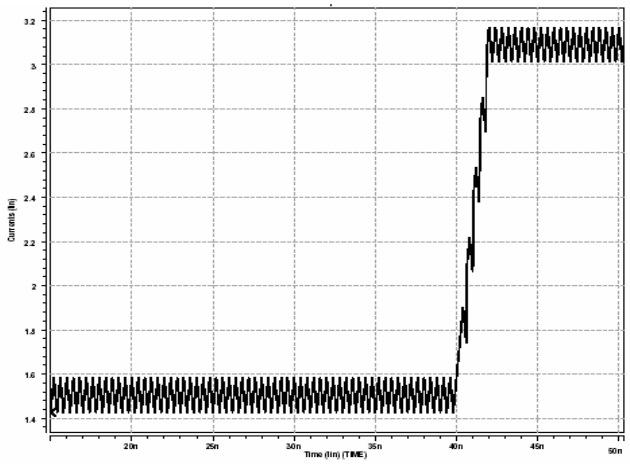

Figure 2. Current waveform in power grids analysis.

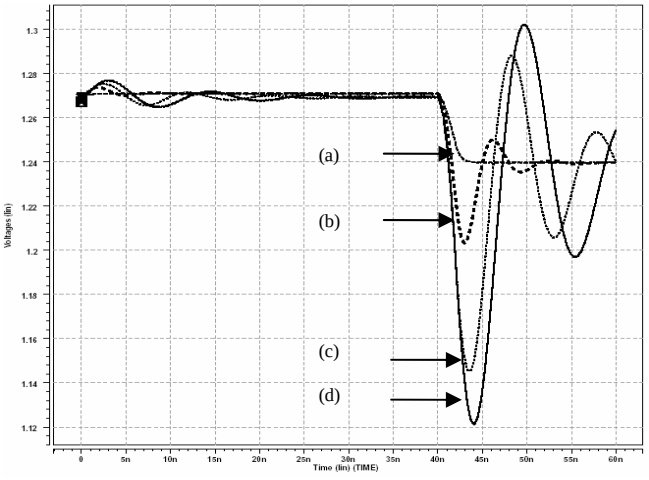

Figure 3. Simulation results of: (a) RC model, (b) RLC model with only on-chip inductances for inductance elements, (c) RLC model with only package inductances for inductance elements, and (d) RLC model with package and on-chip inductances for inductance elements.

Table 2. Voltage drops due to on-chip inductance.

	RC model	RLC with on-chip inductance	RLC with package inductance	RLC with both of the inductances
Voltage drops from supplied voltage	4.6%	7.38%	11.8%	13.8%
Normalized percentage	33.3 %	53.5%	85.5%	100%

The inductance matrix in the PEEC model is dense, meaning that it contains a mutual inductance for each possible pair of non-orthogonal conductors. Hence, the total number of inductances in the proposed model is very large, exceeding 1G elements. It is therefore necessary to reduce the size of this inductance matrix. In our analysis, we use block-diagonal sparsification of the inductance matrix [9]. In this approach, the chip is divided into n x n rectangular regions and all mutual inductances between different regions are discarded, while all mutual inductances within a region are preserved. As the number of regions in increased, the total number of mutual inductances reduces and the simulation becomes more approximate.

Figure 4 shows the simulation results for different block diagonal partition sizes. The number of mutual inductances and the run time are shown in Table3. As can be seen, the number of mutual inductances grows as the reciprocal of the number of partitions. As the number of

partitions reduces, the total number of mutual inductances increases and, as can be seen from Figure 4, the voltage drop increases. For 5x5 and 4x4 partitions, the results are nearly identical, indicating that adding additional mutual inductances does not significantly improve the accuracy of the analysis.

To examine the layer dependency of on-chip inductance on the voltage drops, we compare the voltage drop when on-chip inductance is restricted to the top two layers, the bottom two layers, and all four layers. The results are shown in Figure 5 and show that on-chip inductance in the top two layers result in substantially more voltage drop than the on-chip inductance on the lowest two layers does. This is expected since the lower layers have a much tighter pitch, resulting in a smaller current loop area. Note also that the summation of the voltage drops resulting in the simulation when on-chip inductance is modeled only in the top two or bottom two layers was less than that if on-chip inductance was modeled in all four layers. This is the caused by the mutual inductance that exists between the top and bottom layers if inductance is modeled in all layers simultaneously, which suppresses the total inductance.

Table 3. Runtime and number of mutual inductance with different number of block diagonal partitions.

	# of blocks	# of mutual inductances	Simulation time	Worst drop
4 x 4	16	0.2M	8h	1.208
5 x 5	25	0.09M	4h	1.210
6 x 6	36	0.04M	2h	1.215

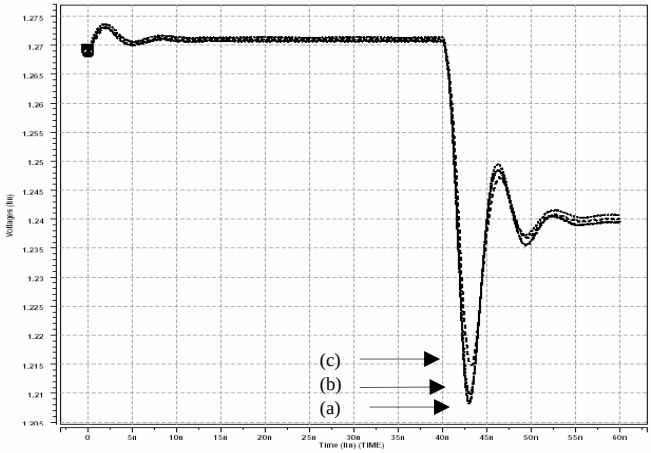

Figure 4. Simulation result of RLC model with different sizes of block diagonal sparsification: (a) 4 x 4, (b) 5 x 5, (c) 6 x 6.

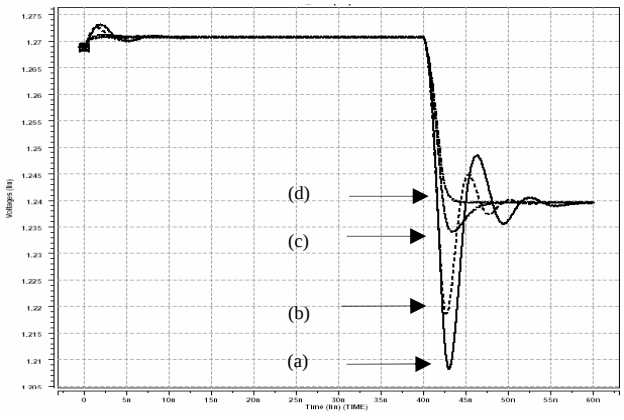

Figure 5. Simulation results of RLC and RC with layers: (a) on-chip inductance for all layers (b) on-chip inductance for top two layers (c) on-chip inductance for bottom two layers (d) RC only for all layers.

4. Design techniques to reduce voltage drops

In this section, we present two new power grid topologies that reduce the voltage drop induced by on-chip inductance. The original power grid design, which we refer to as the interdigitated topology, is shown in Figure 6(a) and consists of alternating power and ground lines that are equally spaced. However, due to the large spacing of the power grid wires, this topology results in large inductance and hence, a high supply voltage drop. The topology shown in Figure 6(b), which is refered to as the single layer paired topology, reduces the spacing between power and ground lines by adding orthogonal routs between the Vdd supply pad the Vdd wires at the top layer. As shown in the simulation results in Figure 7 and 8, this configuration significantly reduces the total voltage drop. However, this topology significantly reduces the routability of the top interconnect layer since it requires orthogonal supply wires. Hence we proposed a so-called multi-layer paired topology in Figure 6(c). In this topology the spacing between power and ground lines is reduced, similar to that in the single paired topology, however, the routability of the design is not reduced since we use paring of the supply lines at different layers.

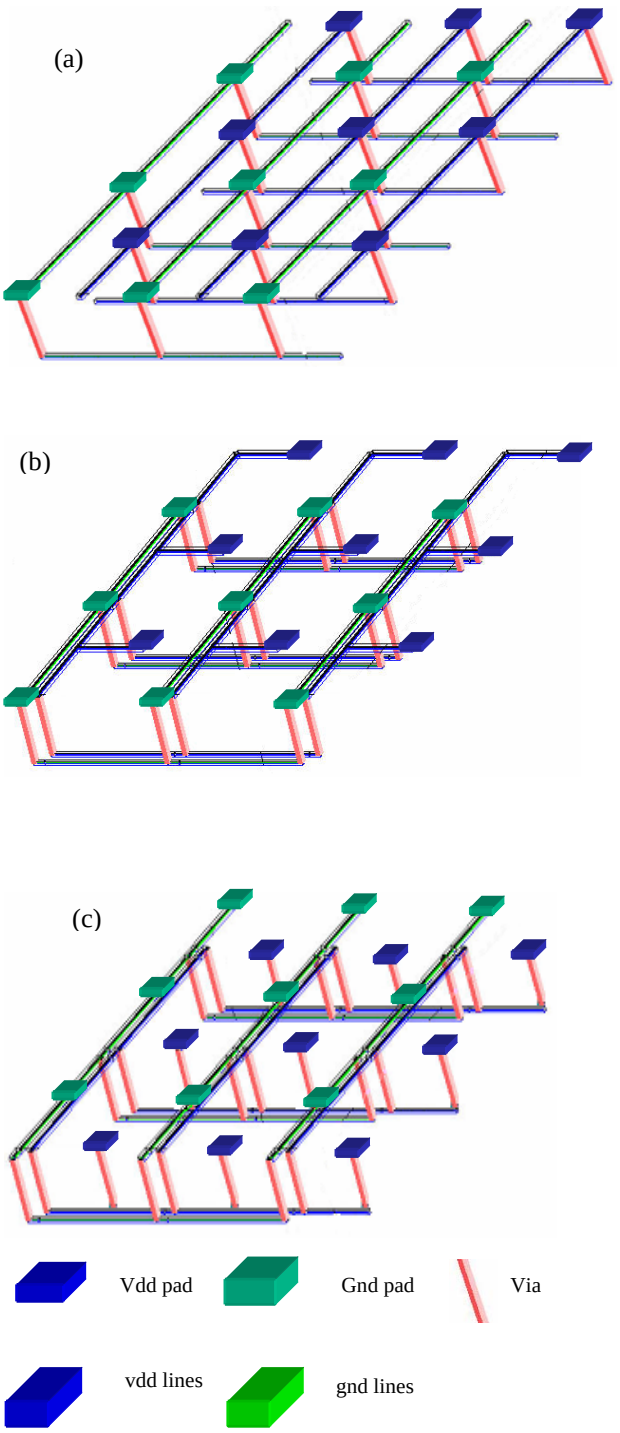

Figure 6. Three designs of power distribution grids. (a) interdigitated power grid, (b) single paired power grid, and (c) multi paired power grid.

The simulation results in Figure 7 show that the multi-layer paired topology reduced the on-chip inductive voltage drop by the largest amount while also exhibiting the smallest IR-drop. The worst-case voltage drops are also shown in Table 4. The voltage drop due to on-chip inductance was reduced by 70% using the proposed topology. Finally, we examine the layer dependency of the proposed paired topology. Figure 9 shows the voltage drops when a paired topology is used only at the top two layers, as well as when it is used only at the bottom two layers. As expected, applying the paired power grid topology at the top layers yields the most significant reduction in LdI/dt drop.

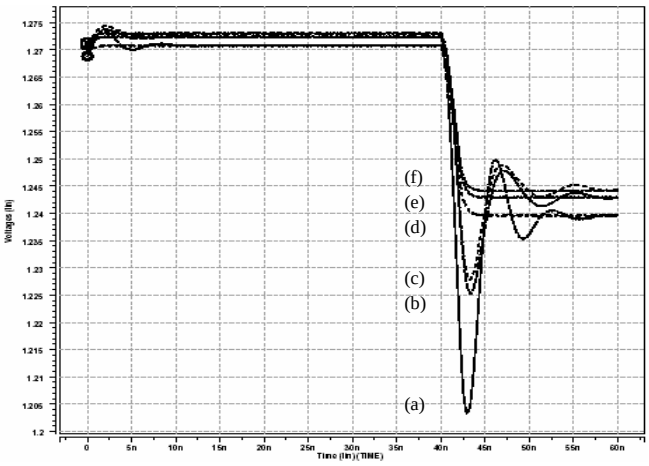

Figure 7. Simulation results of the RC and RLC of the interdigitated power grids, single paired power grids, and multi paired power grids: (a) on-chip inductance of the interdigitated power grids, (b) on-chip inductance of single paired power grids, (c) on-chip inductance of the multi paired power grids, (d) RC of the interdigitated power grids, (e) RC of the single paired power grids, and (f) RC of the multi paired power grids.

Table 4. Comparison of the voltage drops.

Simulation elements	Reference of percentage	Interdigitated method	Single paired method	Multi paired method
IR	% of voltage drop	4.6%	4.3%	4.2%
	Normalized %	100%	93.9%	91.3%
Only on-chip	% of voltage drop	7.5%	5.8%	5.3%
	Normalized %	100%	77.3%	70.7%
On-chip + package	% of voltage drop	13.8%	12.1%	11.9%
	Normalized %	100%	87%	86.2%

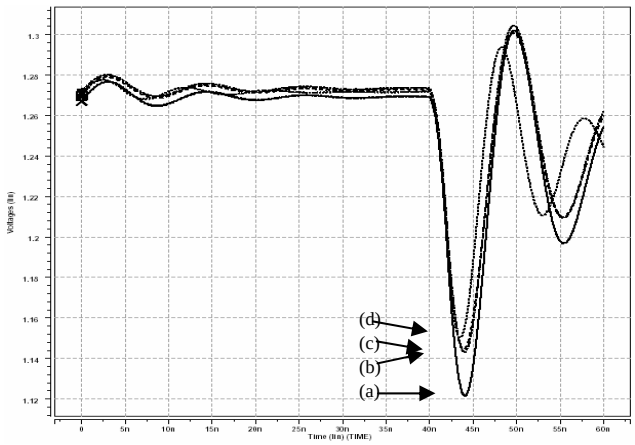

Figure 8. Simulation results of on-chip inductance with flip chip package elements: (a) interdigitated power grids, (b) single paired power grids, and (c) multi paired power grids (d) flip chip inductance without on-chip inductance.

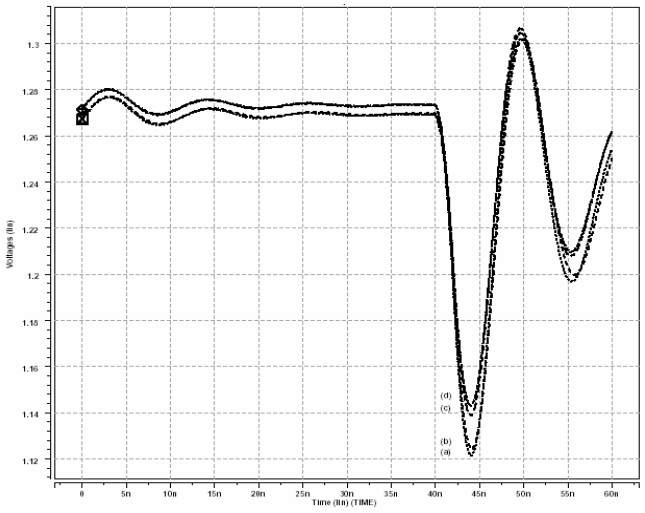

Figure 9. Simulation results of the RLC model with paired power grids with inductance at different layers: (a) interdigitated power grid at all layers, (b) paired power method at the bottom two layers and the interdigitated method ar the top two layers, (c) paired power grid at the top two layers and the interdigitated method at the bottom two layers, (d) paired power grid topology at all four layers.

5. Conclusion

In this paper, we presented a detailed study of on-chip inductance and its impact on the supply voltage drops. We proposed an accurate model of the on-chip supply network using a PEEC model. By combining this PEEC model with a detailed package model, simulations of the overall system were performed under worst-case current transitions. The analysis shows that on-chip inductance makes a significant contribution to the overall inductive voltage drop and therefore must be considered in power integrity analysis. We also showed that the impact of on-chip inductance reduces for lower layers of metal. We then proposed two new power supply topologies and demonstrate that they are effective in reducing the voltage drop induced by the on-chip inductance.

6. References

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