Noise Analysis Methodology for Partially Depleted SOI Circuits

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***Abstract*—In partially depleted silicon-on-insulator (PD-SOI) technology, signal switching history and intial state of the circuit nodes can affect the device body voltage and also cause parasitic BJT leakage currents, which can lead to significant increase in noise propagation and noise failures. In this brief we explore the effects of input switching history, initial circuit conditions and the parasitic BJT device on all steps in a traditional noise analysis methodology: noise injection, noise propagation, and noise failure criterion. We present a new noise analysis methodology to account for the floating body and the BJT effects in PD SOI technology. We demonstrate the new technique on an industrial microprocessor design in PD SOI and show that the current noise analysis methods do not account for 56% of noise fails.**

***Index Terms*—Noise, partially depleted SOI, switching history.**

I. Introduction

RECENT technology trends have lead to an increase in capacitive coupling between interconnects causing more coupling noise on a net due to switching of neighboring nets. Switching noise can cause an increase in signal delay reducing the system performance. It can also propagate through the gates in a logic path and change the latch state introducing logical errors [1].

With the emergence of partially depleted silicon-on-insulator (PD-SOI) technology, new design concerns such as the floating body (FB) and device threshold voltage (Vt) variations and parasitic bipolar junction (BJT) devices have surfaced [1], [4]. Fully depleted (FD) SOI technology does not suffer from body voltage variations but it has so far had limited commercial applications due to sensitivity to process and gate-oxide thickness variations and large source/drain resistance degrading the device performance [3].

Although PD-SOI technology has yielded significant gains in circuit performance, these gains have come at the cost of increased noise sensitivity due to the following issues.

1) Reduced source/drain capacitance i.e., smaller ground to coupling capacitance ratio, thereby increasing noise susceptibility.
2) Device body voltage variations with input switching activity. Higher body voltages yield lower device threshold voltages and increased noise propagation and noise failure.
3) Parasitic BJT in parallel with a device which can turn on when the device is in an off-state, resulting in drain-to-source current and injection of noise at the device output.

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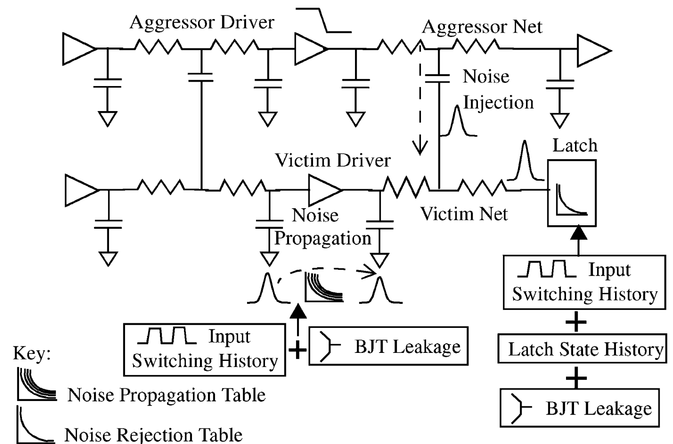

Fig. 1. Traditional noise methodology with SOI modifications.

Furthermore, the increase in gate-oxide leakage current has increased the dependence of the body voltage on the gate voltage. This has exacerbated body voltage variations and its impact on noise in PD-SOI circuits. These effects necessitate changes in current methods of noise analysis.

Fig. 1 shows the typical noise analysis steps with proposed SOI modifications.The net under consideration for noise is called the *victim* net and the nets capacitively coupled to it are called the *aggressor* nets. Aggressors switching from low to high would cause a *low overshoot* type of noise on a victim held at logic low. Similarly, an aggressors switching from high to low would cause *high undershoot* type of noise on a victim held at logic high. Traditional noise analysis tools [6] typically compute noise in three phases, as follows.

1) *Noise injection*: noise on a victim is computed due to the switching of aggressors.
2) *Noise propagation*: noise at the output of a circuit is computed given a noise pulse at its input.
3) *Noise failure*: injected noise and propagated noise is computed along a logic path till a latch is encountered and failure is determined if the latch state is altered.

In PD-SOI, the threshold voltage variation and BJT leakage would cause significant variation in the amount of propagated noise and injected noise. It would also affect the latch immunity. While extensive work has focussed on the impact of the switching history on circuit delay [4], [5], relatively little work is focussed on its impact on noise. Previous work in PD-SOI noise analysis [7] deals with the calculation of specific body voltages during noise analysis but requires *a priori* knowledge of the input states and switching histories of the nets. For most nets, however, the switching history is unknown and a worst case analysis is needed to ensure a robust design.

In this brief, we will consider the impact of switching history and input state on noise injection and noise propagation, as

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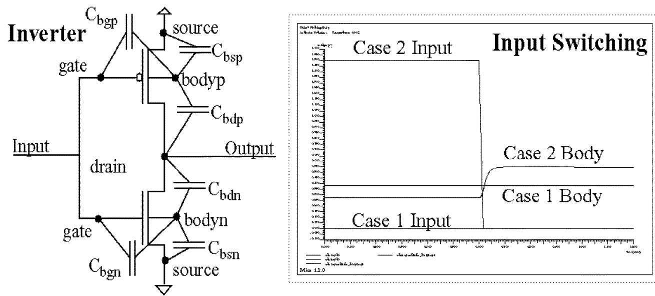

Fig. 2. Inverter input switching.

well as the latching of noise at the memory elements. We propose a practical methodology that allows direct assignment of the worst case switching history scenario to a circuit that results in maximum overall noise impact. The proposed approach is critical in detection and elimination of all possible noise failures in PD-SOI circuits. We present the results from our proposed method for 2466 nets for an industrial microprocessor design in 65-nm gate, 20-Å oxide thickness PD SOI technology [8] and show that current noise methodology only reports 65% of the nets above a noise threshold of 50 mV and accounts for 44% of all possible noise failures when used for SOI-based designs, thus, demonstrating the need for SOI-based noise analysis methodology.

II. SOI Body Voltage Variation

For the purposes of demonstrating the effect of input switching history on the device body voltage, we consider the inverter circuit in Fig. 2. The NFET body terminal is coupled to the input (gate), the output (drain), and the source terminals of the NFET. Consider the following input switching conditions.

Case 1) Input is at logic low with no switching history, output is at logic high and the body terminal of the NFET device is at an intermediate voltage between the source and drain (output) voltages of the NFET, as shown in Fig. 2.

Case 2) Input is switching logic high to logic low, output is also switching low to high. The body terminal of the NFET device is capacitively coupled to the drain (output) of the NFET and hence, the body terminal is also pulled to a higher voltage than Case 1, as shown in the SPICE plot in Fig. 2.

Since the body terminal of the NFET in Case 2 is higher than in Case 1, the input switching history results in the NFET having lower threshold voltage. This body and threshold voltage variation is a transient phenomenon, i.e., the body and threshold voltages in Case 2 would eventually converge to steady-state Case 1 body and threshold voltages, however since this would take several thousand system cycles, any noise event on the inverter input would result in increased noise propagation through the inverter. Also notice that the body terminal is initially not at logic low in Case 2 when both the source and the drain of the NFET are at logic low. This is due to the gate of the NFET at logic high and gate oxide leakage causing the body terminal to be at a higher voltage than expected. The PFET body terminal voltage variations are analogous to the NFET case discussed here.

III. Steps for SOI Noise Analysis

For SOI-based noise analysis as shown in Fig. 1, we develop an analysis approach for determining the combination of switching history for inputs to a circuit such that it results in maximum noise propagation through the circuit. This approach was used to build noise propagation tables and the noise rejection tables for circuits in an industrial microprocessor design. For maximum impact of switching on the noise propagation, we assume input switching in the cycle before the noise event on the input to a circuit. In a circuit, the input from which the noise pulse is propagated to the circuit output is called the *primary input*.

We divide the circuits on the basis of their topology into two categories: series/parallel structures, such as NAND, NOR, and AOI circuits, and pass-transistor structures, such as multiplexers.

A. Noise Propagation

The steps for determining the input switching history for maximum noise propagation for low overshoot type of noise are outlined as follows.

1) Add switching history to the primary input.
2) Determine the circuit inputs controlling the gate terminals of NFETs in series stack with the primary input controlled device; make them logic high.
3) Determine the circuit inputs controlling the gate terminals of NFETs in parallel stack with the primary input controlled device; make them logic low with switching history.
4) If inputs controlling the NFETs in parallel stacks with the primary input controlled NFET can have a switching history resulting in the parasitic BJT leakage, calculate the BJT noise, and superimpose on the worst case propagated noise.

The aim of the algorithm is to arrive at the switching history and logic values for the circuit inputs which results in maximizing the body voltage of all devices while sensitizing the input to output path for noise propagation.

1) Series/Parallel Stacks: In the simple case of an inverter, the input switching, Case 2 in Fig. 2 (methodology Step 1), should yield the maximum low overshoot noise propagation. Noise propagation curves are shown in Fig. 3. The plot has input noise pulse height on the y-axis and input noise width on the x-axis that cause a fixed noise voltage (50 mV) at the inverter output. The plot also has a noise propagation curve for a body tied (BT) inverter in comparable bulk CMOS technology. As expected, low overshoot noise propagation curve for floating body circuit with switching history for the input; Case 2 is the worst. The BT circuit has the best noise immunity, i.e., the SOI floating body circuit is more noise prone.

Similarly for NAND 3 gate, to propagate the low overshoot type noise from the primary input A0 to the output, Case 2 in Fig. 4 has switching history for A0 (SOI methodology Step 1), A1 and A2 are held high (SOI methodology Step 2). Low overshoot noise propagation curves for NAND 3 are shown in Fig. 4. Case 2 has the worst low overshoot noise propagation curve. BT NAND 3 has the least noise propagation.

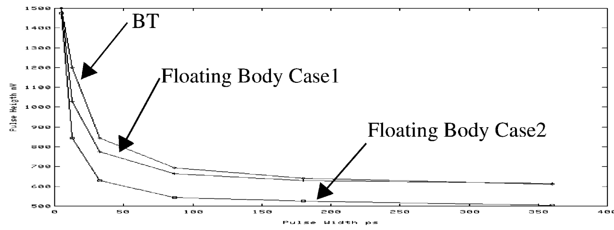

Fig. 3. Inverter noise propagation curves.

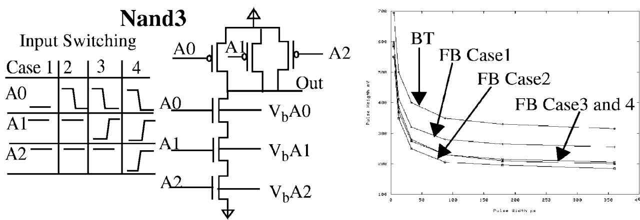

Fig. 4. Series stack NAND3.

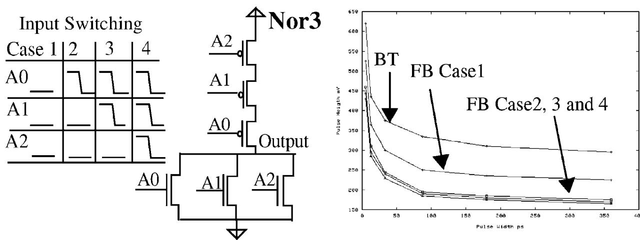

Fig. 5. Parallel stack NOR3.

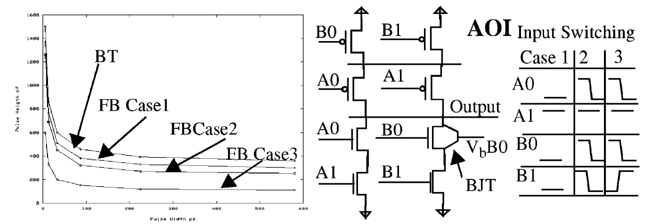

Fig. 6. Parallel and series stack AOI.

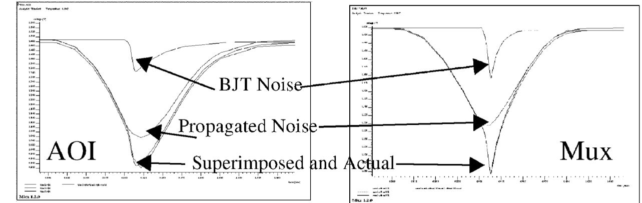

Fig. 7. AOI and MUX BJT noise superposition.

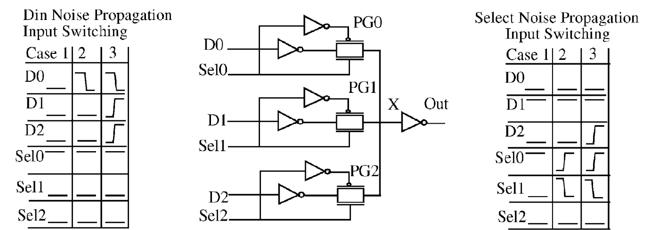

Fig. 8. Three-input MUX.

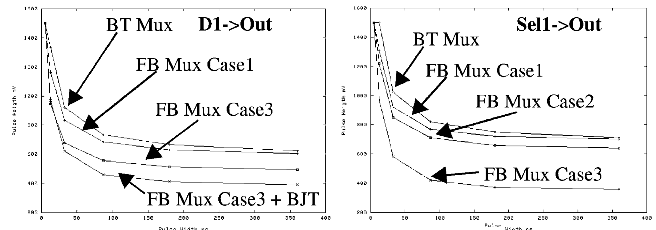

Fig. 9. MUX propagated noise curves.

For a parallel NFET stack, e.g., NOR3 gate, to propagate low overshoot noise from the primary input A0 to the output, Case 4 in Fig. 5, has all inputs A0, A1, and A2 switching (SOI methodology Step 3). Low overshoot noise propagation curves for NOR 3 are shown in Fig. 5 and Case 4 has the worst low overshoot noise propagation.

AOI circuits have parallel stacks of more than one device in series, as shown in Fig. 6. Here with Case 3 input switching there could be BJT leakage across the NFET gate controlled by input B0. This BJT noise is calculated separately and superimposed on the worst case propagated noise to get the total propagated noise as demonstrated by the SPICE simulation in Fig. 7. The noise propagation curves for the AOI stack are shown in Fig. 6. The BJT leakage with propagated noise combination (Case 3) is the worst low overshoot noise propagation curve (methodology Step 4).

Circuits more complex than considered here would require more complex analysis as illustrated by the multiplexer and latch circuits in the following sections.

2) Multiplexers: For a multiplexer (Fig. 8), propagated noise due to noise on data inputs is similar to noise propagation through a buffer and as discussed for series/parallel stacks, the worst case low overshoot noise propagation is when all data in have switching history. Noise propagation curves are shown in Fig. 9; Case 3 has the worst low overshoot noise propagation curve.

For noise propagation due to noise on a select signal, sel1, one other select signal (sel0) would require switching history such that the output of the mux is always driven by a datain inputs, D0 or D1. Also, D2 can have a switching history resulting in BJT leakage through pass gate PG2 which is calculated separately and added to select propagated noise. Fig. 7 demonstrates the additive property of the BJT noise with select propagated noise. Fig. 9 illustrates select noise propagation curves for the mux. Maximum noise is propagated with switching history on primary select input, at least one other select input and datain inputs resulting in BJT leakage.

B. Noise Injection

For calculating the injected noise, the victim driver is modeled as a linear resistance to ground (for an NFET, rail voltage for PFET). A net (victim) driven by a driver is held to logic low through this resistance, called holding resistance (holdR). All nets with significant coupling capacitances to the victim nets are considered aggressors. Noise contributions are individually calculated for each aggressor and all such contributions superimposed to get the worst case noise injected on the victim.

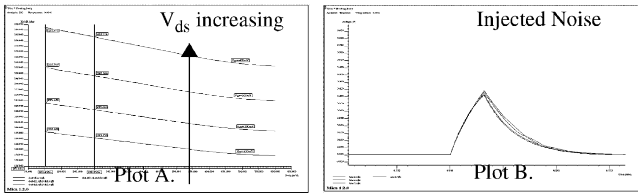

Fig. 10. Injected noise and HoldR variation.

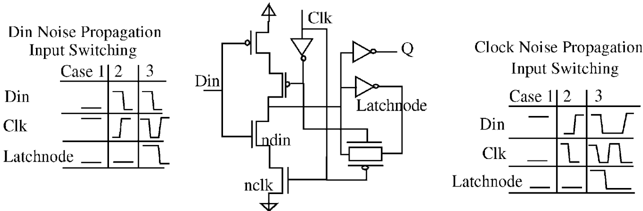

Fig. 11. Latch circuit.

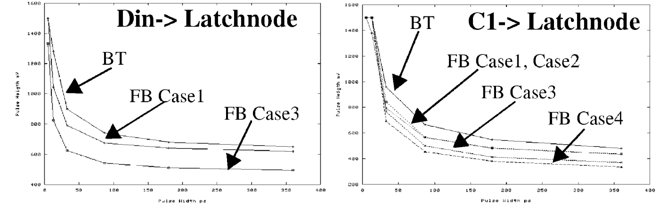

Fig. 12. Latch propagated noise curves.

TABLE I
SOI AND SPICE RESULTS FOR SELECT NETS

Net	SOI Noise Analysis	Spice	Error (%)
1	228mV	234mV	3%
2	252mV	230mV	9%
3	232mV	220mV	5%

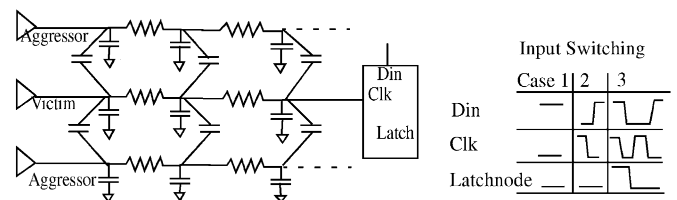

Fig. 13. SPICE setup for switching history.

The holding resistance is calculated based on the worst case input state of the driver circuit. In SOI, in addition to the input states, their switching history is also relevant. The body voltage of the device varies with the switching history and the state of the input. The variation in the body voltage translates to threshold voltage variations which would affect its current sinking capacity.

In Fig. 10, Plot A shows device body voltage for an NFET on the x-axis and holdR on the y-axis. HoldR versus body voltage curves are plotted for different drain-to-source (Vds) voltage values. For an NFET with an injected noise, i.e., Vds of 400 mV, body voltage variation from 100 to 200 mV would change the device holdR by 10 Ω. These small variations in holding resistance do not affect the injected noise significantly as illustrated by Fig. 10, Plot B. It shows injected noise on a victim net from SPICE simulations held by an SOI driver with switching history at its inputs and without input switching history. As expected the injected noise is not affected by holdR variations due to input switching activity.

C. Noise Failure Criterion

The injected noise is propagated through the gates in a logic path to a latch and if this noise pulse causes the latch to change its state it is considered a *noise functional fail*.

Consider a latch shown in Fig. 11. Latch state can alter from noise on data input, din, or clock signal, clk. The amount of noise on latch inputs altering the latch state is dependent on latch input switching history and an additional variable, *latch state switching history*. Latch state switching history is defined as latch storage node switching activity before the noise event on its inputs. Fig. 11 illustrates the input and latchnode switching cases considered for din and clk noise rejection calculations.

For din low overshoot noise rejection, with clock at logic high the latch is transparent and din to latchnode path is equivalent to an inverter (Fig. 11). Based on the noise propagation methodology in Section III-A, maximum noise propagation would occur if din has switching history. Adding switching history to clock signal either can not effect the latch state (Case 2), or could cause state switching history (Case 3). Comparing the body terminal of NFET ndin in Fig. 11 for Case 2 and Case 3, it is at a higher potential in Case 3 than in Case 2. Fig. 12 illustrates din to latchnode noise rejection curves. It can be seen that Case 3 results in worst case low overshoot noise rejection curve.

Similarly, for clock low overshoot noise rejection, clock to latchnode path is similar to select to dout path in a MUX (Section II), and maximum noise propagation would occur if clock has switching history. Adding din switching history would cause the latch state switching history (Case 3). Fig. 12 illustrates the clock noise rejection curves; Case 3 results in worst case noise rejection curve. High undershoot noise cases are analogous and can be similarly analyzed.

IV. RESULTS

The proposed SOI methodology was implemented in an industrial noise analysis tool [6]. To test the accuracy of the proposed approach, we compared the noise analysis using the pre characterized noise propagation tables (NPT) with SPICE simulation, as shown in Table I. In all cases the error was below 10%, and was largely due to run time data interpolation of data values in propagation tables, which can be further reduced by increasing the number of table entries.

We also studied the impact of different switching histories for a net using SPICE simulation. As shown in Fig. 13, the circuit used has aggressor nets injecting noise on a victim latch clock input which can have switching history as shown. Simulations were done with bulk and SOI circuits. The simulation results are shown in Fig. 14. Injected noise is the same in all cases as expected since the holding resistance does not change significantly. The propagated noise from clock input to latchnode increases from bulk technology to SOI technology. For SOI technology, including the input switching history and the latch state

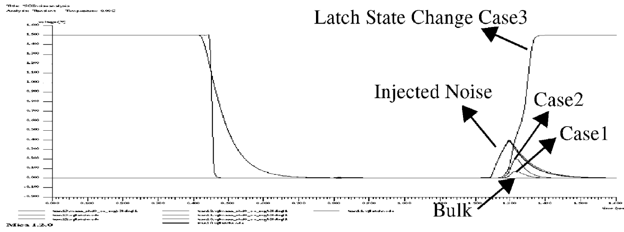

Fig. 14. Latch failure SPICE simulations.

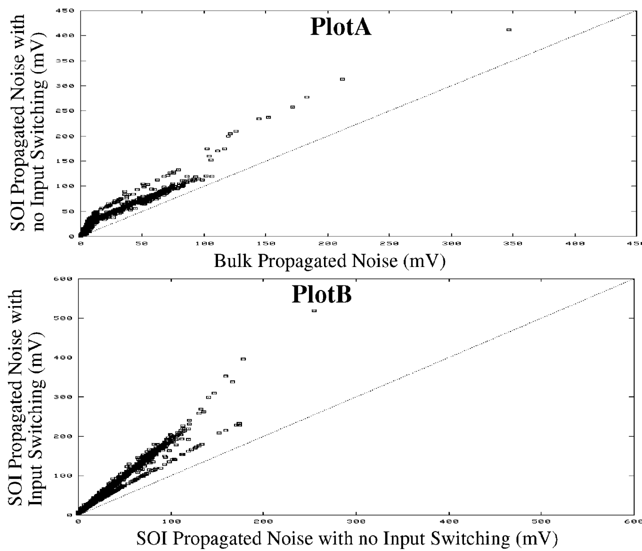

Fig. 15. Comparison of noise propagation.

switching history increases the propagated noise sufficiently to change the state of the latch causing a failure.

Finally, the SOI noise analysis tool was tested on an industrial microprocessor. The noise analysis was performed for a comparable bulk technology, SOI technology with traditional noise analysis and SOI technology with the proposed noise methodology. Data for 2446 nets is compared for all three cases for noise propagation in Fig. 15. Plot A shows each point corresponding to a net, x-axis with bulk propagated noise and y-axis with corresponding noise in SOI with traditional noise analysis. The solid line in the plot is a 45° line denoting equal propagated noise, since all plotted points are above the solid line, this plot confirms that SOI is more susceptible to noise with respect to bulk. Plot B is similar to Plot A except that it compares SOI noise calculated with traditional noise analysis to that calculated with the proposed new methodology. All plot points are above the 45° line, confirming that in SOI propagated noise increases with input switching history and that this effect is not accounted for in traditional noise analysis methodology.

TABLE II
NOISE ANALYSIS RESULTS

Total Nets=2466	Bulk	SOI with no Switching	SOI with Switching
# Nets exceeding 50mV noise height	130	391	602
# Latch nets Failing	28	128	290

To determine the impact of switching history on latching of noise, we show the number of noise failures in the three cases in Table II, the traditional methodology reports only 44% of the total fails predicted by the new methodology. In addition only 65% of the nets above a certain noise threshold are reported by the traditional methodology. Also, note that the comparable bulk technology has 90% fewer fails compared to SOI.

V. CONCLUSION

In this brief, we demonstrated the importance of considering input switching history for noise analysis in SOI-technology-based designs. We showed that SOI is more susceptible to noise due to smaller junction capacitance, floating body voltage, and parasitic BJT leakage. We showed that these effects have significant effects on propagated noise, and latching of noise which can lead to a failure otherwise not accounted for with current noise analysis tools. We proposed an efficient methodology for performing a PD-SOI aware noise analysis and demonstrated results on industrial circuit.

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