Inductance: Implications and Solutions for High-Speed Digital Circuits

SE1 Inductance Extraction and Modeling

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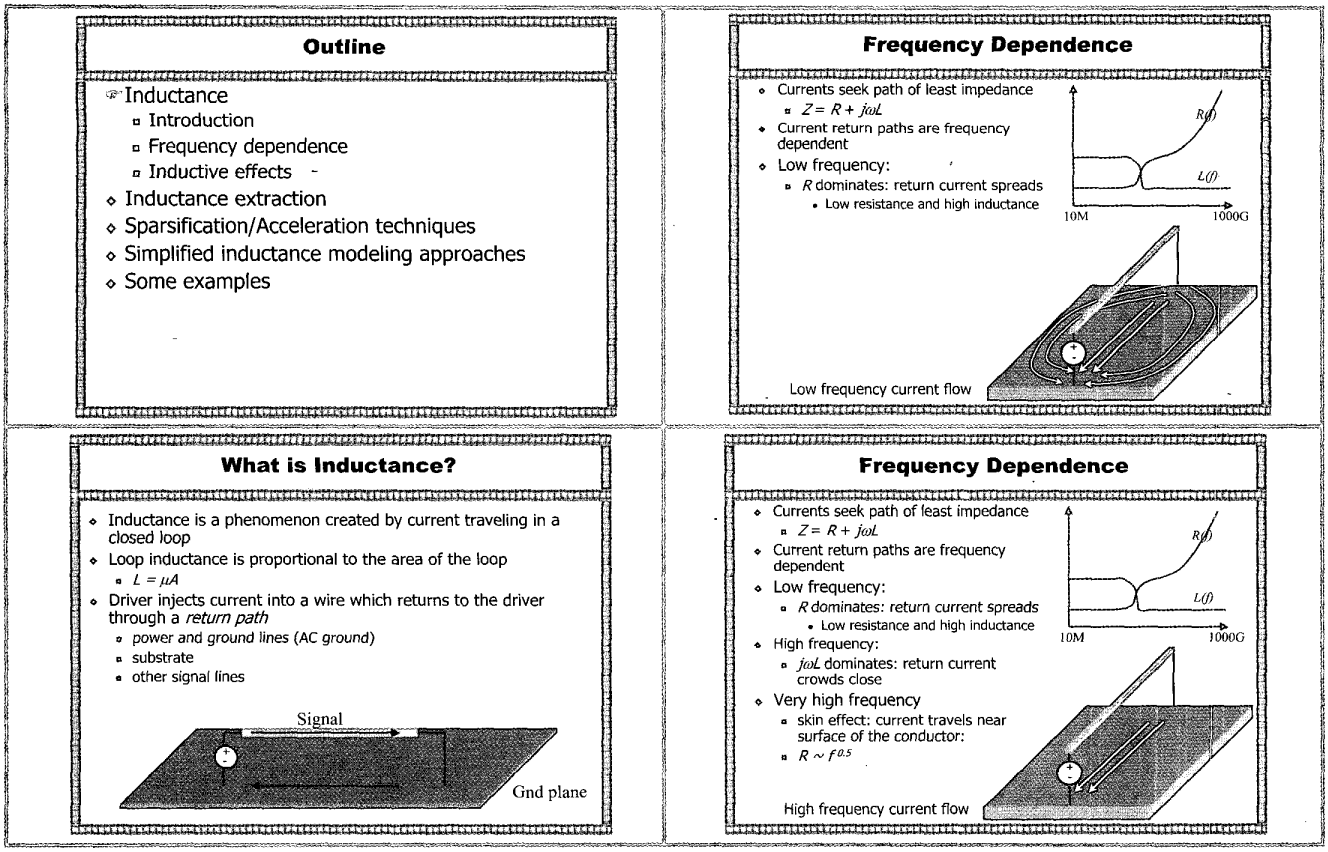
With operating frequencies entering the multi-gigahertz range, inductance is becoming an increasingly important consideration in design and analysis of on-chip interconnects. An overview is given of the extraction and analysis issues related to on-chip inductance effects, starting with a brief overview of Maxwell's equations.

The quasi-static assumption and its implications for analysis of VLSI interconnects are discussed. It is then shown how interconnects can be represented using partial element equivalent circuit (PEEC) models. The complexity of current flow in VLSI circuits is then examined and the PEEC-based model required to represent it is presented. The importance is shown of constructing a comprehensive model that includes substantial portions of the power and ground grid surrounding the signal net to model the distributed current return paths. The importance is shown of modeling the power grid decoupling capacitance, power grid supply pads, signal net coupling capacitance, and local power and ground connections of the driver and receiver gates.

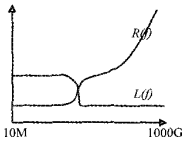
Methods are explained for simulating the constructed model and techniques that can be used to speed-up the simulation of large PEEC models. Simplified approaches are discussed that use so-called loop inductance models, or use RL circuit formulations and are compared with more detailed PEEC models. Results show the trade-off between the accuracy and efficiency of the different methods. The applicability of each method at different stages of the design is discussed. Experimental results are based on simulations of industrial circuits, including a global clock net structure of a large multi-gigahertz processor.

See Digest page 12

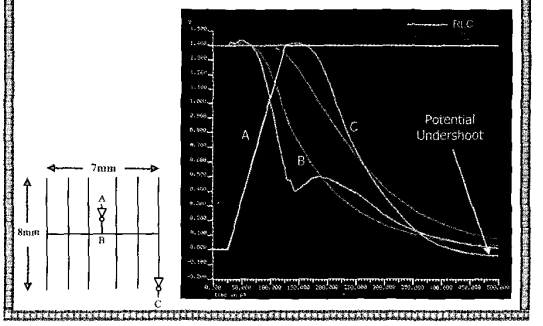


Frequency Dependence

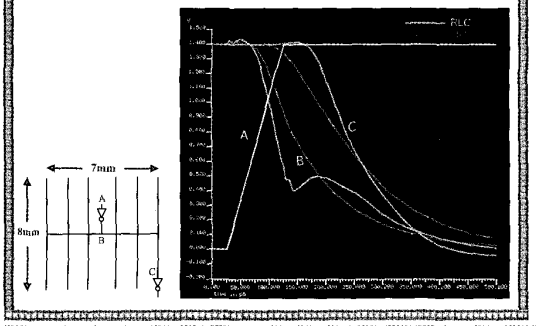
- As frequency increases:
  - R increases due to proximity and skin effect
  - L reduces due to proximity effect
- $Z = R + j\omega L$
  - $R \uparrow$
  - $L \downarrow$
  - $\omega \uparrow$
- Signal response increasingly characterized by inductance....



Inductive Effects



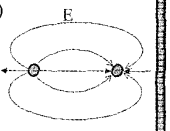
Inductive Effects



Electromagnetic Field Equations (Maxwell)

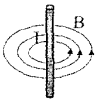
Relation between electric field & charges (Gauss' law)
- Electric field starts and ends on charges

$$\nabla \cdot D = \rho$$

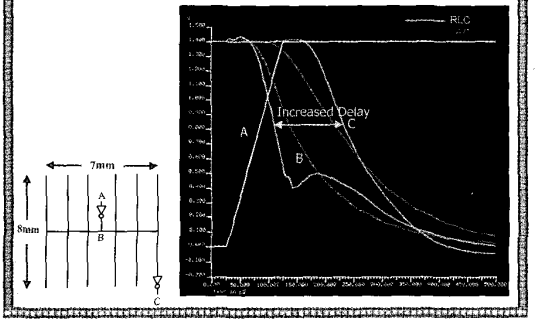


Source free nature of magnetic field
- magnetic field forms closed loops

$$\nabla \cdot B = 0$$



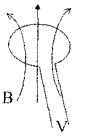
Inductive Effects



Maxwell's Equations (con't)

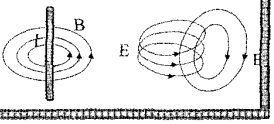
Electromagnetic induction law (Faraday's law)
- change in magnetic field induces electric field

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

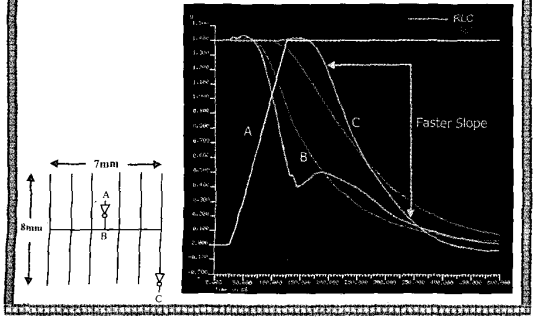


Magnetic field induced by:
- current in conductors (Amperes' law)
- change in electric field (Displacement current)

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$



Inductive Effects



Solving Maxwells eqns: full-wave simulation

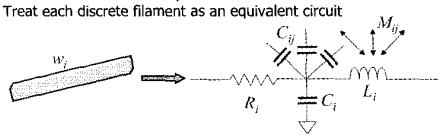
- Solutions
  - Frequency domain
  - Time domain
- Methods
  - Finite Difference Method
  - Finite Element Method (FEM)
  - Boundary Element Method (BEM)
  - Method of moments (MOM)
- Transmission line models

Common Simplifying Assumptions

- Electro-static assumption:
  - $\nabla \cdot D = \rho$, $\nabla \cdot B = 0$, $\nabla \times E = -\frac{\partial B}{\partial t}$, $\nabla \times H = J + \frac{\partial D}{\partial t}$ → $\nabla \cdot D = \rho$, $\nabla \times E = 0$
  - No current and magnetic field
  - Used for capacitance extraction
- DC assumption:
  - $\nabla \cdot D = \rho$, $\nabla \cdot B = 0$, $\nabla \times E = -\frac{\partial B}{\partial t}$, $\nabla \times H = J + \frac{\partial D}{\partial t}$ → $\nabla \cdot D = \rho$, $\nabla \times E = 0$, $\nabla \cdot B = 0$, $\nabla \times H = J$
  - Fixed current
  - Electric and magnetic field are independent
  - Current changes slow: magnetically induced voltage small compared with resistance drop
  - Used for RC interconnect simulations

PEEC Model

- A. Ruehli [IBM Journal of R&D, 1972]
- Discretize all wires for lumped model
- Treat each discrete filament as an equivalent circuit



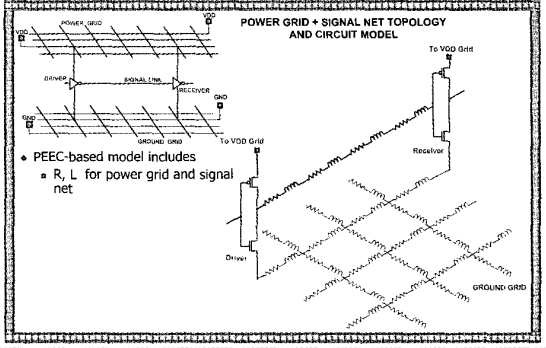
- Compute lumped parameters $R_i, L_i, M_{ij}, C_i, C_{ij}$

Quasi-static Assumption

$\nabla \cdot D = \rho$, $\nabla \cdot B = 0$, $\nabla \times E = -\frac{\partial B}{\partial t}$, $\nabla \times H = J + \frac{\partial D}{\partial t}$

- Magnetic field change creates significant electric field
- Assume:
  - -Displacement current is small
  - -Electric field change does not create significant magnetic field
- No electromagnetic wave propagation without displacement current
- Interaction between pairs of elements becomes instantaneous (no retardation)
- Valid if:
  - -- displacement current is small compared to current density J (sufficiently low frequency)
  - -- characteristic size is smaller than wavelength (10GHz wavelength is 30mm)

Full PEEC Based Circuit Model

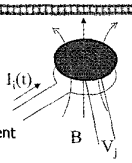


- PEEC-based model includes
  - R, L for power grid and signal net

Inductance Definition Using Flux

- Traditional definition of *inductance* in terms of magnetic flux:

$$\Phi_{ij} = \iint_{\text{Current loop } j \text{ area}} B \cdot da$$

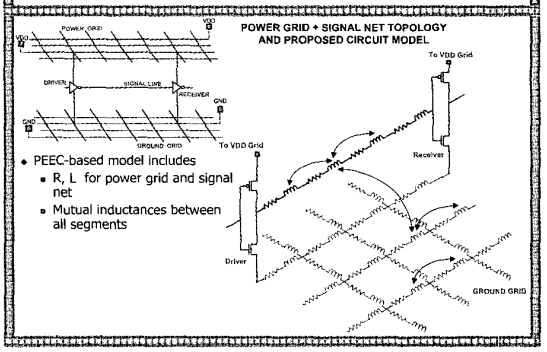


  - Inductance M_{ij} is ratio of flux in loop j over current in loop I

$$\Phi_{ij} = M_{ij} I_i$$

- Flux definition not well suited for on-chip interconnects:
  - system consist of many intersecting loops (no individual loops evident)
  - wire thickness significant compared to loop area (area integral not easily defined)

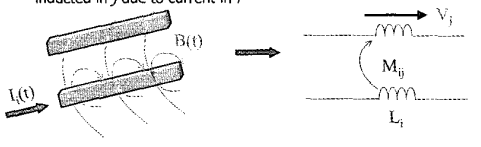
Full PEEC Based Circuit Model



- PEEC-based model includes
  - R, L for power grid and signal net
  - Mutual inductances between all segments

Partial Inductance

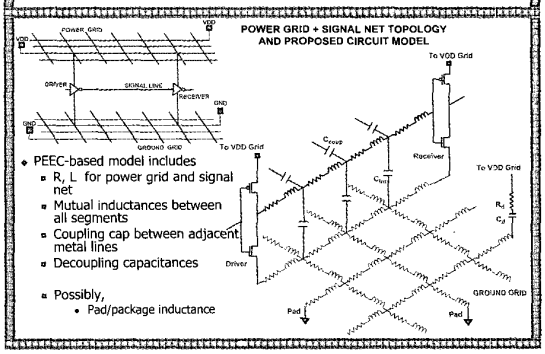
- Each wire segment is assigned partial self and mutual inductance
  - split wires into segments
  - partial inductance M_{ij} between wire segments i,j reflects voltage inducted in j due to current in i



- Analytical solution for partial inductance for parallel filaments with uniform current distribution:

$$M_{ij} = \frac{\mu}{4\pi \cdot a_i \cdot a_j} \iint_{i,j} \frac{1}{R} dV_i dV_j$$

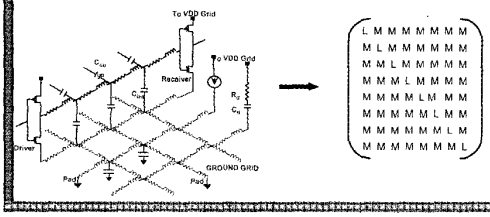
Full PEEC Based Circuit Model



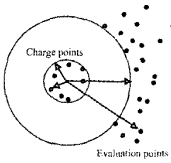
- PEEC-based model includes
  - R, L for power grid and signal net
  - Mutual inductances between all segments
  - Coupling cap between adjacent metal lines
  - Decoupling capacitances
  - Possibly,
    - Pad/package inductance

PEEC Model Approach - Issues

- *Fully-dense L matrix*
  - Computation of all mutual inductances is expensive
  - Large simulation time => needs acceleration



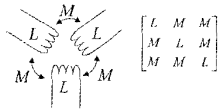
Sparsification - Implicit



- Fast Multipole (FastHenry) [Kamon IEEE-MTT '94]
  - Lump the effect of a bunch of distant conductors into a single mutual inductance

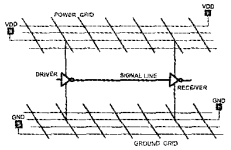
Sparsification Issue

- Simply dropping small entries from the Partial Inductance Matrix, can lead to a non-positive definite matrix.



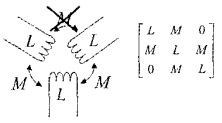
Acceleration - PRIMA

- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model



Sparsification Issue

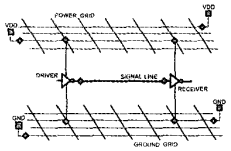
- Simply dropping small entries from the Partial Inductance Matrix, can lead to a non-positive definite matrix.
  - The incorrect sparsification results in system that generates energy.



Acceleration - PRIMA

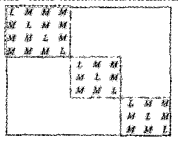
- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model

1. Define ports

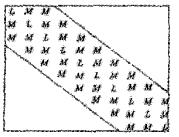


Sparsification - Explicit

- Block diagonal sparsification [Gala DAC '00]
  - Guaranteed passive
  - Loss of accuracy



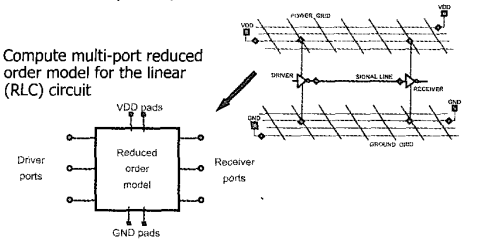
- Shift-and-truncate [Krauter ICCAD '95]
  - Remove couplings between wires with large separation
  - Better accuracy, guaranteed passive



Acceleration - PRIMA

- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model

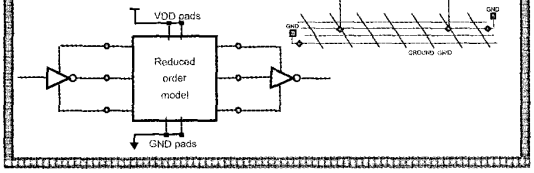
2. Compute multi-port reduced order model for the linear (RLC) circuit



Acceleration - PRIMA

- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model

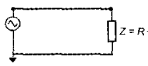
3. Combine with non-linear devices, power supply



Loop Inductance Approach

Use RL PEEC model and solve in frequency domain:

Step 1: Define grid, signal topology



IMPEDANCE EXTRACTION

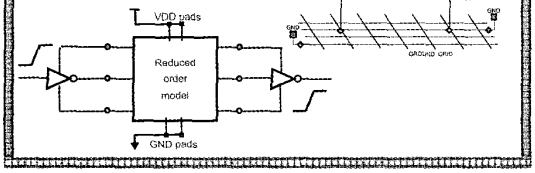
Step 2: Define port at the driver end and short the receiver end of the signal.

Step 3: Compute loop impedance

Acceleration - PRIMA

- Passive Reduced-Order Interconnect Macromodeling Algorithm
  - [Odabasioglu - ICCAD '97]
  - Guaranteed passivity of reduced order model

4. Simulate the reduced system in SPICE



Loop Inductance Approach

Use RL PEEC model and solve in frequency domain:

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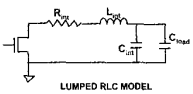


LUMPED RLC MODEL

Step 2: Define port at the driver end and short the receiver end of the signal.

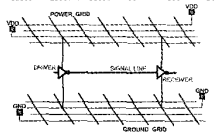
Step 3: Compute loop impedance

Step 4: Construct a lumped circuit model using the loop resistance and inductance with interconnect and load capacitance.

Loop Inductance Approach

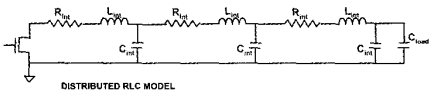
Use RL PEEC model and solve in frequency domain:

Step 1: Define grid, signal topology



POWER GRID + SIGNAL NET TOPOLOGY

Loop Inductance Approach



DISTRIBUTED RLC MODEL

Step 4: Construct a lumped circuit model using the loop resistance and inductance with interconnect and load capacitance.

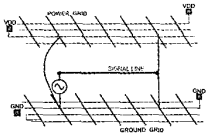
Can be extended to a distributed model

Loop Inductance Approach

Use RL PEEC model and solve in frequency domain:

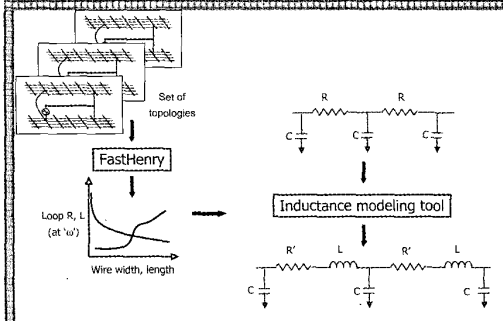
Step 1: Define grid, signal topology

Step 2: Define port at the driver end and short the receiver end of the signal.

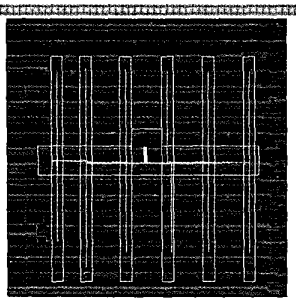


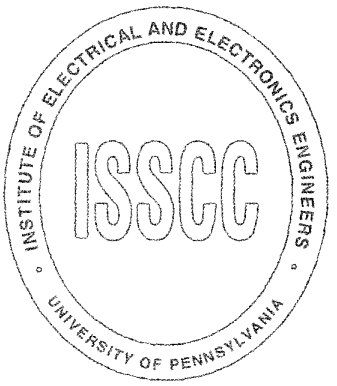
PORT DEFINITION

Characterization

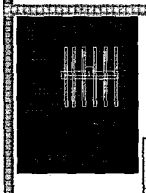


Clock net topology





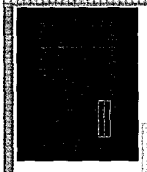
PEEC vs. Loop Inductance



Clock Net 1

	ELEMENTS				DELAY (DIFF W.R.T. PEEC)	SKEW (DIFF W.R.T PEEC)	RUN-TIME
	R	C	L	M			
PEEC	160k	400k	160k	8M	131ps	19ps	60min
RC	3k	6k	-	-	86ps (-45ps)	9ps (-10ps)	2min
LOOP	3k	6k	2k	-	116 (-15ps)	12ps (-7ps)	4min

PEEC vs. Loop Inductance



Clock Net 2

	ELEMENTS				DELAY (DIFF W.R.T. PEEC)	RUN-TIME
	R	C	L	M		
PEEC	34k	70k	34k	400k	63ps	10min
RC	400	800	-	-	44ps (-19ps)	15s
LOOP	400	800	400	-	66ps (+3ps)	30s

Summary

- On-chip inductance is important
  - Higher frequencies
  - Longer wires
- Modeling of inductance is difficult
  - Return paths complicated, frequency dependent
- Detailed model using PEEC
  - Complex
  - Run-time issues => Sparsification/Acceleration
- Simplified models using loop inductance
  - Fast
  - *Accuracy issues => Use for specific topologies*