Receiver Modeling for Static Functional Crosstalk Analysis

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Abstract. Crosstalk analysis has become a significant part of the design cycle of high performance processors in nanometer technologies. In this paper we demonstrate that current crosstalk analysis techniques that ignore the degrading effect of multiple crosstalk events on receiver noise rejection curve filter significant number of true violations. We also demonstrate that techniques that take into account the multiple crosstalk events with traditional receiver modeling result in large number of false violations. We propose improved crosstalk analysis techniques that are multiple noise event aware (MNEA) with minimal changes to existing crosstalk analysis. We also propose enhancements to existing receiver models so they can be used with the MNEA analysis resulting in reduction of number of false violations by 68%-98% while guaranteeing identification of all true violations.

1 Introduction

Crosstalk in nanometer technologies has become a major concern. Technology trends such as *interconnect scaling* has resulted in an increase in the interconnect coupling capacitance and *device scaling* has resulted in faster signal transition time and smaller system cycle time. In addition, the high performance designs are larger with long interconnects further increasing the magnitude of the crosstalk pulses induced on coupled interconnects [1] [2]. Static crosstalk analysis techniques are used for identifying the interconnects that violate the signal integrity criterion as part of the physical design process of a high performance processor. This analysis is called *functional* crosstalk analysis since the violations can lead to logic failures. The analysis is required to be fast and accurate to reduce the impact on the design process time.

A typical crosstalk analysis scheme [3] [4]is illustrated in Fig. 1. The analysis can be divided in two broad categories: device modeling and interconnect modeling. The interconnects are modeled as distributed RC network. The interconnect being analyzed for signal integrity is called the *victim*. The interconnects coupled to it are called the *aggressors*. The victim-aggressor circuit is solved with accurate and efficient reduced-order and/or analytical models proposed in [5] [6]. The aggressor set is reduced based on logical constraints, timing windows and respective clock domains between the aggressors and the victim making the analysis more realistic and the circuit to be

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analyzed smaller [4] [7]. The device modeling requires pre-characterization of the gates in the design. It comprises of: driver modeling and the victim receiver modeling. Various linear and non-linear driver models have been proposed for victim and aggressor drivers in [8] [9].

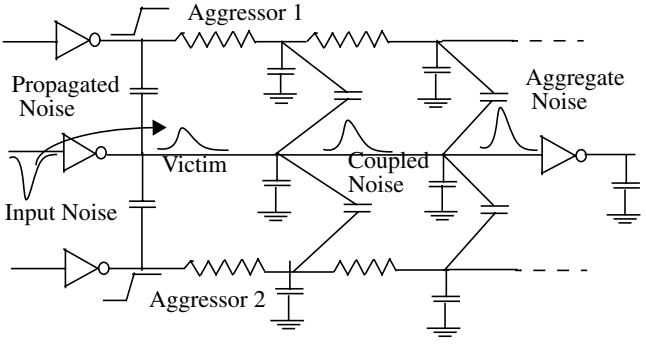

Fig. 1. Typical Static Noise Analysis Scheme

The victim receiver model is composed of input gate capacitance and set of *noise rejection curves* or *noise propagation tables*. If during the crosstalk analysis a victim pulse height exceeds its receiver noise rejection curve value or if the propagation through the receiver gate exceeds a predetermined threshold, the victim is said to fail the signal integrity requirements. Gate characterization for noise rejection curve is therefore, a critical step with direct impact on number of crosstalk violations.

For simple single input gates such as, inverters and buffers, the input noise rejection curve is easily computed. However, for multiple input gates, the noise limit for an input has a dependence on the state of other inputs of the gate. Current crosstalk analysis assumes that no two noise events on different inputs of a gate would align temporally (referred to as *Single Switching Bestcase*) but as the system frequency increases, the temporal alignment of multiple noise events has become a real possibility. To account for these events, current receiver models can be generated

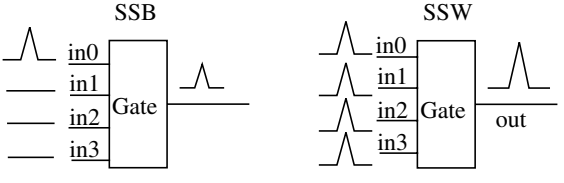

Fig. 2. SSB and SSW for a Comple x Gate

with the assumption that identical simultaneous noise pulses can occur on *all* inputs of a gate (referred to as *Single Switching Worstcase*). Both the SSB and SSW assumptions are illustrated in Fig. 2. The SSB analysis, though a practical assumption

for low frequency designs, can filter a potential signal integrity problem in high performance design with small cycle times. The SSW approach is not a practical assumption since it results in noise rejection curves that are pessimistic by 70%, which can easily lead to 10x the real crosstalk violations and an increased system design process time. The current analysis and receiver models are therefore, only suitable for simple gates such as inverters and buffers.

In this paper, we propose modifications to traditional crosstalk analysis to make it multiple noise event aware (MNEA). We apply the new enhanced analysis to an industrial microprocessor core and design blocks in 65nm bulk CMOS technology. The results demonstrate that the proposed scheme identifies the signal integrity violations which would have been overlooked with SSB crosstalk analysis. We also demonstrate that the proposed scheme reduces the number of false violations by 68% - 98% compared to SSW crosstalk analysis.

Previous work on receiver models has concentrated on determining the dc logic values for other inputs that would yield the most pessimistic noise rejection value for an input for complex gates [4]. Modeling of different noise wave shapes has also been proposed in [10] but again the modeling assumes all inputs other than the primary input are at stable dc values. There has been no modeling which accounts for the possibility of noise events on more than one input of the receiver.

2 Effect of Multiple Crosstalk Noise Events

Receiver model for a gate comprises of its input capacitance and noise rejection curves (NRC) for all its inputs. The NRC is a function of input crosstalk pulse width and gate load capacitance. A sample set of NRCs are shown in Fig. 3, each curve corresponds to a constant output load. The input noise limit (y-axis) increases with reduction in crosstalk pulse width (x-axis) and increase in gate output capacitance.

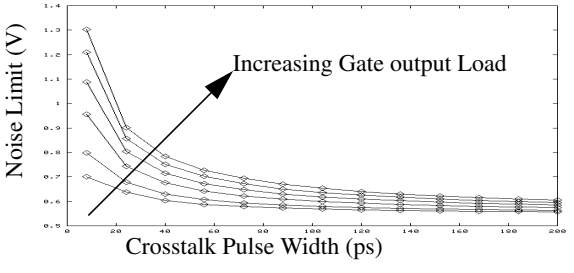

Fig. 3. Sample Noise Rejection Curves

A noise event is defined as *high-down* if the victim is at logic high and the crosstalk pulse results in a voltage dip on the victim. Analogous to this is the *low-up* noise event. Consider the AOI33 structure in Fig. 4, if the input *in00* of this gate is being characterized for noise rejection curves then:

1. Low-up noise of *in00* will be reduced if *in10* is also experiencing a low-up noise event,
2. High-down noise limit of in00 will reduce if one or both in01 and in02 are experiencing a high-down noise event as well.

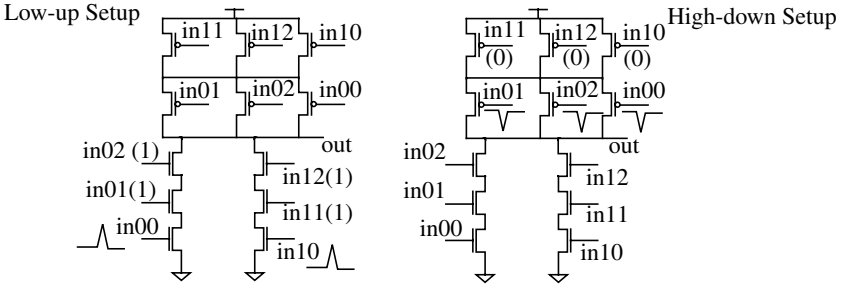

Fig. 4. AOI33 Circuit

The degradation is as a result of each source-drain parallel FET acting as an independent source of noise on the output. This behavior is exhibited by all FETs connected with source-drain parallel connections.

Fig. 5 shows the AOI33 *in00* high-down and low-up noise rejection curve degradation, for a given gate output load, as the number of inputs experiencing the noise evets is increased. The simulations are done assuming simultaneous identical noise pulses on all inputs. The high-up noise limit in this example degrades by 34% for two inputs with crosstalk event and further degrades by 12% when crosstalk event is introduced to the third input as well. The low-up noise limit degrades by 69% for crosstalk events on two inputs. This example illustrates three observations:

1. single switching bestcase (SSB) NRC for a receiver can degrade by a significant amount with multiple noise events,
2. single switching worstcase (SSW) assumptions degrades the NRC by a large amount,
3. as the number of inputs with a crosstalk event increases, the degradation in NRC reduces (diminishing returns).

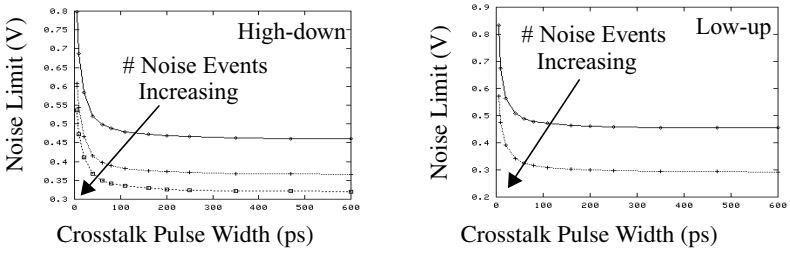

Fig. 5. AOI33 Noise Rejection Degradation

3 Crosstalk Analysis with Noise Rejection Curves

A typical crosstalk scheme using noise rejection curves is illustrated in Fig. 6. For every victim in the design a valid set of aggressors is identified. The victim-aggressor RC circuit is solved for the crosstalk pulse on the victim which is then compared to the receiver noise rejection curve for violation determination. In this normal flow the noise rejection curves are either based on SSB assumption or SSW assumption. For our proposed methodology we use SSB assumption, and further analyze the nets that are filtered for possible multiple noise event failure. Note that a violation with SSB NRC is a valid violation since multiple events would only increase the noise on the failing victim. The flow in Fig. 6, is therefore modified as follows:

1. identify the nets that are filtered from existing analysis and have receivers such as nand, nor, aoi,oai, etc.,
2. determine the number of inputs that can have a crosstalk event for every receiver by aligning aggressor timing windows,
3. degrade the noise rejection curve and determine the violation.

The problem is now reduced to determination of a model that would predict the degradation in noise rejection curve given a gate and the number of its input experiencing the noise events.

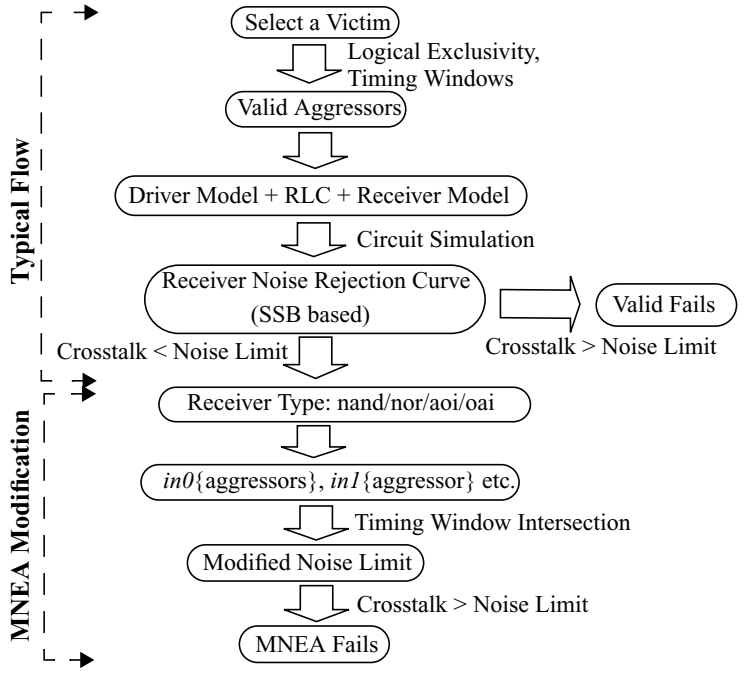

Fig. 6. MNEA Crosstalk Analysis with NRC

3.1 Noise Limit Degradation Model

For a given technology, the noise limits of gates with parallel FETs like aoi, oai, nand, nor etc. can be modeled using the noise limit with SSB assumptions. The new degraded noise limit, $V_{NL}^{'}$, can be derived using a simple exponential formulae given by:

$$V_{NL}^{'} = V_{NL}\left(e^{-\alpha_{nrc}N}\right). \quad (1)$$

where V_{NL} is the SSB noise limit, α_{nrc} is the curve fitting constant ($0<\alpha_{nrc}<1$) and N is the number of gate inputs experiencing identical noise events simultaneously.

The factor α_{nrc} is a constant for a circuit in a technology. It can be determined by simulating the circuit with multiple noise events during gate pre-characterization and stored in the receiver model. Determination of α_{nrc} has the overhead of only a single extra simulation per gate type from the current pre-characterizations. In our experiments we found that α_{nrc} varies with gate topology and the FET beta ratio but is independent of actual FET size. To illustrate the model accuracy we simulated a nand4 circuit in 65nm bulk CMOS technology with Spice for a noise pulse of a fixed width (600ps) and a fixed typical output load (fanout 4x).

Table 1. Nand4 Spice Vs Model High-Up Noise Limit

Number of Inputs Switching	Spice Noise Limit	Modeled Noise Limit	%Err
2	24.9%Vdd	24.2%Vdd	-2.8%
3	21.4%Vdd	20.9%Vdd	-2.3%
4	19.2%Vdd	18.0%Vdd	-6.3%

The simulation is repeated for increasing number of inputs experiencing a noise event. The noise limits measured are listed in Table 1 along with the corresponding model predicted values, the error is less than 10%. Fig 7 shows the spice simulated

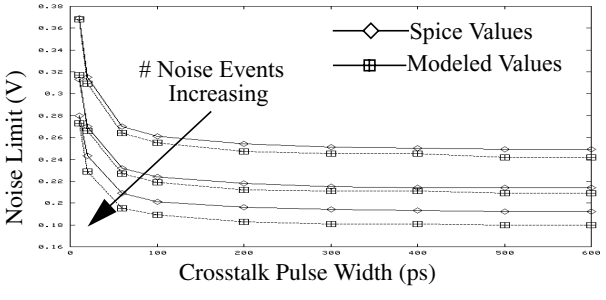

Fig. 7. Nand4 Noise Limit: Spice Vs. Model

and model predicted noise limit values for a nand4 for a range of noise pulse widths as the number of multiple noise events is increased. The data shows a good agreement between the model predictions and spice measurements.

3.2 Multiple Noise Event Aware (MNEA) Crosstalk Analysis Results

We applied the proposed MNEA crosstalk analysis incorporating the proposed noise limit model to industrial microprocessor core and blocks designed in 65nm bulk CMOS technology. The results are listed in Table 2 for original analysis with SSB and SSW assumptions, the proposed MNEA methodology and spice simulations based true violations.

As expected, a large number of violations are reported by SSW flow for all designs. The SSB analysis reports violations less than the Spice reported true violations. The MNEA analysis reduces the number of false violations (*Reduced False Violation factor*) in all cases by 68%-93% with respect to SSW. The MNEA analysis does not eliminate all false violations due to the fact that, the noise limit degradation model assumes that all multiple crosstalk events are identical, whereas in real design, different inputs would experience different crosstalk pulses. This difference is accounted for in the following sections with crosstalk flow based on noise propagation table models.

Table 2. MNEA Crosstalk Analysis Results

Block	Total Nets	SSB	SSW	MNEA	Spice	%RFV
Core	335,282	0	2295	741	454	84%
Blk1	10,386	1	124	45	8	68%
Blk2	103,824	0	487	84	53	93%
Blk3	31,360	0	1470	278	141	90%
Blk4	317,729	11	2851	898	471	82%

4 Crosstalk Analysis with Noise Propagation Tables

The quality of crosstalk analysis results discussed in previous section can be improved by using a topological sort scheme as illustrated in Fig 8. In this scheme all the interconnects and respective receivers in a logical path (terminating into a latch) are identified. The analysis is done such that for each interconnect, the crosstalk pulse is the aggregate of the computed crosstalk pulse and the propagated pulse along the logic path. The violation determination is done when the aggregate crosstalk pulse at the input of a latch results in changing its storage value. This scheme is complex in execution and it is difficult to correct the violations identified. A slightly modified version of this scheme utilizes propagation through the receiver and one logic stage

following the receiver. This provides the benefit of attenuation through the receiver gates and hence, reduces the false violations. In addition the violations are easily identified for correction since only two stages of logic is traversed.

We propose the following enhancements to the typical SSB propagation analysis to make it a MNEA propagation methodology:

1. identify the filtered nets with receivers such as aoi, oai, nand, nor etc.,
2. for each such receiver identify the inputs that can have multiple noise events by aligning the aggressor timing windows,
3. propagate crosstalk pulse taking all noise events into account and determine violations.

Similar to NRC characterization, the gate crosstalk propagation table simulations can be done with SSB or SSW assumptions. The MNEA analysis requires determination of crosstalk propagation given more than one crosstalk pulse at the gate inputs. Analogous to NRCs, the propagation through a gate increases with multiple noise events and it also demonstrates the principle of diminishing returns with each successive crosstalk event. We propose a propagation model given the gate propagation based on SSB assumptions in the following section.

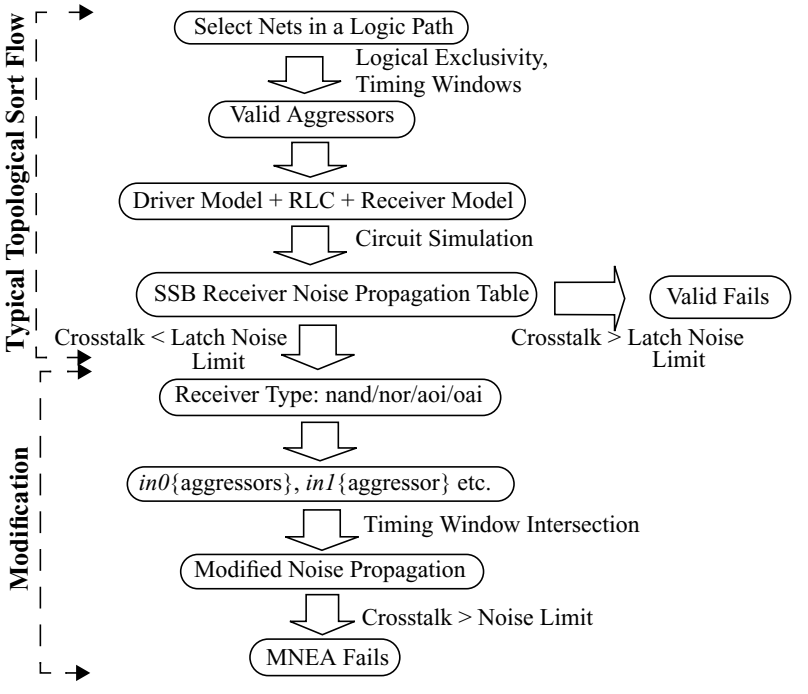

Fig. 8. MNEA Crosstalk with Appreciation Model

4.1 Noise Propagation Appreciation Model

If for a given gate the SSB propagation in known for an input then, the effect of multiple noise events on side inputs is to increase the crosstalk propagation through the gate. We propose the following formula for predicting the propagation, V_{pknew} as follows:

$$V_{pknew} = \sum_{i=0}^{N} V_i \cdot e^{i \cdot \alpha_{prop.}} \tag{2}$$

where, V_i is the propagated peak for an input i with SSB assumption. The constant α_{prop} is the curve fitting parameter. It can be obtained by simulating each gate type for a set of input pulses and propagated noise pulse. The index i is obtained by sorting the input crosstalk propagated pulses such that $i=0$ corresponds to the largest crosstalk pulse width and $i=N$, the smallest. For example for a nand2 with two inputs *in0* and *in1*, with crosstalk propagated pulses: (200mV, 500ps) and (300mV, 200ps) respectively. The new propagated pulse for *in0* would be given by:

$$V_{pknew} = 200 \cdot e^{0 \cdot \alpha_{prop}} + 300 \cdot e^{1 \cdot \alpha_{prop.}} \tag{3}$$

To estimate the accuracy of the model various spice simulations were done on different gate types. The crosstalk pulses on different inputs were assumed to differ in pulse height and width, the pulse width was varied from 20ps to 500ps and the noise height was varied from 50mV to 500mv. Spice simulated propagated noise and model predicted noise propagation are listed in Table 3. The error is within 10% unless one

Table 3. Multiple Noise Event Propagation Model Vs. Spice Results

Gate	#Inputs	SSW	SSB	MSW V_{pknew}	Spice V_{pk}	Err
nand3	2	0.982	0.231	0.265	0.264	0.3%
nand3	3	0.982	0.325	0.459	0.445	3%
nand4	2	0.640	0.126	0.150	0.128	17%
nand4	4	0.640	0.288	0.378	0.324	17%
nor3	2	0.566	0.410	0.470	0.468	0.4%
nor3	3	1.235	0.819	1.158	1.052	10%
aoi12	2	1.06	0.471	0.672	0.669	0.4%
oai12	2	1.02	0.543	0.966	0.817	18%

or more crosstalk noise pulses have a very small height. The data points in Table 3.with error larger than 10% correspond to multiple crosstalk events comprising of one or more crosstalk pulses with very small pulse heights.The table also shows the corresponding SSB and SSW predicted noise propagation.

4.2 MNEA Propagation Crosstalk Analysis Results

A 65nm technology microprocessor core and design blocks were analyzed for crosstalk with SSB propagation, SSW propagation and the proposed MNEA propagation. The results are shown in Table 4.

Table 4. MNEA Crosstalk Analysis Results

Block	Total Nets	SSB	SSW	MNEA	Spice	%RFV
Core	335,282	0	303	40	34	98%
Blk1	10,386	0	7	0	0	-
Blk2	103,824	0	60	5	4	97%
Blk3	31,360	0	104	10	8	98%
Blk4	317,729	0	159	46	34	90%

The proposed MNEA analysis reduced the number of false violations by 98%, demonstrating improvement over the MNEA with NRC degradation. Note that the SSB assumption filters all real violations. Also note that the number of violations with propagation reduces when compared to NRC criterion violations in Table 2.

5 Conclusions

In this paper we demonstrated the need for multiple crosstalk events aware crosstalk analysis schemes due to increasing system frequency. The potential of multiple noise events aligning in time to create a functional violation is a real possibility not addressed efficiently by current crosstalk analysis and receiver models. We proposed modification to NRC and propagation based crosstalk analysis such that the false violations were reduced by 68%-98%. Our proposed changes also reported all true violations possible as a result of multiple crosstalk events.

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