Power Management Issues in High Performance Processor Design

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Abstract

With the growing demand for portable applications, low power processor design is increasingly common. In addition to power requirements, processors also have very stringent performance requirements. These conflicting goals present the designer with a challenging problem. In order to effectively reach an optimal trade-off between performance and power, a number of mature design methods and design tools are needed. The most prominent and mature low power design tool is a power simulator. Power simulation can be performed at the transistor level, gate level, or RTL level. Each additional level of abstraction increases the performance of the tool but reduces the accuracy of the power estimate.

The drive for lower power, as well as process shrink, have led to aggressive reductions in the supply voltage. As a result, to maintian performance, the current needed to supply the chip with power is increasing. Due to the resistance of the interconnect, a small voltage drop develops as the power grid supplies current to the circuitry on the chip. Since the current drawn by the devices fluctuates with time, the voltage delivered to the devices fluctuates. The voltage drop and voltage fluctuation results in a number of problems, such as degraded or unreliable performance, noise injection into the signal lines of the circuit, and electro-migration and reliability concerns.

With the increased use of battery operated devices, standby current is become an important constraint for chip designs. Most portable devices spend the majority of their time in standby mode, during which the system clock is inactive. In this mode, current drawn by the device is due to the static leakage current of the gates in the circuit. Although the magnitude of this current is several orders of magnitude lower than the active current during normal operation, the standby current typically dominates battery life due to the large portion of time that the device spends in standby mode. With the reduction of the supply voltage, the threshold voltage (Vt) of the devices is reduced to maintain proper scaling for performance. With the reduction of Vt, the sub-threshold leakage current of the device increases exponentially, causing the leakage current of devices to be a major concern in new portable chip designs.

In this presentation, we give an overview of traditional power simulation tools and discussed two emerging power management design technologies: power distribution integrity analysis and standby current measurement and optimization. We present methods for accurate peak current simulation, which is needed for power grid integrity analysis, and discuss the generation and compression of the simulation vectors. Standby leakage current is state dependent and we present methods for calculating both the average and maximum leakage current. Finally, optimization methods for minimizing the leakage current by are discussed.