A sub-pW timer using gate leakage for ultra low-power sub-Hz monitoring systems

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Abstract- **In this work, we present a novel ultra-low power timer designed using the gate leakage of MOS capacitors. The test chip was fabricated in a 0.13μm CMOS technology and the total circuit area is 480μm^2. Measurement results show that the circuit functions correctly at a wide range of supply voltages from 300mV to 1.2V, making it particularly suitable for subthreshold systems. The temperature sensitivity is 0.16%/°C at 600mV and 0.6%/°C at 300mV. The power dissipation is less than 1pW running at 20°C and 300mV.**

I. Introduction

The continuing advancement of silicon technology is the driving force creating more powerful integrated circuits, including microprocessors. As the physical dimensions of microprocessors shrink, more functionality can be packed into a single die with reasonable costs. In this paper, we propose an ultra-low power timer intended for an intraocular pressure monitoring system targeting glaucoma patients, shown in Fig. 1. Periodic monitoring of eye pressure is done by taking measurements each hour and requires roughly 1000 cycles for the processor to read, compress and store data into the memory. Thus, the system needs to be shutdown through both power gating and clock gating in order to save energy when not in use. Previous work shows the potential of achieving energy levels of a few pJ per instruction using subthreshold circuit design [1]. A timer that consumes negligible power compared to the idle power of the rest of system (which maybe on the order of nW) is a critical component to awaken the processor when it needs to measure and record new data.

Crystal oscillators are generally the ideal candidate to obtain absolute timing information in terms of process, supply, and temperature sensitivity. Typically incurring a bulky external component, it can also be implemented with a Colpitts oscillating circuit on-chip [2]. However, the resulting power consumption is larger than 1μW and the area is large compared to the rest of the system. A current controlled one-hot timer has been proposed to provide steady output frequency with

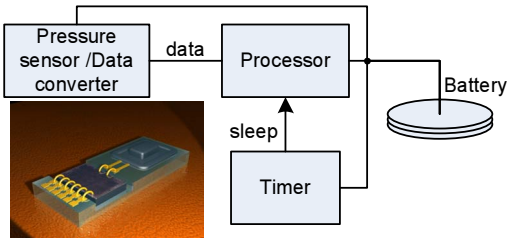


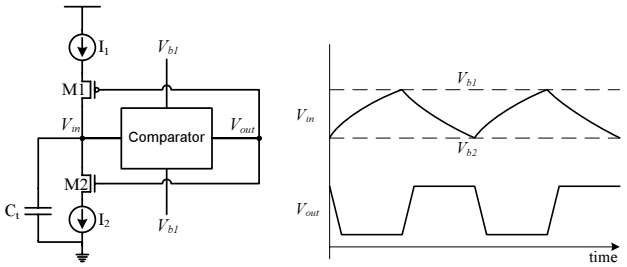
Figure 1: Intraocular pressure monitoring system diagram and mock-up with timer that periodically awakens the processor.

a circuit that combines a Schmitt trigger and a charge pump [3, 4]. For a given time the charge pump provides a fixed amount of charge to the load capacitance and the output will eventually flip when the voltage level exceeds the transition point of the Schmitt trigger. The design of the current source has a direct impact on the frequency sensitivity of the circuit. However, in the subthreshold regime, drain current is exponentially related to temperature. Therefore, it is difficult to maintain constant current output at such a stringent power budget. On the other hand, gate leakage is known to be much less sensitive to temperature [5]. In this work we demonstrate a circuit that takes advantage of gate leakage current to implement a ultra low power watchdog timer.

The remainder of the paper is organized as follows. We first show the general concept and design of our proposed timer in Section II. Measurement results from a 0.13μm CMOS test chip are described in Section III. We conclude our work in Section IV.

II. Design for low power timer

Fig. 2(a) shows the typical concept of the previously mentioned one-hot timer design [3, 4]. A comparator with two bias voltages V_{b1} and V_{b2} is used to flip the output V_{out} whenever V_{in} exceeds V_{b1} or goes below V_{b2} (Fig. 2(b)). I_1 and I_2 are ideal current sources to charge or discharge V_{in}. Assuming I_1 and I_2 are equal to I_{on}, the frequency of the timer is given by $2I_{on}/(C_t(V_{b1} -$



(a) (b)

Figure 2: Traditional concept of constructing a timer using ideal current source (a) Circuit diagram. (b) timing waveform.

V_{b2})), which is independent of supply voltage.

In practice, the current sources are susceptible to bias condition and temperature if not carefully designed. There are many publications on CMOS temperature-compensated current sources, however none target ultra low power applications [6, 7]. To reduce overall power consumption of the timer, the circuit should be biased in the subthreshold region, further complicating the analog circuit design. Implementing the comparator is another challenge since V_{b1} and V_{b2} need to be process, temperature and voltage independent as well. Designing a bandgap reference with a voltage regulator can easily exceed strict power budgets and therefore is not a feasible solution for our application. To reduce the active energy of the timer, it is preferable to run at a very low frequency, just sufficient to awaken the processor in time. This means that either the load capacitor C_t will be very large or the current source must consume very little current in order to achieve a large RC constant.

A circuit using gate leakage can be used to replace the current sources I_1, I_2 in Fig. 2(a). For CMOS technology, gate oxide thickness continues to shrink to maintain good channel control and drive current at reduced channel lengths and supply voltages. Therefore, tunneling-based gate leakage becomes non-negligible compared to other leakage sources. Gate leakage is the sum of many different tunneling currents such as the electron tunneling from the conduction band (ECB), electron tunneling from the valance band (EVB), and hole tunneling from the valance band (HVB). In general, gate current density has the following form [8]

$$J_g = A \cdot T_{oxratio} \cdot \frac{V_g \cdot V_{aux}}{t_{ox}^2} \cdot \exp\left[-B(\alpha - \beta|V_{ox}|)(1 + \gamma|V_{ox}|)t_{ox}\right] \quad (1)$$

where $A = q^2/8\pi h\phi_b$, $B = 8\pi\sqrt{2qm_{ox}}\phi_b^{3/2}/3h$, m_{ox} is the effective carrier mass in the oxide, ϕ_b the tunneling barrier height, t_{ox} the oxide thickness, and V_{aux} is a fitting function of the tunneling carrier density and available states. V_{aux} is a weak function of temperature and has the following form

$$V_{aux} = NIGC \cdot v_t \cdot \log\left(1 + \exp\left(\frac{V_{gs\_eff} - V_{th0}}{NIGC \cdot v_t}\right)\right) \quad (2)$$

Typical temperature sensitivity for gate leakage is 10% per $10°C$, which has a much lower temperature sensitivity than subthreshold leakage. Another advantage of using gate leakage is its small magnitude compared to transistor saturation current (e.g., in 0.13μm CMOS a typical gate leakage is on the order of 10s of pA/um [[9]]). The active energy can therefore be reduced both by the sub-Hz oscillating clock as well as lower charging current based on gate leakage.

The comparator function is implemented with a CMOS Schmitt trigger for simplicity. The hysteresis nature of a Schmitt trigger is often used to suppress signal noise [10]. The low-to-high transition voltage V_{M+} and high-to-low transition voltage V_{M-} are defined as the 2 crossover points in the voltage transfer characteristic; i.e., when the input voltage V_{in} equals the output voltage V_{out}. In this work, V_{M+} and V_{M-} are the equivalent of V_{b1} and V_{b2}, respectively. The advantage here is that since V_{M+} and V_{M-} are circuit parameters, there is no need to generate extra bias voltages.

Based on the previous discussion, our proposed timer is shown in Fig. 3. The Schmitt trigger inverter contains transistors MS1 through MS6. When operating at superthreshold, V_{M+} can be determined when MS1, MS2 and MS5 are all in saturation. With $I_{MS1} = I_{MS2} + I_{MS5}$, and assuming that the channel length modulation effect is negligible, V_{M+} can be found as a function of V_{th} and $V_{x,tran}$

$$V_{M+} = V_{x,tran} \cdot \left(\frac{\sqrt{k_2 + k_5} - \sqrt{k_1}}{\sqrt{k_2 + k_5} - \sqrt{k_1}}\right) + V_{th} \quad (3)$$

where $V_{x,tran}$ is the voltage V_x in Fig. 3 when V_{M+} occurs. From simulation results, we know that $V_{x,tran}$ is nearly constant when temperature varies. Therefore, the temperature impacts V_{M+} in the same way it affects V_{th}. The transition voltage for the Schmitt trigger decreases as the temperature rises. V_{M-} can be computed in the same way. Our simulation results show that at 300mV, $\Delta V_M = V_{M+} - V_{M-}$ reduces 0.1%/°C due to the lower on-off current ratio in subthreshold. This results shows adequate temperature dependency using the Schmitt trigger.

INV1 and INV2 are inverters to provide sharper transition for the timer and stack-forced to reduce leakage power. The clock output is buffered again from the

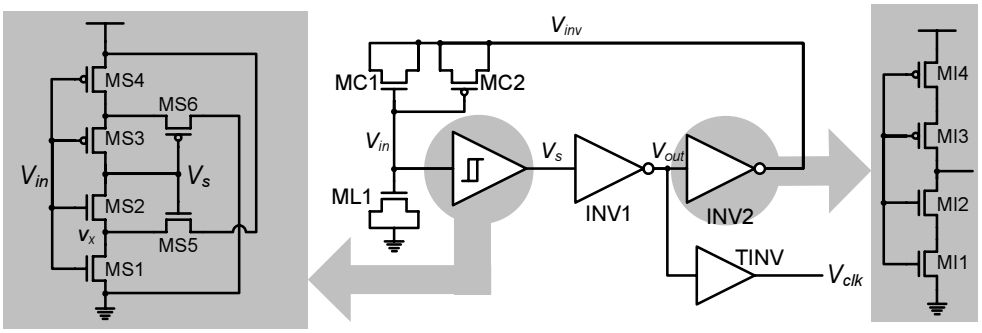


Figure 3: Proposed timer structure for subthreshold operation

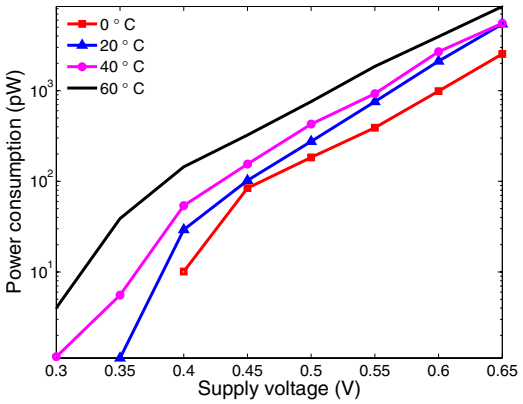


Figure 4: Power consumption vs. supply voltage at different temperature points

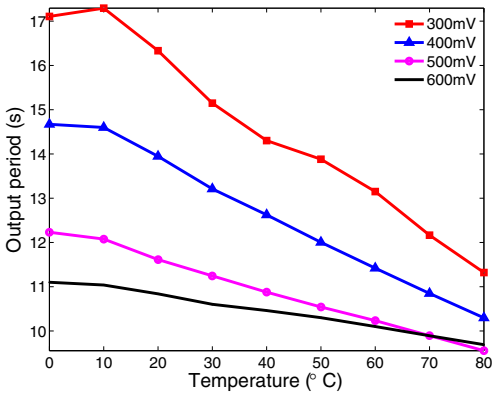


Figure 5: Timer period vs. temperature at various supply voltages.

loading by TINV to isolate any possible noise from the system. MC1 and MC2 are thin oxide MOS capacitors used to replace the current source mentioned before. Both PMOS and NMOS capacitors are used to provide comparable charging/discharging strengh. The load capacitance ML1 is implemented with a thick gate oxide transistor, which are commonly available in modern CMOS processes, to avoid unwanted gate leakage to ground. The corresponding waveform of V_{in} and V_{out} also illustrated with Fig. 2(b). When V_{out} is pulled up, V_{inv} is pulled down to discharge V_{in} through MC1 and MC2 until V_{in} is lower than V_{M-} of the Schmitt trigger, and vice versa. V_{clk} is the input signal to digital counter that is configurable by the system to decide the number of timer ticks before awakening the processor.

III. Measurement results

The chip was implemented in a commercial 0.13μm digital CMOS process. The total circuit area is approximately 480 μm^2 where half of the area is allocated to the load capacitor ML1. Fig. 4 plots the power consumption of timer as a function of both Vdd and power. At 300mV, the power consumption of the timer is less than 1pW at 20°C and it consumes roughly 2nW at 600mV measured by Keithley 6217 electrometer.

Fig. 5 shows the timer output period measured at different supply voltages and temperatures. The timer is more temperature insensitive at higher supply voltages, largely due to the fact that the impact of ΔV_M, is minimized at the superthreshold region. Similarly, the variation due to supply voltage is also reduced at higher Vdd for the same reason. The measured temperature sensitivity is 0.16%/°C at 600mV and is 0.6%/°C at 300mV; supply sensitivity is 0.15%/mV from 300mV to 500mV and 0.04%/mV at 600mV, the lower figure at 600mV is specifically due to operating in the superthreshold region. For in-tissue biomedical sensor-type applications, temperature normally will not deviate more than a couple degrees and the temperature sensitivity is adequate. Also, for a system containing a temperature sensor, updated temperature information can be obtained when the processor wakes up and the number of sleep clock cycles can be adjusted the next time the system goes to sleep.

Within-die and die-to-die process variation is a significant concern in advanced VLSI technologies. We

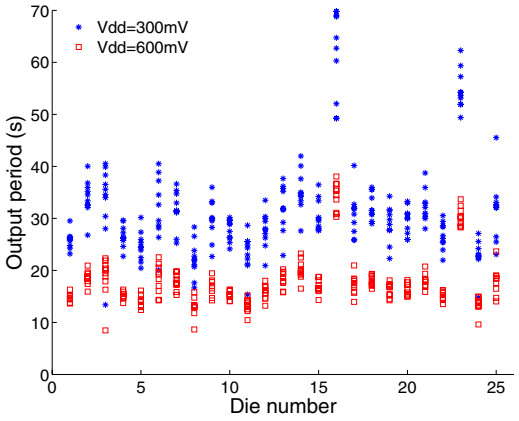


Figure 6: Output period scatter plot highlighting die-to-die and within-die variations.

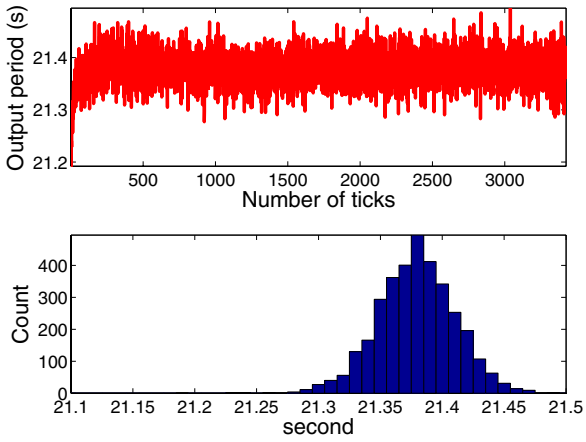


Figure 7: Timer output period variation with respect to time.

measured ten timers (2x5) in each of 25 dies and plot the output period in Fig. 6. To characterize die-to-die variation, we first compute the mean for each die and obtain σ/μ across all 25 dies. Die-to-die variation is 28% and 27% at supply voltage of 300mV and 600mV respectively. Within-die variation is obtained by taking the average of σ/μ within individual die and is measured at 12.4% and 9.2% for 300mV and 600mV. Key sources of variation includes oxide thickness variation and the voltage shift of Schmitt trigger trip points V_{M+} and V_{M-} due to transistor mismatch. In general, the variation can be calibrated by adjusting the aforementioned counter. The processor can easily configure the number of counts between the readings by preloading digital values.

We also tested the proposed timer by running it continuously for 20 hours to measure timing stability over an extended period. Measurement results over time along with the resulting histogram are shown in Fig. 7. It takes approximately ten minutes for the timer to reach steady state, after which the output frequency is always within 1% throughout the remaining 20 hours of testing. The rms *jitter* for this timer is 30ms, equivalent to 0.14% of the output period.

IV. Conclusion

In this work, we designed and tested a new watchdog timer that can be easily integrated into a sensor-type system due to its compact size. In addition, since the timer uses gate leakage as the charging/discharging source, the operating voltage can range from 0.3V to 1.2V in order to adapt to different sensor system power consumption restrictions. For systems containing temperature sensors, the timer can be recalibrated upon wake-up, allowing operation at 0.3V with less than 1 pW power consumption.

Acknowledgement

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References

[1] B. Zhai et al. A 2.60pj/inst subthreshold sensor processor for optimal energy efficiency. In *2006 Symposium on VLSI Circuits*, pages 154–155, June 15-17, 2006.

[2] K. Hosaka, S. Harase, S. Izumiya, and T. Adachi. A cascode crystal oscillator suitable for integrated circuits. In *Frequency Control Symposium and PDA Exhibition, 2002. IEEE International*, pages 610–614, 29-31 May 2002.

[3] R. Woudsma and J.M. Noteboom. The modular design of clock-generator circuits in a CMOS building-block system. *Solid-State Circuits, IEEE Journal of*, 20(3):770–774, Jun 1985.

[4] H. Okuno et al. A programmable clock oscillator for integrated sensor applications. In *Electron Devices Meeting, 1998. Proceedings., 1998 IEEE Hong Kong*, pages 1075–1077vol.1, 29 Aug. 1998.

[5] M. Klein. Static power and the importance of realistic junction temperature analysis. Technical report, Xilinx, Aug 2005.

[6] C.-H. Lee and H.-J. Park. All-CMOS temperature independent current reference. In *Electronics Letters*, volume 32, pages 1280–1281, 4 July 1996.

[7] J. Georgiou and C. Toumazou. A resistorless low current reference circuit for implantable devices. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, volume 3, pages III–193–III–196vol.3, 26-29 May 2002.

[8] K.M. Cao et al. BSIM4 gate leakage model including source-drain partition. In *Electron Devices Meeting, 2000. IEDM Technical Digest. Intl.*, pages 815–818, 10-13 Dec. 2000.

[9] Chang-Hoon Choi, Ki-Young Nam, Zhiping Yu, and R.W. Dutton. Impact of gate direct tunneling current on circuit performance: a simulation study. *Electron Devices, IEEE Transactions on*, 48(12):2823–2829, Dec. 2001.

[10] M.J.S. Smith and J.D. Meindl. Exact analysis of the schmitt trigger oscillator. *Solid-State Circuits, IEEE Journal of*, 19(6):1043–1046, Dec 1984.