Short Papers

A Library Compatible Driver Output Model for On-Chip RLC Transmission Lines

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***Abstract*—This paper presents a new library-compatible approach to gate-level timing characterization in the presence of resistive/inductive/capacitive (RLC) interconnect loads. We show that for a gate driving an RLC interconnect, the driver-output waveform exhibits inflection points and, hence, the traditional approach of approximating driver output with a saturated ramp is highly inaccurate. We describe a two-ramp model based on transmission-line theory that accurately predicts both the 50% delay and waveform shape (slew rate) at the driver output when inductive effects are significant. The approach does not rely on piecewise linear Thevenin voltage sources and is compatible with existing library characterization methods. Results are compared with SPICE and demonstrate typical errors under 10% for both delay and slew rate. We also propose a new criterion for evaluating the importance of on-chip inductance by comparing rise time at the driver output with the time of flight.**

***Index Terms*—Inductance, interconnect, timing.**

I. Introduction

With higher clocking frequencies, longer and wider global interconnects and faster signal rise times, on-chip inductive effects have become significant in today's high-performance deep-submicron designs. These inductive effects are concerns for signal integrity and overall interconnect performance and must be accounted for during timing analysis.

Existing gate-level static timing analyzers break down the path delay into gate delay and interconnect delay. Gate delays are precharacterized in terms of input transition time and output load capacitance using detailed circuit simulators such as SPICE. In reality, the gate drives an *RC*/resistive/inductive/capacitive (RLC) load and, hence, the incompatibility that exists between precharacterized look-up tables and *RC*/RLC loads is resolved by finding an effective capacitive load seen by the gate. This requires synthesizing a reduced order driving point model, which is then mapped to an *"effective capacitance"* value. O'Brien and Savarino [1] synthesized a pi-model for *RC* loads by matching the first three moments of the driving point admittance and Pillage *et al.* [2] presented an effective capacitance model for this pi-load. It has been shown that, with the introduction of inductance, the pi model cannot be synthesized [3]. A ladder-type model is presented in [3] that assures the realizability of a reduced-order circuit by introducing a realizability parameter k. However, no physical explanation is given for k and no approach is described to map this model to an effective capacitance.

Another issue with inductance is that the driver-output waveform may be nonmonotonic and frequently exhibits inflection points. Traditionally, static timing analysis tools compute delay and rise time at the output of a gate using its precharacterized look-up table. The gate output is then approximated with a saturated ramp and this ramp is used to derive the far end response of the interconnect. While this approach usually works well for *RC* lines, it fails for RLC lines because the output waveform of the driving gate cannot always be well modeled by a single ramp [4].

In this paper, we develop a methodology to enable the complicated inductive waveforms at driver output to be modeled by using simple traditional precharacterized look-up tables. Our approach computes the effective capacitance for RLC interconnects by using their driving point admittance moments. The idea of using driving point admittance moments directly (instead of mapping them to a reduced order pi model) was introduced in [5]. However, unlike their approach, the proposed methodology is compatible with existing cell characterizations and does not require modeling of cells with piecewise linear Thevenin voltage sources. Also, our approach models the driver output waveform directly as compared with the approach in [5], which requires a SPICE or PRIMA run (with a piecewise linear Thevenin voltage and series resistance driving an RLC line) to compute the driver output response. We also show that, with dominant inductive effects, a single ramp cannot model the entire driving point waveform accurately and at least two ramps should be computed to capture both the delay and slew. It has been shown that with significant resistive shielding, even *RC* lines cannot be modeled as single ramps and a gate resistor model is used to capture its long exponential tail [2]. However, inductive cases are unique since the output waveform of the driver exhibits a kink (and sometimes a flat plateau) due to transmission line effects. This kink, which causes a clear slope change, occurs in all inductively dominated lines and can be captured by the proposed two-ramp model based on transmission line theory. We synthesize this two-ramp waveform by finding two effective capacitances. In the process, we propose a new criterion for evaluating the importance of on-chip inductance. Our method compares rise time at the driver output with the time of flight instead of taking the rise time at the input to the driver as in [6].

The paper is organized as follows. We begin by reviewing some basic properties of inductive lines and transmission line theory in the following section. Sections III and IV present our modeling approach to capture the inductive waveforms at the driver output. Section V summarizes our modeling flow. Section VI shows experimental results and we conclude in Section VII.

II. Driver-Output Waveform With Inductance

It is known that with significant inductance the driver output waveform is no longer smooth as in *RC* cases and exhibits inflection points. Fig. 1 shows the driver output waveform of an RLC line driven by a 75X inverter.[1] It is clear from the figure that the waveform is not smooth and shows kinks during the transition.

This behavior can be explained based on reflections in a transmission line. For fast drivers, transmission line effects become significant since the rise time of the signal is less than or comparable to the signal's time of flight delay [7]. At the source end of the line, the driver resistance and the line impedance divide the input voltage, giving an initial voltage step. This initial voltage step travels down the line and is reflected at the far end of the line. In typical CMOS designs, the receiver has a small input capacitance that leads to a reflection coefficient of

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[1]Here, driver size 75X means the NMOS width in the inverter is 75 times the minimum width ($= 2^{*}\mathrm{L}_{\min} = 0.36\ \mu$m). PMOS is twice as wide as NMOS.

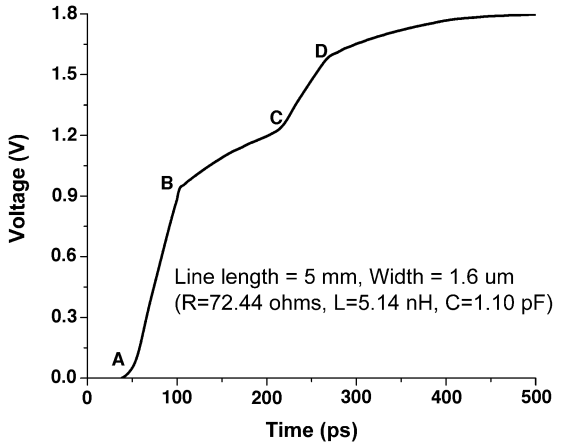

Fig. 1. Driver-output waveform of a 5-mm RLC line driven by a 75X inverter. The waveform has three distinct pieces: AB, BC, and CD. AB is the initial step, BC is the plateau, and CD is the step due to first reflection.

around $+1$ at the far end [8]. Hence, the forward traveling initial step is almost completely reflected at the far end. The voltage at the far end of the line is nearly doubled due to the superposition of the incident initial step and the reflected reverse wave. The reflected wave returns to the source after two time-of-flight delays and adds to the initial step at the driver output. If the driver resistance does not match line impedance, this reverse wave itself can reflect off the source leading to multiple reflections. If the driver is weak and its output impedance is high, then multiple reflections are required to take the line to $\mathrm{V_{DD}}$. But if the driver resistance is equal to the line impedance, we obtain an initial half-amplitude step at the source end of the line and only one reflection is needed to take the line to the switching point. Fig. 2 shows the reflection phenomena in an ideal lossless transmission line driven by a step voltage. The figure shows the waveforms for the cases when the source impedance is less than, equal to, and greater than the line impedance. The reflection coefficient at the far end of the line is assumed to be $+1$.

We have seen that, due to transmission line effects, the driver-output waveform rises to an *initial step* and then shows a *plateau* while waiting for reflections from the far end to return. Once a reflection from the far end comes back to the driver, the waveform rises to another step due to this reflection. This pattern of plateaus and steps (due to reflections) is continued until the waveform has risen fully to the supply voltage. For example, in Fig. 1, AB represents an initial ramp, BC is the plateau, and CD is the ramp due to the first reflection. Beyond point D, the plateaus and reflections are not clearly visible because the signal is near its final value of $\mathrm{V_{DD}}$.

From the above discussion, it is clear that modeling the driver-output waveform as a single ramp or even an exponential wave can lead to large errors in delay and slew prediction at the near as well as far end. When the wires are driven by strong buffers and inductive effects are significant, the waveforms exhibit transmission line effects and a better model of the driver output waveform is necessary for accurate timing analysis.

III. Modeling Driver Output Waveform

The ratio of the signal rise time to the time of flight delay can be related to the ratio of the source resistance of the driver to the characteristic impedance of the line [7]. At the driver end, the transmission line can be modeled as a source resistance in series with the characteristic line impedance. In this case, we have a simple voltage divider and the ratio of the source resistance to the line impedance determines the size of the initial step generated on the line.

If the driver resistance is $\mathrm{R_s}$ and the characteristic line impedance is $\mathrm{Z_0}$, the height of the initial step during the transition is given by the following expression:

$$\text{Height of initial step} = {V_{\mathrm{DD}}}^{*} f, \qquad \text{where } f = \frac{Z_0}{Z_0 + R_S}. \tag{1}$$

For weak drivers, the driver resistance is much larger than the line impedance and the rise time is much larger than the time of flight. This causes reflections to come back to the source end even before the output has risen to the initial step. Thus, the waveform resembles an *RC* line, and transmission line effects are not significant. However, for fast drivers, the initial step is large and clear kinks and plateaus are seen in the waveform.

Based on the transmission line theory above, nonmonotonic driver-output waveforms should ideally be modeled as multipiecewise linear waveforms to capture plateaus and multiple reflections. However, it is shown in [7] that reflections and other transmission line phenomena become important only when the source impedance of the driver is less than or comparable to the characteristic line impedance. This causes the initial step to be greater than 50% of $\mathrm{V_{DD}}$. In such cases, modeling of just the first reflection is sufficient since plateaus and ramps due to later reflections are not visible in the driver-output waveform. In order to model just one reflection, the driver output can seemingly be represented as a three-piece linear waveform. The three pieces would be used to model the initial ramp, the plateau, and the ramp due to the first reflection. For example, in Fig. 1, the three ramps will correspond to the AB, BC, and CD portions of the waveform. However, we point out that the plateau often spreads out so it is almost unnoticeable. Furthermore, even when it is prominent it can be modeled along with the first reflection (CD in Fig. 1) as a single ramp with little loss of accuracy. Hence, we do not require an extra piece for the plateau and the driver output can be modeled sufficiently by two ramps. The first ramp is used, therefore, to model the initial step and the second ramp is used to model the remaining part of the transition. Though modeling inductive waveforms with three or more pieces can fit the waveform better, the two-ramp approach provides greater simplicity with comparable accuracy. As mentioned earlier, in cases with weak drivers and insignificant inductive effects, a single ramp may be sufficient for the entire transition.

A transmission line can have overshoots at the near end and, in this case, a simple two-ramp approximation of the driver-output waveform is inaccurate. However, for all practical very large scale integration applications that we examined, we found that these near-end overshoots are normally negligible and the simple two-ramp approximation is sufficient. Fig. 3 shows near and far-end waveforms of a 4-mm-long and 1.6-μm-wide line driven by a 250X inverter (a large driver is chosen to maximize near-end overshoot). In this case, the source resistance of the driver was only 19.2 Ω compared to the characteristic line impedance of 69 Ω. Even in this scenario, the near-end overshoot is only 2.85% of $\mathrm{V_{DD}}$ compared to 27.2% overshoot observed at the far end of the line.

Some important considerations in two-ramp modeling are to determine the slopes of each ramp and find the breakpoint during the transition. The breakpoint, defined as the point at which the first ramp (initial step) ends and the second ramp starts, can be calculated using (1). The slopes of the two ramps can be found using an effective capacitance-based approach discussed later in this paper.

Using the two-ramp approach, the driver output can be modeled as shown in Fig. 4. The slope of the first ramp is $(\mathrm{V_{DD}}/\mathrm{T_{r1}})$ and the slope of the second ramp is $(\mathrm{V_{DD}}/\mathrm{T_{r2}})$. The two-ramp expression is given by

$$\begin{aligned} V(t) &= V_{\mathrm{DD}} \frac{t}{T_{r1}} && 0 < t < fT_{r1} \\ V(t) &= V_{\mathrm{DD}} \frac{t}{T_{r2}} + kfV_{\mathrm{DD}} && fT_{r1} < t < fT_{r1} + (1-f)T_{r2} \\ \text{where } k &= \left(1 - \frac{T_{r1}}{T_{r2}}\right) \end{aligned} \tag{2}$$

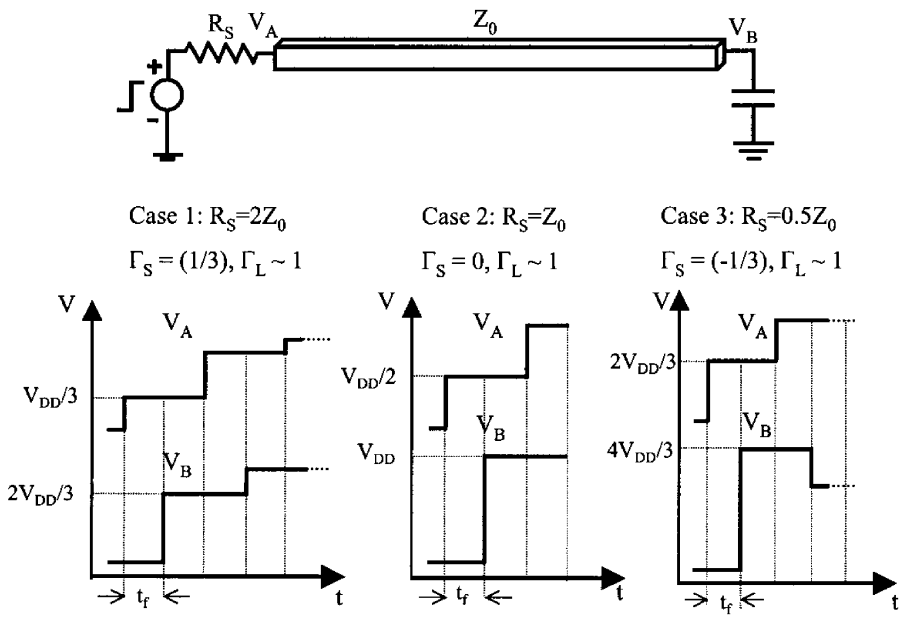

Fig. 2. Reflections in a lossless transmission line for various R_s and Z_0 combinations. Three different values of source resistance are considered. Z_0 is the characteristic impedance of the line, t_f is the time-of-flight, and Γ_S and Γ_L are the reflection coefficients at source-end and far end of the line respectively. Γ_L is assumed to be $+1$.

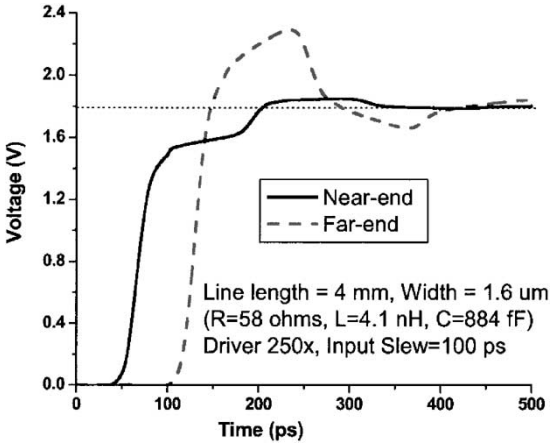

Fig. 3. Near and far-end response of a 4-mm line driven by 250X inverter. Source resistance of the driver (19.2 Ω) is significantly lower compared to the characteristic impedance of the line (69 Ω). Still, overshoot at near-end of the line is almost negligible.

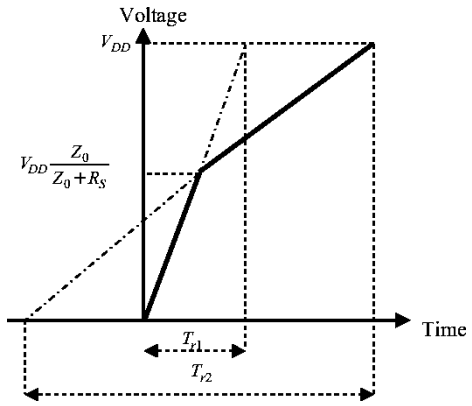

Fig. 4. Simplified two-ramp model of driver-output waveform. Slope of the first ramp is (V_{DD}/T_{r1}), slope of the second ramp is (V_{DD}/T_{r2}), and the breakpoint is $V_{DD}(Z_0/(Z_0 + R_s))$.

We use the above driver-output model in this paper. Our modeling approach is summarized below. The details are discussed in the following sections.

- Find breakpoint using (1).
- Find two effective capacitances (the first effective capacitance models the ramp due to the initial step and the second effective capacitance models the ramp due to the first reflection).
- Model plateau and fit a ramp that captures both the plateau and first reflection.
- Model driver output with two ramps.
- Replace the driver with a voltage source consisting of two ramps and compute the far-end response of the interconnect.

The above flow is compatible with existing precharacterized cell tables that store only 50% delay and output transition time for each input slew and output capacitive load. Our model uses only this information and obtains the double-ramp waveform at the driver output. As mentioned in the modeling flow above, we compute two effective capacitances to model driver output. For each effective capacitance, we use the precharacterized look-up table to compute output slew. The slew corresponding to the first effective capacitance gives the slope of the first ramp and the slew corresponding to the second effective capacitance (along with plateau) gives the slope of the second ramp. Thus, the two-ramp waveform can be computed without changing the existing cell characterization procedure. It may seem that the above approach would require cell characterization to be changed to consider two-ramp input waveforms. However, this is not required because the far-end waveforms that are propagated to the next stage can be modeled by a single ramp (as seen in Fig. 2).

IV. Effective Capacitance(s)

In this section, we show how the two effective capacitances can be calculated to model the driver-output waveform. The underlying principle of our effective capacitance methodology is similar to the approach described in [2]. We calculate effective capacitance by equating the charge transfer required by a single capacitance to that required by the original RLC load. It was shown in [2] that equating the charge up to the 50% point captures delay accurately, but fails in modeling the tail

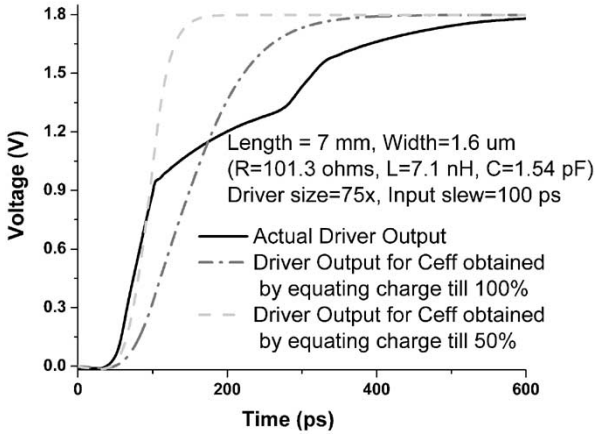

Fig. 5. Driver-output response and C_{eff} approximations obtained by equating charge up to 50% point and over entire transition.

portion of the transition. We have observed that in RLC loads with dominant inductive effects, we regularly see a flattened second half (long tail). Thus, integrating up to the 50% point is always inaccurate as it gives unacceptably large errors in slew (although it may model delay well). Also, equating the charge over the entire region of the transition will not address this problem, since this approach yields an *average* curve, where both the delay and slew may be inaccurate. Fig. 5 shows that equating charge up to the 50% or 100% point can cause significant errors in modeling driver-output waveforms. The equations used to calculate the effective capacitance in this figure are derived later in this section.

This leads to the conclusion that a single effective capacitance cannot accurately model the entire transition. The key idea of our approach is to model the driver-output as a two-ramp waveform as described in Section III. We then find two effective capacitances, where the first effective capacitance models the first ramp and is obtained by equating average charge during the transition of the first ramp. The second effective capacitance models the second ramp and is calculated by equating average charge during the interval when the second ramp is in transition.

The driving point RLC interconnect is modeled using a reduced-order approximation, obtained from matching the moments of the input admittance of the interconnect. We model the driving-point admittance by the following rational function:

$$Y(s) = \frac{a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2}. \tag{3}$$

The above expression is similar to the admittance of an RLC Π load. The coefficients in (3) can be obtained by matching the first five moments of the driving point admittance [13].

A. C_{eff1} Calculation

For the first ramp of the two-ramp waveform described in (2)

$$V(s) = \frac{V_{\mathrm{DD}}}{T_{r1}} \frac{1}{s^2}. \tag{4}$$

The current delivered to the interconnect is given by

$$I(s) = V(s)Y(s) = \frac{V_{\mathrm{DD}}}{T_{r1}} \frac{1}{s^2} \left(\frac{a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2} \right). \tag{5}$$

We need to consider the cases of real and imaginary poles. Let us first assume that the roots of $s^2 + (b_1/b_2)s + (1/b_2) = 0$ are real. Let the roots be s_1 and s_2. Using the inverse Laplace transform, we obtain

$$I(t) = \frac{V_{\mathrm{DD}}}{T_{r1}} \left(a_1 + \frac{a_1 + a_2 s_1 + a_3 s_1^2}{b_2 s_1 (s_1 - s_2)} e^{s_1 t} + \frac{a_1 + a_2 s_2 + a_3 s_2^2}{b_2 s_2 (s_2 - s_1)} e^{s_2 t} \right). \tag{6}$$

We define C_{eff1} to be the capacitance that requires the same charge transfer as that required by the RLC moments during the interval when the first ramp is in transition. From Fig. 4, we know that the first ramp is transitioning from $t = 0$ to $t = f \cdot T_{r1}$, where f is calculated using (1). Charge transferred to the moments can be calculated by integrating $I(t)$ from 0 to $f \cdot T_{r1}$. Also, the charge transfer associated with charging the effective capacitance for this interval is given by $C_{\mathrm{eff1}} \cdot f \cdot V_{\mathrm{DD}}$

$$\int_0^{fT_{r1}} I(t)dt = C_{\mathrm{eff1}} f V_{\mathrm{DD}}. \tag{7}$$

Solving the above equation for C_{eff1}

$$C_{\mathrm{eff1}} = a_1 + \frac{a_1 + a_2 s_1 + a_3 s_1^2}{T_{r1} f b_2 s_1^2 (s_1 - s_2)} \left(e^{s_1 T_{r1} f} - 1 \right) + \frac{a_1 + a_2 s_2 + a_3 s_2^2}{T_{r1} f b_2 s_2^2 (s_2 - s_1)} \left(e^{s_2 T_{r1} f} - 1 \right). \tag{8}$$

Now, let us assume that the roots of $s^2 + (b_1/b_2)s + (1/b_2) = 0$ are imaginary. Let the roots be $\alpha + \mathrm{j}\beta$ and $\alpha - \mathrm{j}\beta$

$$I(t) = \frac{V_{\mathrm{DD}}}{T_{r1}} \left(a_1 + e^{\alpha t} \cos \beta t \left(\frac{a_3}{b_2} - a_1 \right) + e^{\alpha t} \sin \beta t \left(\frac{a_1 b_2 \alpha + a_2 + a_3 \alpha}{b_2 \beta} \right) \right). \tag{9}$$

By equating the charge in a similar way as done for the real roots case, we have

$$C_{\mathrm{eff1}} = a_1 + \frac{1}{f T_{r1}} \left(\frac{a_3}{b_2} - a_1 \right) \int_0^{fT_{r1}} (e^{\alpha t} \cos \beta t)dt + \left(\frac{a_1 b_2 \alpha + a_2 + a_3 \alpha}{f T_{r1} b_2 \beta} \right) \int_0^{fT_{r1}} (e^{\alpha t} \sin \beta t)dt \tag{10}$$

where

$$\int (e^{\alpha t} \cos \beta t)dt = \frac{e^{\alpha t}(\alpha \cos \beta t + \beta \sin \beta t)}{\alpha^2 + \beta^2}$$
$$\int (e^{\alpha t} \sin \beta t)dt = \frac{e^{\alpha t}(\alpha \sin \beta t - \beta \cos \beta t)}{\alpha^2 + \beta^2}.$$

C_{eff1} can be obtained by iterating on T_{r1}. We start with an initial guess of C_{eff1} equal to the total capacitance and iteratively improve the effective capacitance until the value converges. T_{r1} at each step can be obtained from precharacterized cell information and the T_{r1} corresponding to the final C_{eff1} is used to model the first ramp. We now turn to the derivation of expressions for C_{eff2} to complete the two-ramp driving point waveform model.

B. C_{eff2} Calculation

For the second part of the two-ramp waveform described in (2)

$$V(s) = \frac{V_{\mathrm{DD}}}{T_{r2}} \frac{1}{s^2} + \frac{k f V_{\mathrm{DD}}}{s}. \tag{11}$$

We define C_{eff2} to be the capacitance that requires the same charge transfer as that required by RLC moments during the interval when the second ramp is in transition. Using Fig. 4, the second ramp is transitioning from $t = f \cdot T_{r1}$ *to* $t = f \cdot T_{r1} + (1 - f) \cdot T_{r2}$. The charge

transfer to charge the effective capacitance for this interval is given by $C_{\text{eff2}} \cdot (1-f) \cdot V_{\text{DD}}$

$$\int_{fT_{r1}}^{fT_{r1}+(1-f)T_{r2}} I(t)dt = C_{\text{eff2}}(1-f)V_{\text{DD}}. \tag{12}$$

By using a similar approach as for C_{eff1} and considering the case of real and imaginary roots separately, we have the following. For real roots

$$\begin{aligned} C_{\text{eff2}} &= a_1 + Ae^{s_1 fT_{r1}}\left(e^{s_1(1-f)T_{r2}} - 1\right) \\ &\quad + Be^{s_2 fT_{r1}}\left(e^{s_2(1-f)T_{r2}} - 1\right) \\ A &= \frac{\left(a_1 + a_2 s_1 + a_3 s_1^2\right)(kfs_1 T_{r2} + 1)}{(1-f)b_2 s_1^2 (s_1 - s_2)T_{r2}} \\ B &= \frac{\left(a_1 + a_2 s_2 + a_3 s_2^2\right)(kfs_2 T_{r2} + 1)}{(1-f)b_2 s_2^2 (s_2 - s_1)T_{r2}}. \end{aligned} \tag{13}$$

For imaginary roots

$$\begin{aligned} C_{\text{eff2}} &= a_1 + A\int_{fT_{r1}}^{fT_{r1}+(1-f)T_{r2}} (e^{\alpha t}\cos\beta t)dt \\ &\quad + B\int_{fT_{r1}}^{fT_{r1}+(1-f)T_{r2}} (e^{\alpha t}\cos\beta t)dt \\ A &= \frac{1}{(1-f)}\left(\frac{a_3 - a_1 b_2}{b_2 T_{r2}} + \frac{kf(2a_3\alpha + a_2)}{b_2}\right) \\ B &= \frac{1}{(1-f)}\left(\frac{a_1 b_2 \alpha + a_2 + a_3\alpha}{b_2 \beta T_{r2}}\right. \\ &\quad \left. + \frac{kf(a_1 + a_2\alpha + a_3\alpha^2 - a_3\beta^2)}{b_2\beta}\right). \end{aligned} \tag{14}$$

C_{eff2} is obtained by iterating on T_{r2} with an initial guess of C_{eff2} equal to the total capacitance. Typically 3–4 iterations are required for each effective capacitance calculation. The final value of T_{r2} corresponding to the converged C_{eff2} is then used to model the second ramp.

One of the issues involved in using existing gate-characterization techniques to calculate C_{eff2} is that gates are normally characterized for delay and rise time assuming the input signal starts rising from zero at time zero. In our approach, C_{eff2} is evaluated for a region of time in which the input ramp has already reached a value greater than 0 V (a similar argument applies for falling input transitions). Also, when the load changes from C_{eff1} to C_{eff2}, the internal nodes in the driver are already charged to some value. Hence, it seems that using a standard characterization approach could cause errors in C_{eff2} computation. However, our studies found this difference to be very minor (<1% error) and C_{eff2} iterations can be performed using precharacterized look-up tables without loss of accuracy.

As described in Section III, the complete modeling of the driver output requires capturing the plateau along with the initial ramp and the first reflection. We account for the plateau by modifying T_{r2} such that the resulting ramp fits both the plateau and the first reflection. The plateau is difficult to represent because it is not flat and, hence, an intuitive approach of modeling the driver output by a linear ramp, a flat step, and then another ramp, is often inaccurate. We incorporate the effect of a plateau by modifying the second ramp as shown in Fig. 6. The point where the second ramp meets V_{DD} is shifted by the plateau time and a new ramp is fitted as shown in the figure. The new T_{r2} can be obtained by

$$T_{r2\_\text{new}} = T_{r2} + \frac{2t_f - T_{r1}}{(1-f)}. \tag{15}$$

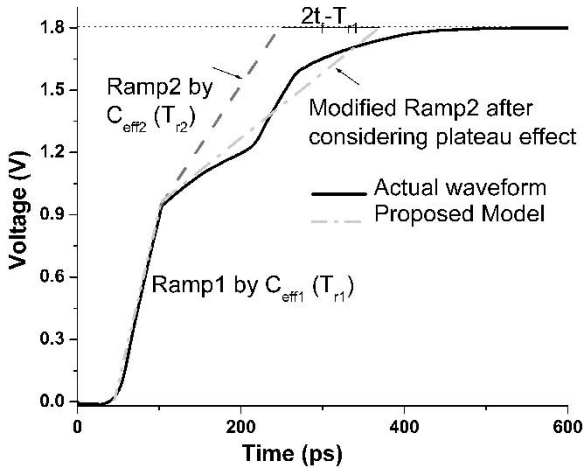

Fig. 6. Summary of the proposed two-ramp approach. The first ramp is modeled by C_{eff1} and the second ramp is modeled by first finding a ramp due to C_{eff2} and then shifting it by the plateau time.

In this equation, t_{f} is the time of flight and $2\text{t}_{\text{f}} - \text{T}_{\text{r1}}$ is the duration of the plateau. The idea behind this approach is that there is no charge transfer during the plateau time $(2\text{t}_{\text{f}} - \text{T}_{\text{r1}})$. Hence, when we calculate C_{eff2} by equating the charge during the second portion of transition, we consider charge transfer after the plateau, but we fail to capture the delay due to the plateau effect. One solution to account for the plateau is to have a flat step for time $2\text{t}_{\text{f}} - \text{T}_{\text{r1}}$ between the two ramps. Another solution is to modify T_{r2} as in (15), where plateau delay is accounted for by shifting the second ramp by the plateau time. The first solution is more accurate when a clear flat plateau exists and the second solution works better when the plateau is not flat and smears out such that it is almost unnoticeable. Experimentally, we have found that the second case occurs more often than the flat case in practice and hence modifying T_{r2} using (15) works better for most cases.

V. Modeling Flow

The two-ramp modeling of the driver-output waveform requires finding the breakpoint (1) and computing two effective capacitances, one for each portion of transition. $\text{T}_{\text{r1}}(\text{C}_{\text{eff1}})$ gives the slope of the initial ramp and $\text{T}_{\text{r2\_new}}(\text{C}_{\text{eff2}})$ gives the slope of the transition after the reflection has come back to the output of the driver. In order to model the breakpoint, we need to find the on-resistance R_{s} of the driver and the characteristic impedance Z_0 of the line. We use a simple approximation of $\text{Z}_0 = \sqrt{L/C}$ in our calculations. On-resistance of the driver is modeled using a similar approach as in Thevenin-based models [10]. We observe the delay between 50% and 90% points of the output waveform and fit an exponential between these points. The on-resistance calculated in this way depends on the load capacitance. We use total capacitance of the line to compute on-resistance. Ideally, one should find an effective capacitance and then calculate on-resistance of the driver for this value of the load capacitance. However, we have seen that the resistance value and, more importantly, the breakpoint do not change significantly by using total capacitance instead of the effective capacitance. Since using the effective capacitance makes this an iterative process, we use the total capacitance to find driver on-resistance in our flow.

In order to validate the approximation used in on-resistance calculation, we considered a 4-mm-long and 1.6-μm-wide line ($\text{R} = 58\ \Omega$, $\text{L} = 4.12$ nH, and $\text{C} = 884$ fF). This line was driven by an inverter whose size was swept from 75 to 250X. The characteristic impedance of the line was 69 Ω. For each driver size, we calculated on-resistance

TABLE I
COMPARING CALCULATED AND MEASURED TRANSITION BREAKPOINTS FOR A 4-mm LINE DRIVEN BY DIFFERENT DRIVER SIZES. LINE IMPEDANCE IS 69 Ω

Driver Size	Calculated driver on-resistance	Calculated breakpoint	Measured breakpoint
75X	58Ω	0.54	0.52
100X	44Ω	0.61	0.62
125X	36Ω	0.66	0.67
150X	30Ω	0.7	0.72
175X	26Ω	0.73	0.76
200X	23Ω	0.75	0.78
225X	21Ω	0.77	0.81
250X	19Ω	0.78	0.82

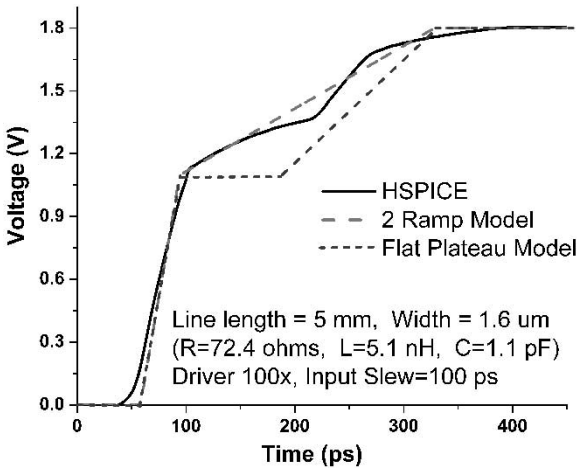

Fig. 7. Two-ramp driver output response and two-ramp with flat plateau response compared to HSPICE for a 5-mm line driven by 100X driver.

of the driver and used this value to calculate the breakpoint during transition. The calculated breakpoint was compared to the value measured from HSPICE simulations. Table I shows this comparison. This table shows that the calculated breakpoint is close to the measured value and, hence, the approximation of using total capacitance to calculate $\mathrm{R_s}$ is acceptable.

When the inductive effects are insignificant, the driver-output waveform looks like an *RC* waveform. In this case, one effective capacitance is sufficient to model the entire transition accurately. This effective capacitance can be calculated by equating the charge over the entire region of transition. We have already derived equations to calculate $\mathrm{C_{eff1}}$; the same equations can be used with $f = 1$ to calculate this single effective capacitance. Usually, a single ramp obtained by this capacitance can model such waveforms very well but if there is significant resistive shielding, the gate resistor model [2] can be used to model the exponential tail of the transition.

We use the following criteria from [6] and [11] to determine the significance of inductive effects:

$$\begin{aligned} C_L &\ll Cl \\ Rl &\leq 2Z_0 \\ R_s &< Z_0 \\ T_r &< 2t_f. \end{aligned} \tag{16}$$

Here, R and C are line resistance and capacitance per unit length, l is line length, $\mathrm{C_L}$ is load capacitance (contributed by fanout input capacitance), $\mathrm{T_r}$ is the rise time at the output of the driver, and $\mathrm{t_f}$ is the time of flight. If the above criteria are satisfied, then inductive effects are significant and we use the two-ramp modeling approach. Otherwise, a single effective capacitance is used to model the driving point waveform.

The criteria in (16) are identical to those in [11], but with an additional condition that compares rise time with the time of flight. This condition is important for screening short lines. These lines rarely exhibit inductive behavior since their time of flight is normally smaller than their transition time. The authors of [6] consider this by comparing rise time at the input of the driver with the time of flight. However, inductive effects are fairly insensitive to the input transition times and strongly dependent on the driver's output transition time [12]. Hence, we use output transition times in (16). This is complicated by inductive effects, however, as the driver output waveform rises sharply to a certain level and then flattens before meeting the reflections. When comparing the rise time with the time of flight, it is the initial ramp that is important. We compute this initial ramp $(\mathrm{T_{r1}})$ using $\mathrm{C_{eff1}}$ iterations and apply it to the inductance criteria.

The outline for the overall modeling flow is as follows. Given the line parasitics (R, L, C) and the characterized output delay table for the driver, perform these steps for timing analysis.

1) Find driving point admittance moments and compute $\mathrm{a_1}$, $\mathrm{a_2}$, $\mathrm{a_3}$, $\mathrm{b_1}$, and $\mathrm{b_2}$.
2) Find driver on-resistance $(\mathrm{R_s})$ and compute breakpoint (f) using (1).
3) Perform $\mathrm{C_{eff1}}$ iterations using (8) or (10) and compute $\mathrm{T_{r1}}$.
4) Check inductance criteria using (16).
   If inductance is significant:
   - perform $\mathrm{C_{eff2}}$ iterations using (13) or (14) and compute $\mathrm{T_{r2}}$;
   - modify $\mathrm{T_{r2\ r2\_new}}$ using (15);
   - use $\mathrm{T_{r1}}$, $\mathrm{T_{r2\_new}}$ and breakpoint to model the driver output as a two-ramp waveform.

   If inductance is not significant:
   - perform $\mathrm{C_{eff}}$ iterations using (8) or (10) with $f = 1$ and compute $\mathrm{T_r}$;
   - model the output as a single ramp. If there is significant resistive shielding, then model an exponential tail using the approach of [2].
5) Convolve driver output waveform with interconnect transfer function and compute far-end response.

VI. EXPERIMENTAL RESULTS

We tested the new two-ramp approach for varying line lengths, widths, and driver sizes. All experiments were performed using a commercial 1.8-V, 0.18-μm CMOS technology. Line parasitics were extracted using the commercial extraction tool Raphael. A two-dimensional power grid of 50-μm pitch and 5-μm linewidth was used for inductance extraction.

First, we compare the driving point waveforms obtained by our model with HSPICE simulations. Figs. 7 and 8 show two such comparisons for RLC lines driven by inverters. The inputs to the inverters are ramp signals having 100-ps and 75-ps transition times, respectively. It is clear from the figures that the two-ramp model captures the overall shape of the driver output waveform (including the breakpoint and key delay points) very accurately. These examples also show that, even when the plateau is clearly visible in SPICE waveforms, the

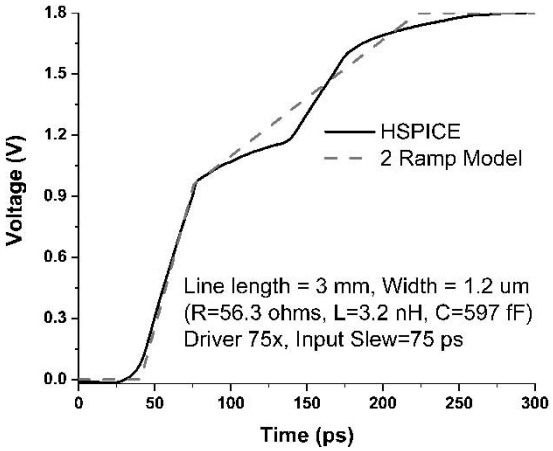

Fig. 8. Two-ramp driver output response compared to HSPICE for a 3-mm line driven by 75X driver.

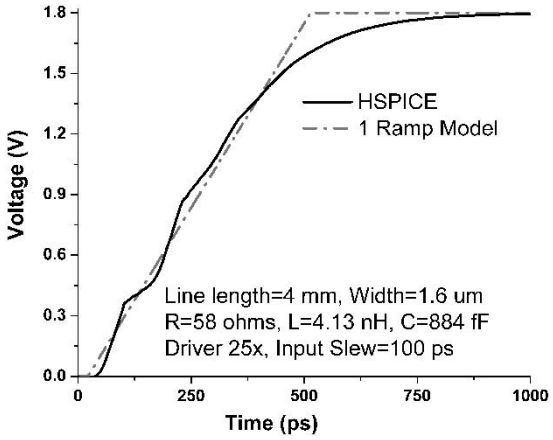

Fig. 9. One-ramp driver output response compared to HSPICE for a 4-mm line driven by 25X driver.

assumption of modeling plateau and reflection together with one ramp is effective. Fig. 7 also shows the model where the plateau is captured with a flat step. It is clear from the figure that modeling the plateau as a flat step is significantly less accurate than the simple two-ramp model.

Next, we compare the waveforms of a 4-mm line driven by a 25X inverter (Fig. 9). In this case, driver resistance was much higher than the line impedance. The inductance criteria (16) were not satisfied and a single C_{eff} model was used. We see that a single ramp is sufficient to model the entire transition in this case. This result is useful because it shows that transmission line effects are significant only when lines are driven by strong drivers and that two-ramp model should be used only when inductive effects are dominant.

We also observed the far-end waveforms by applying the modeled two-ramp input waveform to an RLC line within HSPICE. These waveforms were compared with the actual far-end response. Fig. 10 shows one such comparison for a 4-mm line driven by 75X driver. The figure shows that the far-end response derived using the two-ramp model matches very well with SPICE, validating the two-ramp assumption at the near end.[2] The figure also shows that the plateau and the reflections are visible only in near-end waveforms. The far-end waveforms

[2]The far-end waveforms from the model show higher overshoot due to the ramp approximation at the near-end.

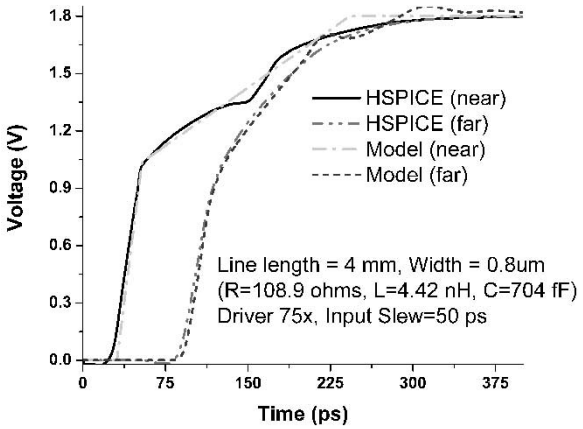

Fig. 10. Two-ramp driver output response and corresponding far-end response compared to HSPICE for a 4-mm line driven by 75X driver.

do not show these effects and can be modeled by one ramp. This observation ensures that the two-ramp modeling of the near-end waveform does not require characterizing drivers for two-ramp inputs. Hence, our approach remains compatible with existing cell characterization.

We tested the new model by sweeping line lengths from 1 to 7 mm and linewidths from 0.8 to 3.5 μm. Driver strengths were also swept from 25 to 125X. Input transition was varied from 50 to 200 ps. The two-ramp model results were compared to HSPICE and one-ramp assumptions. For one-ramp modeling, we considered both possibilities: when the ramp is obtained by equating charge transfer till 50% of the transition and also when it is obtained by equating charge over entire transition (as shown in Fig. 5). For the target 0.18-μm technology, we found inductive effects to be particularly significant in long ($\geq$3 mm) and wider wires ($\geq$ 1.6 μm) driven by fast inverters (75X and larger). When inductive effects were dominant, the single ramp assumptions were highly inaccurate and the two-ramp model provided good results. The two-ramp model results for the 165 inductive cases we tested are shown in Fig. 11. The average error in delay was 6% and the average error in the slew rates was 11%. For delay, 48% of the cases had less than 5% error and 83% of the cases had less than 10% error. For slew rate, 31% of the cases showed less than 5% error and 61% of the cases showed less than 10% error.

Table II shows more complete results for a representative set of cases with significant inductive effects. HSPICE delay and slew numbers are compared with the single ramp and two-ramp modeling results. It is clear from the table that increasing linewidths lead to more significant inductive effects and the delay values from one-ramp assumptions become more inaccurate. The delay values for the one-ramp model based on equating the charge until the 50% switching point are much better than those obtained by the one-ramp model when equating charge over the entire transition. However, as discussed in Section IV and shown in Fig. 5, the slew values with 0–50% one-ramp model are much worse than the 0–100% one-ramp model. In addition, the 50% delay estimates for the two-ramp model are typically superior to those using the standard one-ramp C_{eff} methodology (0–50%). In general, the slew predictions using one-ramp modeling approaches exhibit substantial error, since they cannot capture the long tail of the inductive waveform. We also note that the extended model of [2], which captures *RC* tails due to resistive shielding, cannot be applied to inductive cases as it is *RC*-based and does not comprehend the nature of the tail in the inductive response. The results in Table II both demonstrate the accuracy of the two-ramp approach and confirm that the traditional approach of

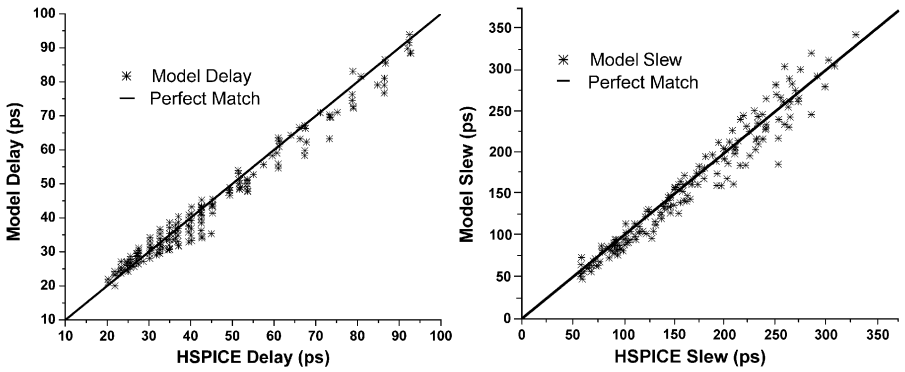

Fig. 11. 50% delay and 10%–90% slew obtained with two-ramp model compared to HSPICE for 165 inductive cases.

TABLE II
HSPICE, ONE-RAMP, AND TWO-RAMP MODEL COMPARISON RESULTS

Len/Wid mm/μ	Line Parasitics R(Ω)/L(nH)/C(pF)	Driver Size	Input Slew (ps)	Delay (ps)				Slew (ps)			
				SPICE	2 ramp (%error)	1 ramp 0-100% (%error)	1 ramp 0-50% (%error)	SPICE	2 ramp (%error)	1 ramp 0-100% (%error)	1 ramp 0-50% (%error)
3/0.8	81.8/3.3/0.52	75x	50	25.01	24.2 (-3.2%)	41.3 (65.1%)	23.3 (-6.8%)	124.1	129.9 (4.6%)	61.5 (-50.4%)	27.8 (-77.5%)
3/1.2	56.3/3.2/0.59	75x	50	26.44	25.6 (-3.1%)	56.3 (112.9%)	24.9 (-5.7%)	128.9	141.1 (9.4%)	91.8 (-28.7%)	30.4 (-76.4%)
3/1.6	43.5/3.1/0.66	75x	50	32.15	29.9 (-6.9%)	66.1 (105.5%)	26.3 (-18.1%)	135.4	148.8 (9.8%)	112.1 (-17.2%)	32.9 (-75.6%)
4/0.8	108.9/4.4/0.7	75x	50	25.02	25.7 (2.7%)	39.1 (56.2%)	24.9 (-0.5%)	157.3	163.1 (3.6%)	57.3 (-63.5%)	30.4 (-80.7%)
4/1.2	75/4.2/0.8	75x	50	26.51	27.7 (4.4%)	59.1 (122.9%)	26.8 (1.24%)	164.4	179.0 (8.8%)	97.6 (-40.6%)	33.9 (-79.3%)
4/1.6	58/4.1/0.88	75x	50	32.69	30.2 (-7.6%)	74.9 (129.1%)	28.6 (-12.5%)	175.0	196.0 (12.0%)	130.5 (-25.3%)	37.1 (-78.8%)
5/1.2	93.7/5.3/1	100x	100	36.43	35.6 (-2.2%)	46.4 (27.3%)	33.5 (-8.1%)	192.8	173.7 (-9.9%)	60.0 (-68.8%)	42.0 (-78.2%)
5/1.6	72.4/5.1/1.11	100x	100	39.56	37.7 (-4.7%)	53.0 (33.9%)	35.6 (-9.9%)	200.3	204.0 (1.8%)	71.8 (-64.1%)	44.5 (-77.7%)
5/2.0	59.7/5/1.22	100x	100	42.53	39.5 (-7.1%)	63.1 (48.3%)	37.7 (-11.4%)	207.6	226.3 (9.0%)	90.9 (-56.2%)	47.0 (-77.3%)
5/2.5	49.5/4.8/1.31	100x	100	45.26	42.4 (-6.3%)	78.2 (72.7%)	39.4 (-13.0%)	212.2	231.8 (9.2%)	121.1 (-42.9%)	49.3 (-76.7%)
6/1.2	112.4/6.3/1.19	100x	100	36.44	37.0 (1.5%)	46.5 (27.6%)	34.9 (-4.2%)	222.7	203.7 (-8.5%)	60.1 (-73.0%)	43.7 (-80.4%)
6/1.6	86.9/6.2/1.33	100x	100	39.58	39.3 (-0.7%)	52.4 (32.3%)	37.4 (-5.4%)	232.0	235.5 (1.5%)	70.7 (-69.5%)	46.8 (-79.8%)
6/2.0	71.6/6/1.46	100x	100	42.55	41.4 (-2.7%)	60.8 (42.8%)	39.7 (-6.6%)	240.9	254.7 (5.7%)	86.4 (-64.1%)	49.8 (-79.3%)
6/2.5	59.3/5.8/1.58	100x	100	45.29	45.9 (1.3%)	75.1 (65.9%)	41.7 (-8.0%)	246.3	276.9 (12.4%)	114.2 (-53.6%)	52.6 (-78.6%)
6/3.0	51.2/5.6/1.80	100x	100	49.41	47.8 (-3.2%)	101.4 (105.2%)	44.8 (-9.3%)	261.7	299.1 (14.2%)	168.4 (-35.6%)	57.3 (-78.1%)

modeling driver output with one ramp is highly inaccurate in inductive interconnects.

VII. CONCLUSION

In this paper, we presented a new approach to model the driving point waveform in the presence of RLC interconnect loads. We showed that when transmission line effects are significant in RLC interconnects, driver output waveforms are nonsmooth and they exhibit inflection points during transition. We developed a two-ramp model to accurately capture these inductive effects. Our approach is based on the theory of reflections in transmission lines and is compatible with existing precharacterized cell delay tables. We tested this model on a variety of test cases and showed that it accurately predicts delay and slew at the driver output when inductive effects are significant. We also showed that a one-ramp assumption may be sufficient for *RC* and weakly inductive lines, but becomes highly inaccurate for inductively dominated interconnects. In such cases, the two-ramp modeling approach provides delay and slew estimates that are within 6% and 11% of SPICE on average, respectively.

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