Low-Voltage Circuit Design for Widespread Sensing Applications

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Abstract— **Ubiquitous computing has a number of compelling applications ranging from biomedical sensing to environmental monitoring. These computing systems require low cost sensor nodes with volumes <1mm^3 and lifetimes on the order of months or years. We advocate the use of aggressively scaled supply voltages in such applications to maximize energy efficiency. This paper reviews our recent progress in mapping out the low energy design space. We explore the design and test of three low voltage systems targeting ubiquitous computing. We conclude with a survey of open research directions in the ultra-low energy design space.**

I. Introduction

Ubiquitous sensing systems, with a single node or thousands of nodes, are quickly becoming a viable technology option with the advancement of circuit and sensor design. In such a system, the most basic building block is an inexpensive sensor node with data processing and storage, off-chip communication, sensing elements, and a power source all linked within a robust package with a volume on the order of 1mm^3. The sensor node must have a lifetime on the order of months or years. Due to the limitations of power sources, the most pressing implication of this lifetime requirement is that the power consumption of all components must be minimized.

In this work, we describe our recent progress in developing highly integrated ultra-low energy sensor nodes. In particular, we discuss the use of low voltage circuits to meet stringent energy budgets. We begin by demonstrating the energy benefits of low voltage operation using measurements of an 8-bit processor that is operational below 200mV. We also use this processor to explore the mitigation of process variability at low voltage. We then discuss the design of robust SRAM for low voltage systems, which is the most important problem facing low voltage designers when coupled with variability. We include measurements of a 2kb memory that remains functional below 200mV. In addition to our studies of processor and memory design, we have recently made important first steps toward viable ubiquitous sensing systems by integrating a low voltage processor with a DC-DC converter and a compact battery. We discuss these results and then conclude with a discussion of remaining challenges and open research directions.

II. Low Voltage Logic Design

Due to the quadratic dependence of switching energy on supply voltage (V_{dd}), dramatic energy reductions can be achieved in digital logic by reducing V_{dd}. It has long been known that CMOS circuits continue to function with V_{dd} well below the threshold voltage (V_{th}), so aggressive voltage scaling into the subthreshold regime ($V_{dd}<V_{th}$) is possible with careful design. To explore low voltage operation, we fabricated an 8-bit processor with 1.5kb instruction memory and 1kb data memory in a 0.13µm process [1]. The processor targets mobile sensor applications where energy consumption is the primary metric and performance is a secondary concern. Logic blocks were synthesized using a limited set of low fan-in CMOS standard cells, and the memories were implemented using a robust latch-based memory [2].

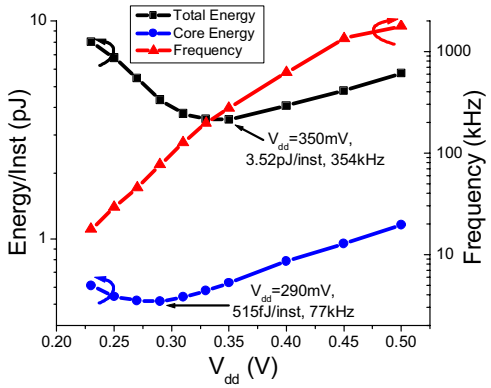

Figure 1. Energy and frequency for an 8-bit subthreshold processor [1]

Figure 1 shows energy and frequency measurements of the processor as functions of V_{dd}. At V_{dd}=350mV, energy consumption reaches a minimum of 3.52pJ/instruction at a frequency of 354kHz. At this voltage, energy consumption is improved by an estimated 8X as compared to normal superthreshold operation. The presence of an energy minimum [3,4] is an important concept for low voltage designers. Despite a reduction in switching energy with V_{dd}, delay increases exponentially at low V_{dd} causing leakage energy ($V_{dd}\cdot I_{leak}\cdot t_{delay}$) to increase and eventually create an

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energy minimum. Energy has been plotted in Figure 1 for the total system as well as the core logic (not including memories). At V_{dd}=350mV, ~80% of the total energy is consumed by memories, suggesting that memory design will play a critical role in the energy efficiency of low V_{dd} systems. We discuss one such memory in the next section.

While energy is dramatically reduced at low V_{dd}, subthreshold operation suffers from an exponential sensitivity to process- and temperature-induced V_{th} variations. Previous work has shown that random V_{th} variability caused by random dopant fluctuations (RDF) can be addressed by increasing gate sizes [5,6] and by increasing the number of logic gates between sequential elements [5]. Systematic V_{th} variation is also problematic but can be addressed more directly by applying body biases to compensate for systematic PFET/NFET mismatch. We demonstrate this compensation within the 8-bit processor described previously. Figure 2 shows energy and frequency distributions for 20 measured dies under four different body bias configurations. In the first configuration, no body bias is applied. In the remaining three configurations, body bias is applied uniquely to each die to target frequencies of 66kHz (the worst case frequency when no body bias is applied), 100kHz, and 160kHz. Frequency variations are eliminated with the application of a body bias while energy variations are reduced significantly. Also note that the frequency can be tuned from 66kHz to 160kHz with minimal energy penalties.

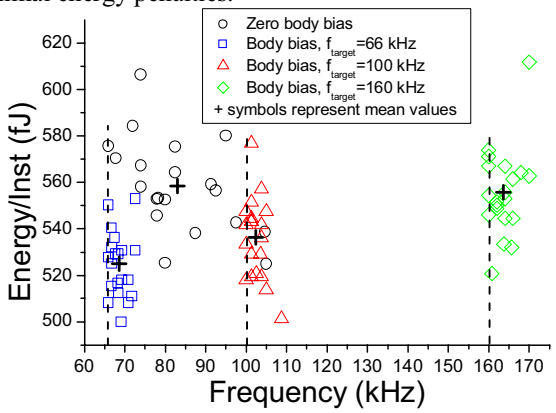

Figure 2. Energy and frequency distributions for 20 dies with and without body bias [1]

III. Robust Low Voltage Memory Design

As shown in the last section, memory design has important energy implications for low voltage system design. Even more importantly, the 6T SRAM is particularly susceptible to V_{th} mismatch induced by RDF. A number of alternative SRAM cells have been proposed recently to enable robust low voltage operation in the face of variability [7-11]. We investigate one such cell in this section. A 2kb SRAM array was fabricated in a 0.13µm process using the modified 6T SRAM cell shown in Figure 3 [7]. The single-ended design is inherently more robust to read upsets since noise is isolated to the single bitline. Additionally, the transmission gate can drive the bitline from rail-to-rail, eliminating the need for area-intensive sense-amplifiers. To decouple read and write operations and regain lost write margins, the power supply of the feedback inverter is gated during write operations. Transistor sizes are also increased to combat RDF. Measurements of the SRAM show that it remains functional below 200mV. Figure 3 shows that the proposed cell is far more energy efficient than a latch-based memory similar to the one used in the processor described in Section II.

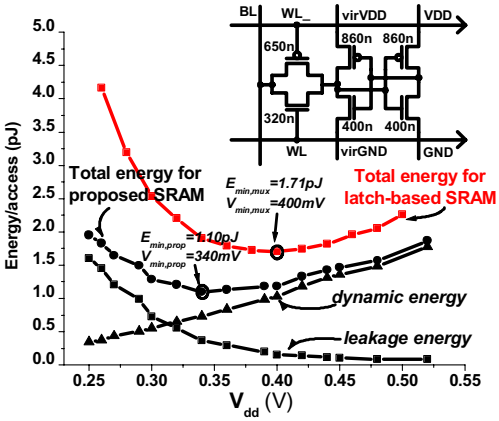

Figure 3. Energy measurements for a modified 6T SRAM [7] and a latch-based memory are compared. Inset shows the proposed 6T SRAM cell.

IV. System Integration

With low voltage digital design rapidly maturing, the next important step toward ubiquitous computing is to integrate the power source with the computational elements. In this section, we describe the integration of a solid state battery and a digital processor which are part of an implantable system for biomedical applications. Since the battery does not produce the voltage required by the digital processor, a DC-DC converter is also used to down-convert voltage.

Ubiquitous computing systems pose a substantial challenge to traditional energy storage technologies. Integrated circuits are fabricated in planar architectures, which are of much smaller profile than the layered battery electrodes required for high capacity and power/energy density. At present, there are no power sources available commercially which meet key design requirements as well as the established energy target of 30 mWh/cm^2 [24]. Thin film lithium (Li) and nickel/zinc (Ni/Zn) batteries have been proposed to power ubiquitous computing systems but have energy densities (100-500 µWh/cm^2) which fall substantially short of this goal [25,26]. A generic assembly consists of direct fabrication onto a semiconductor chip, the chip package or the chip carrier using solid-state materials. However, most battery fabrication processes are not compatible with integrated circuits due to high processing temperatures (up to 800ºC), which can be harmful both circuits and packages. Furthermore, the use of a clean room environment necessitates expensive separate manufacturing steps and packaging.

We have developed a technology to manufacture 3-D microbatteries on silicon substrates that is both simple and

cost effective [27]. Using our optimization algorithm POWER [28,29] we identified a zinc/silver oxide electrochemistry (Zn/AgO) as the optimum power source for the present application. We designed and fabricated a monolithic power supply, with planar architecture, suitable for the proposed device architecture [30]. The chosen electrochemistry generates a nominal voltage of 1.55V and, with a footprint of ~1cm^2, has a capacity of ~0.1mAh and specific capacity of ~100μAh/cm^2. A battery area of 5.25mm^2 was used in this study to match the form factor of the processing element.

Since the battery nominally generates 1.55V, a DC-DC converter is used to down-convert to the energy-optimal voltage of 0.3-0.4V. Switching power supply designs, like the Buck converter, can achieve power efficiency >90% [21], but the size of the inductor must be prohibitively large to maintain such high efficiency at load currents on the order of 100nA. Linear voltage regulators are extremely simple and area efficient but achieve poor power efficiency for large down-conversions. Switched capacitor-based converters are an attractive alternative to these two architectures. They have been shown to achieve power efficiencies as high as 85% [22] and require simple, compact design.

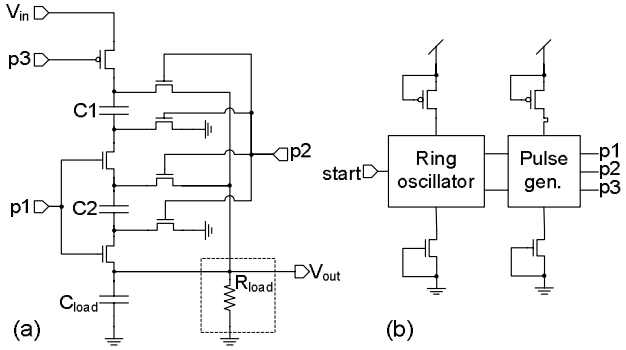

Figure 4. (a) 3-stage switched capacitor DC-DC converter (b) Current starved pulse generator

The DC-DC converter, shown in Figure 4(a), was fabricated in a 0.13μm process. A 3-stage conversion was used with NFET gate oxide capacitors. Power losses in the switched capacitor DC-DC converter are largely a result of pulse generation, so it was important to minimize the current consumption of the pulse generation circuitry. A simple current starved 15-stage ring oscillator, shown in Figure 4(b), was fed to a similarly starved pulse generator. Measurements show that the DC-DC converter reaches a maximum power efficiency of 44% when converting from 1.2V to 0.29V with an 87nA load current.

The 8-bit processor, which was fabricated in a 0.18μm process, uses the same architecture as the processor described in Section II. A simple on-chip oscillator was used for clock generation to ensure that the clock frequency scales with battery output voltage.

The battery, DC-DC converter, and processor were integrated at the board level. To measure the energy efficiency of the system, we run a simple arithmetic routine once every ~1 minute until the battery can no longer sustain the required voltage and current. Between runs, the processor idles in a light sleep state. The processor and DC-DC converter draw an average active current of ~113nA and an average idle current of ~100nA. After 11 hours, the battery output voltage drops dramatically below 1.55V. Since the DC-DC converter divides the voltage by a fixed ratio, this voltage drop causes the processor to fail.

The lifetime of the processor under test is ultimately limited because it does not include power gating or any other form of power management. Using the measured capacity of the battery and the current demand of the processor, we can estimate the leakage savings needed for a more useful one year lifetime. Measurements of our integrated system give a capacity of ~1.1μAh (given an average measured current of ~100nA over the 11 hour lifetime). Measurements show that the processor draws an average active current of 113nA. For an application where computation (i.e., a sensor measurement followed by data processing) is carried out for 100ms periods once every 10 minutes, we find that the average sleep current must be 107pA to achieve a one year lifetime. This clearly underscores the need for research efforts in sleep power management, which will be covered briefly in the next section.

V. Future Directions

The work described in the previous sections highlights the fantastic progress made recently in ubiquitous computing. However, several challenges remain before the 1mm^3 is commercially viable. In this section, we suggest several avenues for future exploration in ubiquitous computing.

Variability due to all sources, including process, voltage, and temperature (PVT) are all magnified in subthreshold, as discussed earlier. There is a great need for a range of effective techniques to combat this variability. In particular, temperature-insensitive design approaches become an interesting topic of study; this may employ adaptive body bias [12]. Logic families other than CMOS may also offer greater resiliency to certain variation sources such as voltage or process. Architectural approaches to variability are also vital – these may include a proliferation of traditional schemes such as error correction and redundancy, although the power costs of added hardware need to be weighed carefully against the improvements in robustness achieved.

Very low-power wireless communication schemes are needed; else the low energy budget of the digital processing component of a system will simply be swamped out by the communication requirements. This is highly application-specific; there may be cases where proximity communication schemes [13,14] are suitable and others where more traditional radios are used but with new architectures to address strict power budgets [15]. Ultra-wideband radio design is also becoming increasingly attractive since low energy consumption can be achieved at low data rates [23].

In a widespread ubiquitous system, tight synchronization between physically adjacent nodes enables multi-hop long distance communication. Watchdog timers are therefore critical components in ubiquitous computing; however, accurate timing is extremely challenging given

stringent energy budgets and volatile environmental conditions. Recent work in ultra-low power timing has reported power consumption below 1pW [16], but further work will be necessary to minimize jitter and temperature sensitivity at such low power levels.

Extremely low duty cycle applications, for instance environmental monitoring or the monitoring of cracks along oil pipelines, require a sensor to be read and data to be processed on a relatively infrequent basis (on the order of minutes). For such systems, standby mode power will be the dominant source of power consumption. Current techniques to reduce standby mode leakage, such as power gating, are insufficient to provide required battery lifetimes. In these cases transistors should be employed as frugally as possible since added devices will inherently leak during standby. Novel architectures and low-power modes will need to be invented to enable sleep mode current levels below 1nA.

Subthreshold circuits can greatly benefit from a rethinking of device [17,18] and interconnect architectures. Since it may not be feasible to have a process variant dedicated to subthreshold, work is needed to find ways to tailor device and interconnect behavior to the unique needs of subthreshold design. Interconnect is interesting since parameters such as wire resistance become inconsequential compared to channel resistances. This may lead to a complete re-thinking of how things such as clock and power routing are done, as well as how back-end stacks are manufactured (e.g., thick/wide wires are counterproductive since capacitance is the only important parasitic) [19].

Finally, further research in CMOS-compatible power sources is necessary. The microbattery described in this work is a cost efficient solution, but other options such as solar power, ambient vibration, or other scavenging techniques [20] must be considered.

REFERENCES

[1] S. Hanson, et al., "Performance and Variability Optimization Strategies in a Sub-200mV, 3.5pJ/inst, 11nW Subthreshold Processor," *Symp. on VLSI Circuits, pp. 252-253, 2007.*

[2] A. Wang, A. Chandrakasan, "A 180mV FFT processor using subthreshold circuit techniques," *Int. Solid-State Circuits Conf.*, pp. 292-293, 2004.

[3] B. Zhai, D. Blaauw, D. Sylvester, K. Flautner, "Theoretical and Practical Limits of Dynamic Voltage Scaling," *Design Automation Conf.*, pp. 868-873, 2004.

[4] B. Calhoun, A. Chandrakasan, "Characterizing and Modeling Minimum Energy Operatoin for Subthreshold Circuits," *Int. Symp. On Low Power Electronics and Design*, pp. 90-95, 2004.

[5] B. Zhai, S. Hanson, D. Blaauw, D. Sylvester, "Analysis and Mitigation of Variability in Subthreshold Design, pp. 20-25, 2005.

[6] B. Calhoun, A. Chandrakasan, "Analyzing Static Noise Margin for Sub-threshold SRAM in 65nm CMOS," *European Solid-State Circuits Conf.*, pp 363-366, 2005.

[7] B. Zhai, D. Blaauw, D. Sylvester, S. Hanson, "A Sub-200mV 6T SRAM in 0.13µm CMOS," *Int. Solid-State Circuits Conf.*, pp. 332-333, 2007.

[8] L. Chang, et al., "Stable SRAM cell design for the 32nm node and beyond," *Symp. on VLSI Technology*, 128-129, 2005.

[9] B. Calhoun, A. Chandrakasan, "A 256kb Sub-threshold SRAM in 65nm CMOS," *Int. Solid-State Circuits Conf.*, pp. 628-629, 2006.

[10] T. Kim, J. Liu, J. Keane, C.H. Kim, "A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme," *Int. Solid-State Circuits Conf.*, pp 330-331, 2007.

[11] N. Verma, A. Chandrakasan, "A 65nm 8T Sub-Vt SRAM Employing Sense-Amplifier Redundancy," *Int. Solid-State Circuits Conf.*, pp. 328-329, 2007.

[12] S.V. Kumar, C.H. Kim, S.S. Sapatnekar, "Mathematically-Assisted Adaptive Body Bias (ABB) for Temperature Compensation in Gigascale LSI Systems," *Asia-South Pacific Design Automation Conf.*, pp. 559-564, 2006.

[13] R.J. Drost, R.D. Hopkins, R. Ho, I.E. Sutherland, "Proximity communication," *Journal of Solid-State Circuits*, pp. 1529-1535, 2004.

[14] N. Miura, D. Mizoguchi, T. Sakurai, T. Kuroda, "Analysis and design of inductive coupling and transceiver circuit for inductive inter-chip wireless superconnect," *Journal of Solid-State Circuits*, pp. 829-837, 2005.

[15] J. Chen, M.P. Flynn, J. Hayes, "A Fully Integrated Auto-Calibrated Super-Regenerative Receiver," *Int. Solid-State Circuits Conf.*, 2006.

[16] Y.-S. Lin, D. Sylvester, D. Blaauw, "A sub-pW timer using gate leakage for ultra low power sub-Hz monitoring systems," *Custom Integrated Circuits Conf*, 2007.

[17] A. Raychowdhury, B.C. Paul, S. Bhunia, K. Roy, "Computing with subthreshold leakage: device/circuit/architecture co-design for ultralow-power subthreshold operation," *Trans. on VLSI Systems*, pp. 1213-1224, 2005.

[18] S. Hanson, M. Seok, D. Sylvester, D. Blaauw, "Nanometer Device Scaling in Subthreshold Circuits," *Design Automation Conf.*, 2007.

[19] S. Hanson, et al., "Ultralow-voltage minimum-energy CMOS," *IBM Journal of Research and Development*, Vol. 50, pp. 469-90, 2006.

[20] J.A. Paradiso, T. Starner, "Energy scavenging for mobile and wireless electronics," *Pervasive Computing*, pp. 18-27, 2005.

[21] G.-Y. Wei, M. Horowitz, "A Fully Digital, Energy-Efficient Adaptive Power-Supply Regulator," *Journal of Solid-State Circuits*, Vol. 34, pp. 520-528, 1999.

[22] S.V. Cheong, H. Chung, A. Ioinovici, "Inductorless DC-to-DC Converter with High Power Density," *Trans. on Industrial Electronics*, Vol. 41, pp. 208-215, 1994.

[23] F. Lee, A. Chandrakasan, "A 2.5nJ/b 0.65V 3-to-5GHz Subbanded UWB Receiver in 90nm CMOS," *Int. Solid-State Circuits Conf.*, pp. 116-117, 2007.

[24] J.W. Long, B. Dunn, D.R.Rolison, H.S. White, "Three-dimensional battery architectures," *Chemical Reviews*, Vol. 104, pp. 4463-4492, 2004.

[25] B. Bates, et al., "Thin-film lithium and lithium-ion batteries," *Solid State Ionics*, Vol. 135, pp. 33, 2000.

[26] P.H. Humble, J.N. Harb, R. LaFollette, "Microscopic nickel-zinc batteries for use in autonomous microsystems," *Journal of the Electrochemical Society*, Vol 148, pp. A1357, 2001.

[27] PATENT DISCLOSURE #3633, A.M Sastry, F. Albano, "Micromachined Deposited Battery," 2007.

[28] K.A. Cook, A.M. Sastry, "An Algorithm for Selection and Design of Hybrid Power Supplies for MEMS with a Case study of a Micro-gas Chromatograph System," *Journal of Power Sources*, Vol. 140, pp. 181-202, 2005.

[29] K.A. Cook, F. Albano, P.E. Nevius, A.M. Sastry, "POWER (Power Optimization for Wireless Energy Requirements): A MatLab Based Algorithm for Design of Hybrid Energy Systems," *Journal of Power Sources*, Vol 159, pp. 758-780, 2006.

[30] F. Albano, et al., "Design of an implantable power supply for an intraocular sensor, using POWER (Power Optimization for Wireless Energy Requirements)," *Journal of Power Sources*, Vol 170, pp. 216-224, 2007.