

Sensor Data Retrieval Using Alignment Independent Capacitive Signaling

Yu-Shiang Lin, Dennis Sylvester and David Blaauw
University of Michigan, Ann Arbor, MI

Abstract

We propose a capacitive coupling based method for sensor data retrieval which can be easily integrated with miniature sensor nodes of sub-mm scale. An alignment independent mechanism is implemented to achieve <15% difference in achievable data rate when the sensor chip is randomly dropped on the data retrieval chip regardless of alignment. To enable passive operation of the sensor chip, the data retrieval chip send power to/receive signal from the sensor chip simultaneously.

Introduction

Miniature self-sustaining sensor nodes have become a viable option with silicon technology scaling. Such a system can be easily attached to, or implanted into, various objects for applications such as periodic sensing and recording of temperature or bio-chemical data. With energy minimization techniques [1] and aggressive power gating, these systems can potentially operate using a micro-fabricated battery with comparable form factor over an extended period of time. Passive RFID transponder techniques can be used to eliminate read-out energy dissipation for the sensor, but this requires an external coil on a centimeter scale, significantly limiting the application space. In this work, we propose a capacitive coupling based method where the communication module is fully integrated with the sensor node, on a sub-mm scale. The goal is to allow a passive sensor chip (SC) to be dropped face-to-face onto a data retrieval chip (DR) for read-out without precise positioning.

Capacitive coupling has been proposed for high performance communication due to its high bandwidth and low energy consumption of less than 0.1pJ/b [2-3]. Since the signal strength of capacitive coupling is inversely proportional to the distance, Vernier device and other electrical methods need to be adopted for correcting pad misalignment [4-5]. In our system, a digital alignment circuit is proposed to overcome misalignment issues. At the same time, the DR sends both power and signal to the SC so that the SC consumes no power during read-out.

Proposed Approach

Fig. 1 shows the proposed system diagram for sensor data retrieval. Two power channels and a signal channel between SC and DR are established through capacitive coupling. The clock signal is modulated with the power signals, so no additional channel is needed for synchronization. This also helps to precisely control the sensing window of the receiver circuit for better noise rejection. While the SC has 3 pads dedicated to individual channels, DR contains an array of 20 by 20 pads that each can be assigned as the signal channel or can be clustered as a power channel as needed. The pad size and spacing are optimized so that the coupling capacitance under worst case alignment is within 1% of the best case. Physical dimensions are summarized in the table of Fig. 1.

After SC is dropped on top of DR, the alignment detector shown at top of Fig. 2 determines the best configuration. The alignment detector is an embedded ring oscillator feeding a counter enabled by a programmable pulse for each DR pad. The output *data_out* is first recorded without the transmitter chip present, and later the difference of *data_out* (Δcnt) can be calculated when the transmitter chip is in position. A larger value of Δcnt indicates that the parasitic capacitance corresponding to the cell is also larger. Shown in the bottom right of Fig. 2, measured Δcnt values clearly depict the outline of the SC chip and the location of both the power pads (large circles) and signal pad (small circle). After Δcnt is computed, the cell array is

reconfigured to the appropriate three clusters to perform power transmission or signal reception as illustrated in bottom left of Fig. 2.

Figure 3 shows the data retrieval mechanism. Two differential amplifiers are used to detect both the rising and falling transitions. The input node (V_{in}) is precharged to $VDD/2$ before the clock goes high. Immediately after the clock fires, either V_{th} or V_{hl} will be pulled down depending on the direction of the coupled signal. The high-to-low transition triggers the 400-to-1 AND tree gate that simultaneously monitors all DR pads and results in an UP/DN signal for the one-bit saturation counter that determines the data output. Shortly after the rising edge of the clock, signal preset is asserted again to avoid unintentional glitching. The difference between V_{dc} and V_{dc1}/V_{dc2} is designed to be 50mV to mitigate input offset voltage and the impact of noise.

The main block of SC is the regulator circuit shown in Fig. 4. The AC coupled inputs V_{in} and V_{inn} are rectified into DC voltage outputs. Each voltage doubler stage contains a full-bridge cross-coupled rectifier. At the output of the 10th stage, a voltage limiter prevents the supply voltage from going above operating range. Node $n2$ will remain close to VSS before $VDD10$ exceeds $2\Delta V$ (where ΔV is the turn-on voltage of the diode-connected transistors m5 and m6). When $VDD10$ increases beyond $2\Delta V$, the excessive voltage drop will occur mainly across R1, and thus voltage V_{n2} begins to track the supply voltage. On the other hand, voltage V_{n1} will be limited at ΔV once the supply voltage is higher than this value. By comparing V_{n1} and V_{n2} , the amplifier output V_{n3} will begin to turn on m10 when the supply voltage is greater than 1.6V. Since each voltage doubler stage is identical, intermediate voltage levels are inherently generated. In this work, we use $VDD4$ (0.65V) to supply the voltage for a 4-bit LFSR circuit to generate a data stream with low power consumption and then up-convert to $VDD10$ to increase signal strength before transmission.

The test chip was fabricated in 0.13 μm CMOS technology (Fig. 5). The active area of the SC and DR chip are 0.014mm² and 1.3mm², respectively. The sensor chip is 0.5x0.5mm after being diced.

Measured waveforms are shown in Fig. 6. The measured operating frequency of this system is defined when no errors occur in 10⁹ cycles. Fig. 7 shows the operating frequency (f_{data}) and energy consumption per bit with respect to the transmitting amplitude (A_{in}) and carrier frequency (f_c) of the power signals. We use I/O devices for power transmission so A_{in} can be as high as 3.3V in this 0.13 μm technology. The system successfully operates at $A_{in} > 1.8V$. Estimated working distance is also shown on the second x-axis of the f_{data} plot. Based on measurement data, I/O devices would not be needed if the passivation thickness were reduced by 2/3. It is observed that raising f_c above 150MHz increases energy consumption while also reducing f_{data} . The reason for this is that at high frequencies, the clock skew of different cells can cause signals in the same power cluster to become out-of-phase and cancel each other out. Since targeted data working sets for sensor nodes are on the order of kb, the achievable data rate is sufficient for complete data retrieval on the ms timescale.

Fig. 8(a) shows BER with respect to the window size (T_w) of the modulated clock for power transmission. T_w is the period when the output clk_{mod} (Fig. 1) remains 0. The bathtub shape of BER shows that the optimal T_w is constrained by two different factors: demodulation time and rectified voltage. When T_w is small, the demodulator cannot respond quickly enough to restore the clock. However, increasing T_w eventually results in insufficient energy to maintain the

supply voltage for SC. Fig. 8(b) shows the data rate vs. BER for 10 different random locations at which the SC was dropped. Some regions yield a lower data rate mainly due to the non-uniform surface of the passivation layer. These results verify that the proposed system adapts to different orientations without the need for precise positioning machinery.

	Pad size	Pad spacing	Pad number
sensor chip	Power: $225\mu\text{m} \times 225\mu\text{m}$ Signal: $150\mu\text{m} \times 150\mu\text{m}$	$\sim 20\mu\text{m}$	Power: 2 Signal: 1
data retrieval chip	$48\mu\text{m} \times 48\mu\text{m}$	$5\mu\text{m}$	400 (20x20)

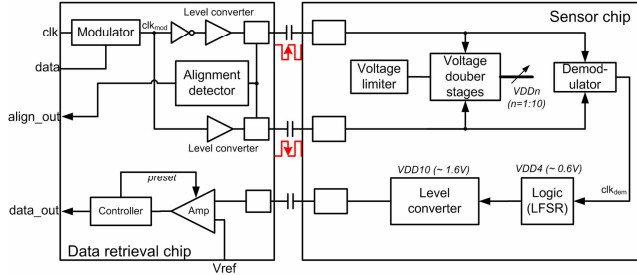


Figure 1: Block diagram of the capacitive coupling based sensor data retrieval system. The physical pad dimensions are summarized in the table.

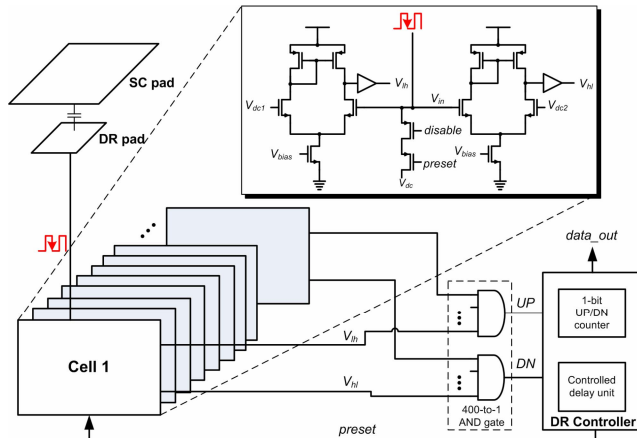


Figure 3: The self-setting loop for data sensing and recovery for the DR chip.

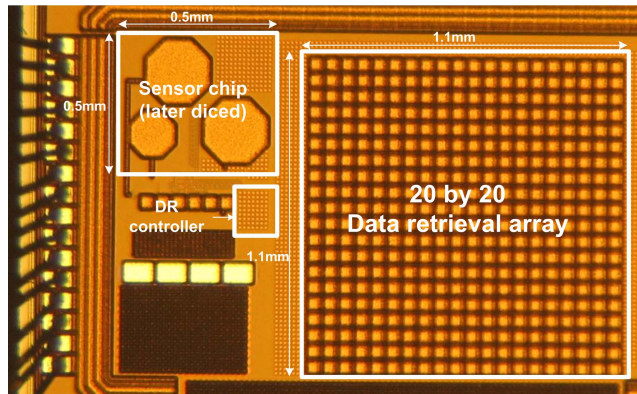


Figure 5: Die Macrograph

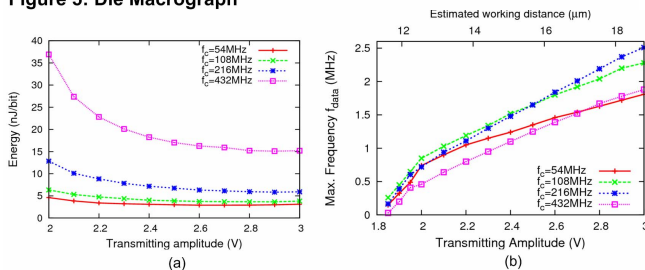


Figure 7: Measurement results. (a) Energy and (b) maximum operating frequency v.s. transmitting amplitude and carrier frequency f_c .

References

- [1] S. Hanson et al., IEEE Symposium on VLSI Circuits, Jun. 2007.
- [2] R. Drost et al., IEEE J. Solid-State Circuits, Sep. 2004.
- [3] A. Fazzi et al., ISSCC Dig. Tech. Papers, Feb. 2007.
- [4] R. Drost et al., ISSCC Dig. Tech. Papers, Feb. 2004.
- [5] R. Canegallo et al., ESSCIRC, Sep. 2005.

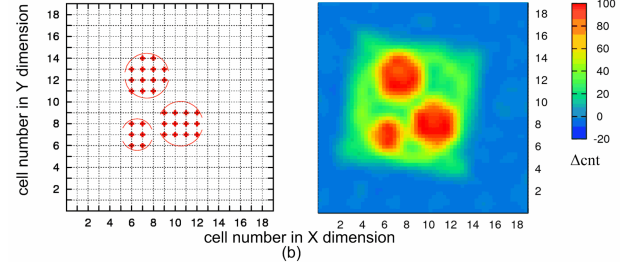
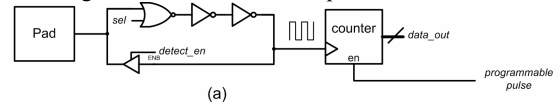


Figure 2: Alignment detection technique. (a) circuit diagram (b) measurement results represented by Δcnt and cluster of pads.

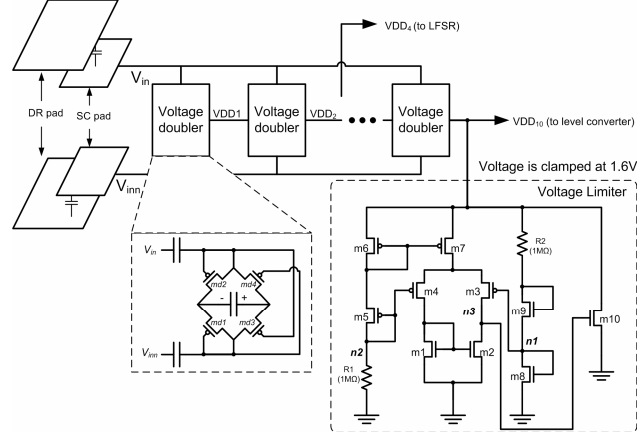


Figure 4: Voltage rectification and voltage regulation block diagram.

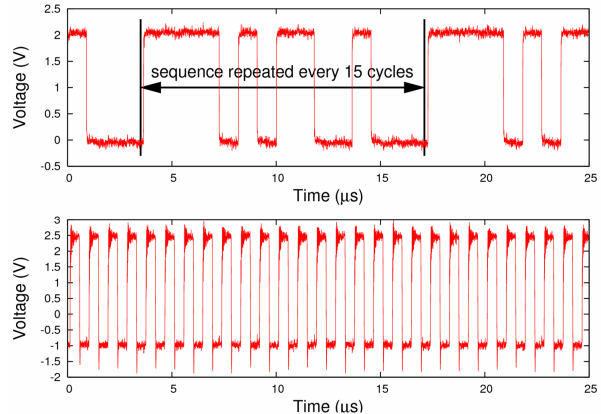


Figure 6: Measurement waveforms running at 1.1MHz.

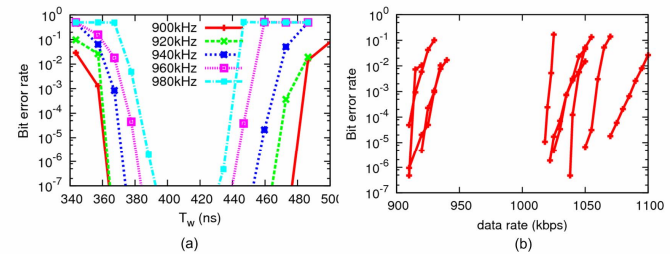


Figure 8: Measurement results. (a) BER v.s. the selection of the modulated clock window size, T_w (b) BER with 10 randomly dropped sensor location.