

### 19.3 A 150pW Program-and-Hold Timer for Ultra-Low-Power Sensor Platforms

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Lifetime and form factor are two critical concerns for emerging sensor platforms, particularly for applications such as implantable medical devices. The limited energy from power sources, typically either microfabricated batteries or scavenged energy, remains one of the biggest challenges for such platforms. Reducing power consumption can lower system volume and extend lifetime. To achieve very low power consumption aggressive voltage scaling has been applied in recent microsystems [1, 2]. The average power consumption of sensor platforms, which are often low duty cycle, can be greatly reduced by applying strong power gating while idling [3]. A key component in power gating is the timekeeping device while the system is in the idle mode. Since the timer is always active, it is often the dominant source for energy loss and must oscillate at a low frequency (e.g., from sub-Hz to 10Hz).

Crystal oscillators are widely used as a frequency reference for their insensitivity to temperature and supply variations. However, they operate at high frequencies and with considerable power consumption and they are unsuitable for sensor platforms due to their stringent power budgets and cost sensitivities. To reduce active power, a gate-leakage-based timer is presented in [4]. MOSFET gate leakage provides lower temperature sensitivity than other device leakage sources. However, gate-leakage models are inaccurate, making the timer behavior difficult to predict based on the past measurement data. More importantly, porting to other technologies is difficult since gate leakage varies by several orders of magnitude across technologies in use today.

In this work, a program-and-hold timer with temperature self-compensation is presented. The bias stage, hold stage, and oscillator stage are shown in Fig. 19.3.1. During the programming mode  $I_{ref}$  is used to bias transistor  $M_0$  and store the bias voltage on the hold stage. In the active mode  $I_{ref}$  is turned off to reduce power and the oscillator is biased by the sampled voltage. With a 200:1 ratio between  $M_1$  and  $M_0$ , the active power is greatly reduced. In most sensor applications, temperature varies slowly and therefore the programmed bias voltage remains valid for the next refresh cycle [5].

Figure 19.3.2 shows the detailed schematics of the bias and oscillator stages. The bias stage exploits a polysilicon resistor with low temperature coefficient. Transistors  $M_{d1}$ - $M_{d6}$  form a low-power voltage divider that provides a constant voltage  $nd3$ . A negative-feedback loop is formed by  $M_0$ ,  $A0$ , and  $R1$  so that  $n1$  tracks  $nd3$  and the drain current of  $M_0$  can be written as  $(V_{DD} - V_{n1})/R1$ , which is temperature independent. Bias transistors  $M_{n0}$  and  $M_{p0}$  are current-mirrored from transistor  $M_0$  through the hold stage. The N-stacked transistors provide a high-resistance path when switched off. Depending on the output state, charge is either injected into, or discharged from,  $C_1$ . Two comparators  $C0$  and  $C1$  are used to limit the voltage on node  $load$  to be between  $nd2$  and  $nd4$ , which are also defined by the voltage divider. The timer output is latched by the comparator outputs  $ss$  and  $rs$ .

The power consumption of the bias stage is mainly determined by the value of  $R1$ , leading to a trade-off between area and power during programming. To reduce power at a reasonable area, a hold stage is used to store the bias voltage so that the bias stage can be turned off in the active mode (idle mode of the sensor). On the left side of Fig. 19.3.3, the hold stage consists of a load capacitor  $C_1$ , two amplifiers  $A1$  and  $A2$ , and a programming transistor  $M_c$ . The program-and-hold operation can be understood by the waveform shown on the right side of Fig. 19.3.3. During the programming phase P1,  $A2$  is off while  $A1$  is turned on. The feedback loop forces  $bn2$  to follow  $bn$  by slowly charging  $C_1$  with the gate current of a thin-oxide transistor  $M_c$ . With thick-oxide input transistors,  $A1$  and  $A2$  do not contribute leakage to  $bn2$ . In calibration

phase P2,  $M_c$  is turned on to equalize voltages on nodes  $bn$  and  $bn1$ .  $A1$  is turned off during transition phase P3 to leave  $bn2$  floating. In P4, the timer enters active mode and the bias stage is turned off. Meanwhile,  $A2$  turns on to minimize the voltage difference between  $bn1$  and  $bn2$  to ensure that the gate current of  $M_c$  is several orders of magnitude smaller compared to that during P1.

A test chip is designed in 0.13 $\mu$ m CMOS. The timer is measured to have a nominal period of 0.09s at 600mV. At the beginning of the active mode, the normalized frequency with respect to temperature and supply voltage is shown on the left side of Fig. 19.3.4. Consistent trends are seen across  $V_{DD}$  with the frequency showing an inflection point around 50 to 60°C. Voltage sensitivity is 2% when reducing  $V_{DD}$  from 600 to 550mV. Supply noise is a minor concern for this application domain since very few logic blocks are switching during the active mode of the timer. The graph on the right side of Fig. 19.3.4 shows the average frequency for a range of refresh rates across temperatures. At 90°C, frequency reduces two times faster than at 0°C due to larger leakage. When refreshing the timer every 2 minutes the frequency deviation at worst-case temperatures is 5%.

The measurements in Fig. 19.3.4 are taken at a programming time  $T_{prog}$  (total time for P1+P2+P3) of 10s.  $T_{prog}$  is defined by the temperature-insensitive oscillator output that is directly controlled by  $bn$ . Figure 19.3.5 shows the timer behavior under different programming times. On the left,  $T_{prog}=1s$  is applied while refreshing the timer every 4 minutes. Three cycles are required to achieve the steady-state frequency due to the limited charge that can be provided by programming transistor  $M_c$  within the programming period. At the right of Fig. 19.3.5, the output frequency saturates when  $T_{prog}>15s$  and decreases as  $T_{prog}$  reduces. The timer cannot be programmed successfully at  $T_{prog}<1s$  due to insufficient time for properly biasing the circuits. The temperatures curves in the right plot are each normalized to  $T_{prog}=10s$  and show an additional 2% in frequency variation across temperature at  $T_{prog}=1s$ . Hence, by selecting  $T_{prog}=1s$ , a 10 $\times$  reduction in programming energy is obtained for less than 2% additional frequency variation.

Figure 19.3.6 shows the trade-off between refresh time and power consumption at  $T_{prog}=1s$ . At room temperature, programming power is 11nW and active power is 50pW. At a refresh time of 220s, the energy contribution from the programming and active modes are identical over the timer lifetime. The frequency deviation across temperature rises monotonically beyond 2 minutes refresh time. Choosing a refresh time between 2 and 4 minutes provides a good balance between frequency deviation and power consumption. The table at right of Fig. 19.3.6 summarizes this work and compares it to a previous low-power timer work using gate leakage [4]. At comparable power consumption, the presented program-and-hold timer exhibits smaller temperature and supply sensitivity and a more technology portable design at the cost of silicon area.

Figure 19.3.7 shows a die micrograph of the test chip fabricated in 0.13 $\mu$ m CMOS.

#### References:

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- [3] M. Seok, S. Hanson, Y.-S. Lin, et al., "The Phoenix Processor: A 30pW Platform for Sensor Applications," *IEEE Symp. VLSI Circuits*, pp. 188-189, June, 2008.
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- [5] National Oceanic and Atmospheric Administration, "Real-Time Meteorological Observation Network," Accessed on Dec. 4, 2008, <<http://www.glerl.noaa.gov/metdata>>.

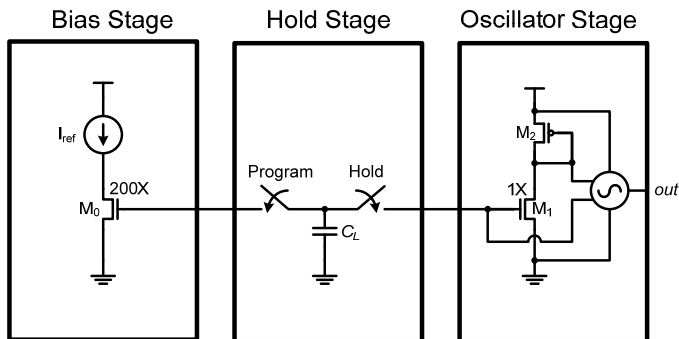


Figure 19.3.1: Block diagram of the presented timer.

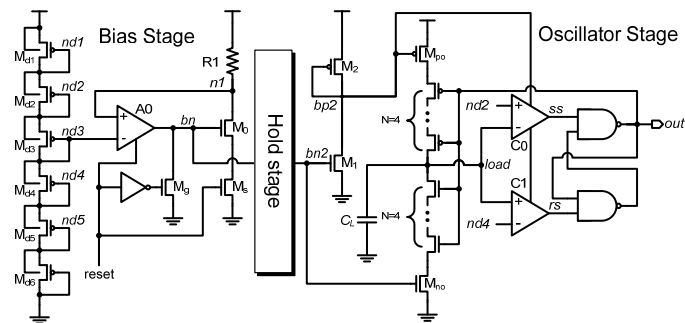


Figure 19.3.2: Schematics of the bias stage (left) and oscillate stage (right).

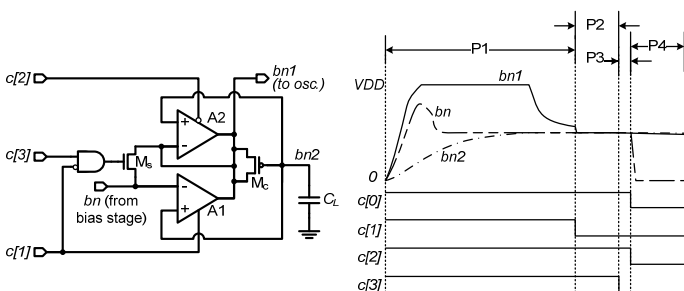


Figure 19.3.3: Schematic of the hold stage (left) and the timing diagram of the operation in each transition phase (right).

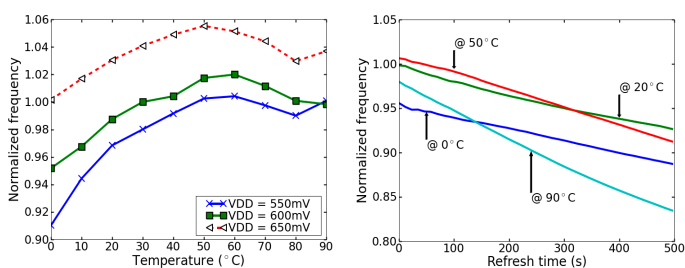


Figure 19.3.4: Measurement results of frequency variation caused by temperature: the oscillator frequency at the beginning of the active phase (left) and average frequency over different refresh times (right).

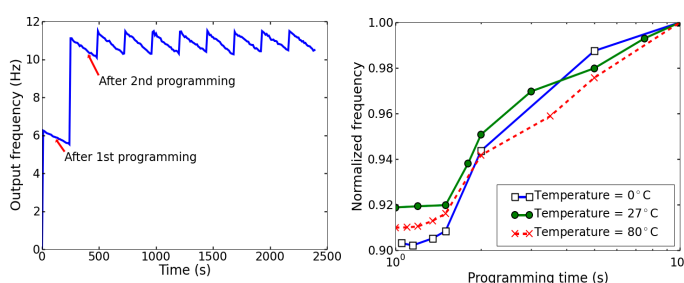


Figure 19.3.5: The output frequency as a function of time (left) and The frequency shift over the refresh cycle versus the programming time (right).

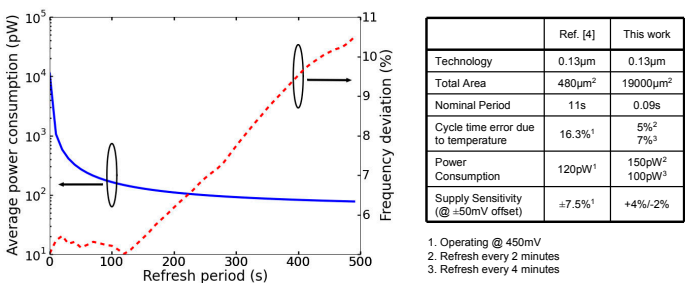


Figure 19.3.6: Trade-off between the temperature-induced frequency deviation and average power consumption (left) and comparison to a previous work [4] (right).

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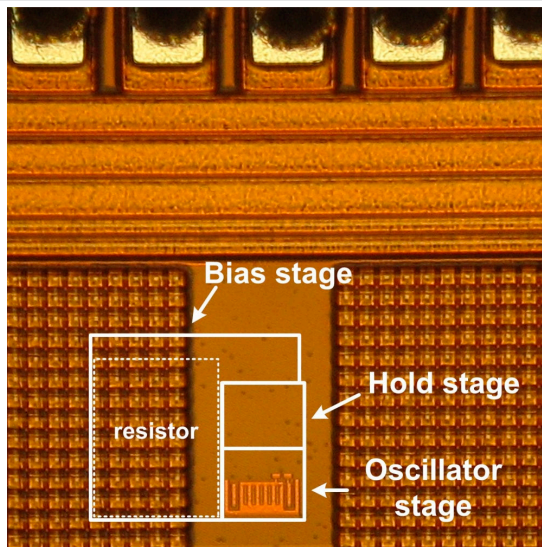


Figure 19.3.7: Die micrograph of the test chip fabricated in 0.13µm CMOS.