A Hybrid DC-DC Converter for Sub-Microwatt Sub-1V Implantable Applications

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Abstract

A DC-DC converter for sub-microwatt sub-1V loads is presented for efficient supply regulation of implantable devices powered by thin-film batteries. Using a hybrid, switched-capacitor architecture, it provides 444mV of DC output from a 3.6V DC source. Ultra-low power clock generation, level conversion, and linear regulation, combined with a unique startup circuit, enable a peak efficiency of 56% (4.6X ideal linear regulator) for loads from 5nA to 500nA. Fabricated in 130nm CMOS, it occupies 0.26mm^2.

Background and Motivation

Recent trends in low-power design have resulted in a new class of electronic systems using very low supply voltages constrained by miniscule power budgets. For example, the processors in [1-3] have energy optimal supply voltages of less than 500mV and consume power in the picowatt to nanowatt range. These processors are ideally suited for the battery-powered, implantable application space and require efficient DC-DC voltage conversion from the level of the battery to their supply. When considering size and integration, Lithium based thin-film batteries are particularly attractive. At the same time, they pose additional challenges owing to the relatively high output voltages of their chemistries, typically above 3V [4,5]. Such high input to output voltage ratios make pure linear regulation highly inefficient. Similarly, such light load power makes switching converters inefficient as well when using traditional techniques because clock and control power become dominant. To date, little work has been focused on this emerging design space. The closest design for comparison requires two input voltages of 1.2V and 1.8V and provides a variable 300mV to 1.1V output with 74% power efficiency (2.6X ideal linear regulator) under 5μW of loading [6]. The converter in this work targets one order of magnitude lower power loading, supports 2X higher input voltage, and realizes 56% power efficiency (4.6X ideal linear regulator) in a self-contained system that requires no off chip components and only a single battery connection.

DC-DC Converter Architecture

The converter in this work uses a monolithic hybrid approach consisting of a 5:1 Fibonacci switched capacitor network (SCN) in series with a low-dropout linear regulator as shown in Fig. 1. Theoretically, the ideal upper limit of power efficiency for such an arrangement is 62% assuming a 3.6V input. In order to approach this limit for loads of 250nW with an ideal 150nW of dissipation in the linear drop-out device, the power budget of the switched converter and peripherals was aggressively restricted to approximately 30nW. The resulting design outperforms a traditional linear regulator by an efficiency factor of 4.6X as shown in Fig 7. Several novel circuit techniques were key enablers in achieving this target, including a monostable multi-vibrator based oscillator to drive the SCN, a low power level converter for interfacing the SCN switches, and a startup methodology to reduce active mode power dissipation.

The SCN, shown in Fig. 2, consists of eleven MOSFETS and four 200pF dual-MIM capacitors. This topology and sizing allowed us to slow the clock from the typical MHz range down to 2kHz, thus aiding to meet the power budget without penalizing the SCN output voltage [7]. We efficiently generate this clock using a ring of multivibrator delay elements (MDE), shown in Fig. 3. Each MDE can be placed into an unstable state by asserting the set signal (S) high. When S transitions low, the MDE will remain in this unstable state while charge slowly leaks away from Q and /Q. After some delay, the cross-coupled transistors will begin to turn on and the MDE will quickly flip into its stable state. As a ring oscillator, this design is well tuned to our frequency range and provides full swing outputs with power levels one order of magnitude lower and supply sensitivities half that of inverter-based configurations.

The first startup circuit shown in Figs. 1 and 4 keeps the MDE oscillator in reset mode when the system is first connected to a power supply. Once the input voltage is of sufficient magnitude to support MDE oscillations, this startup circuit will toggle and release the oscillator from reset where it operates for several cycles in a high frequency, high power mode. The output of the SCN then quickly stabilizes, after which a second startup circuit switches the MDE supply from the battery to the SCN output as depicted in Fig. 8. A low-to-high level converter shown in Fig. 6 is used to boost the reduced MDE outputs back to the battery voltage thus preventing short-circuit current when underdriving the SCN switches. This boosting design relies on a periodic input signal and dissipates less than 300pW at 2kHz, a two orders of magnitude power reduction over a typical low-power DCVS structure, enabling high efficiency in driving the SCN.

The 720mV output of the SCN is regulated using the two-stage linear design shown in Fig. 5. A composite cascode differential pair is used to provide sufficient gain in the input stage under a stringent 5.2nA tail current [8]. The on-chip V_{th} based voltage reference is a low current design modified with thick-oxide NFETs to safely interface to the battery. This circuit provides stable 225mV and 444mV references over temperature, exhibits minimal supply sensitivity thus avoiding battery discharge dependency, and dissipates approximately 11nW of power.

Measurement Results

The DC-DC converter was manufactured in a 130nm bulk CMOS process in an area of 0.262 mm^2 (525μm x 500μm). All circuits, except for devices in the SCN, were placed under the MIM capacitors to save area, as shown in the die photo of Fig. 12. For stand-alone operation, all chips were verified to successfully run from a 3.6V lithium coin cell battery. Efficiency measurements are shown in Fig. 7 as a function of load current, and a peak efficiency of 56% was measured with a load of 285nA at 444 mV.

A second copy of the proposed design was used to provide observability for test and measurement. Using this version with a multiplexed off-chip reset signal, the MDE ring could be isolated and measured for power consumption, with the results shown in Fig. 9. Process variation resulted in slightly lower frequencies than expected, though not unreasonable for the 444 mV supply voltage. The output ripple distribution is plotted in Fig.10. Functionality of the startup circuit was measured as shown in Fig. 8 where the initial cycles of the MDE ring were observed using a digital output pad. As the SCN stabilizes, the MDE supply properly transitions to its normal, low power mode.

Sufficient load and line regulation for subthreshold processing was verified and is plotted in Fig. 8. The peak load regulation is 0.13%/nA at 2.5V. The peak line regulation is 0.05%/mV at 3.3V.

Table 1 summarizes the performance results of our measured converter as well as two competitive designs. The ability of our hybrid converter to efficiently handle large input to output voltage ratios makes it a particularly attractive option for low power, implantable systems where high voltage battery sources can be expected and high efficiency is required.

References

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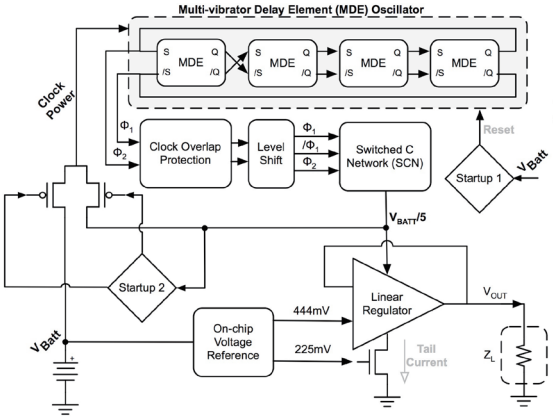

Figure 1. System level architecture - Startup 1 resets the MDE oscillator until V_{Batt} rises high enough. Startup 2 switched the MDE supply from V_{Batt} to $V_{Batt/5}$ once the system is stabilized.

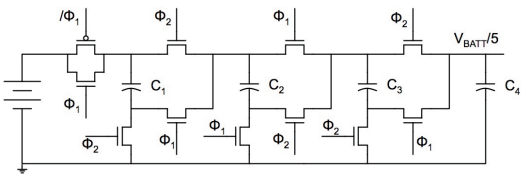

Figure 2. Fibonacci 5:1 switched capacitor network (SCN)

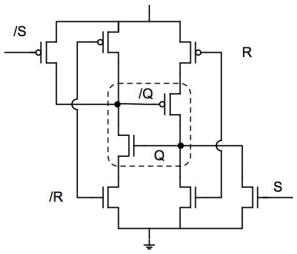

Figure 3. Single monostable multivibrator delay element

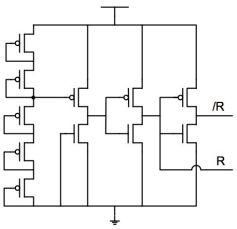

Figure 4. Startup circuit

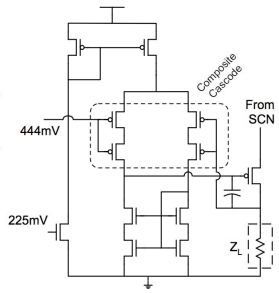

Figure 5. Linear regulator using composite cascode differential pair

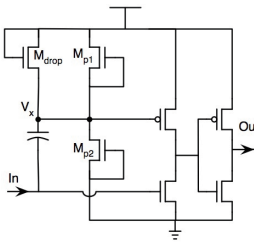

Figure 6. Low-power (300pW @ 2kHz) level converter from SCN output level to battery level

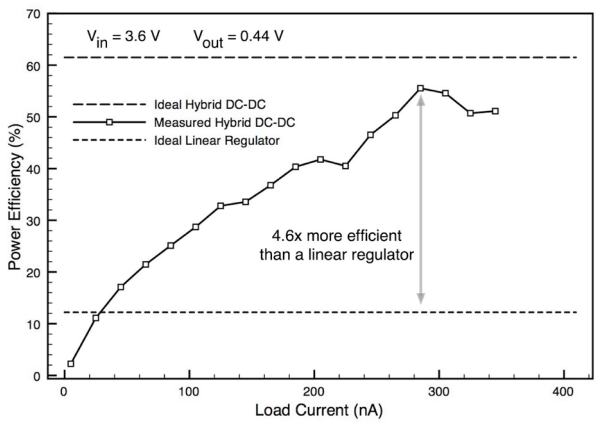

Figure 7. Converter efficiency vs. load current - for all loads above 25 nA, the proposed design outperforms an ideal linear regulator

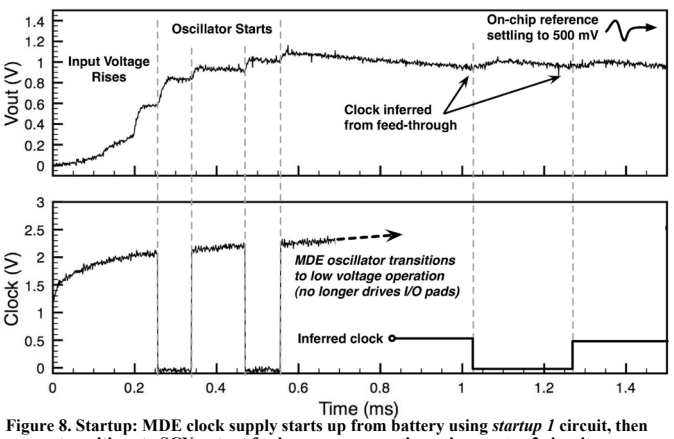

Figure 8. Startup: MDE clock supply starts up from battery using *startup 1* circuit, then transitions to SCN output for low power operation using *startup 2* circuit.

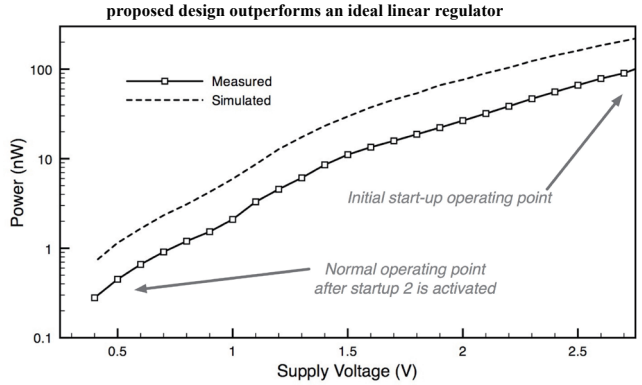

Figure 9. Simulated and measured MDE clock power vs. supply - after startup, the extremely low power of the MDE clock improves converter efficiency

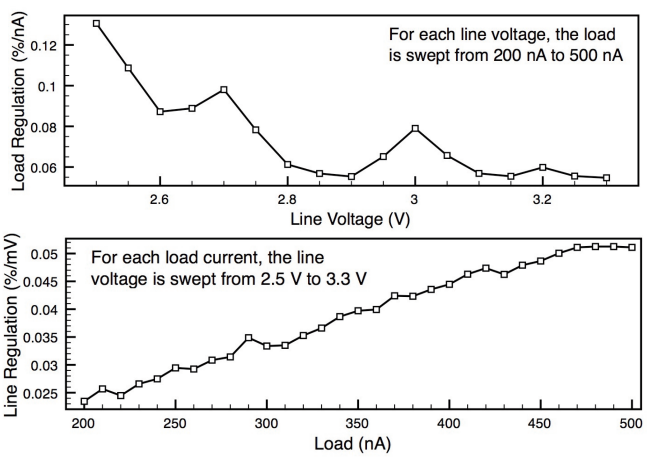

Figure 11. Load regulation vs line voltage and line regulation vs load current

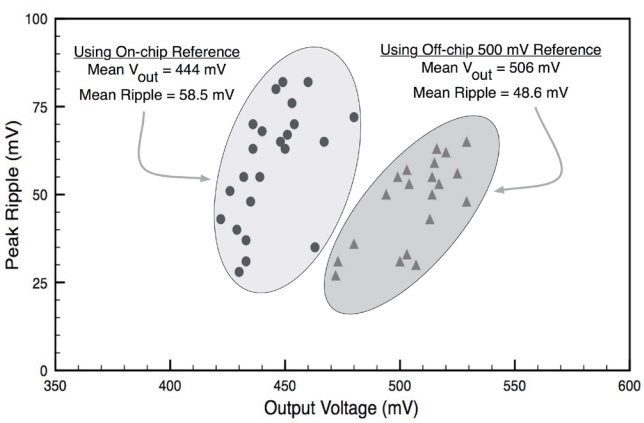

Figure 10. Scatter plot of ripple and output voltage for measured dies

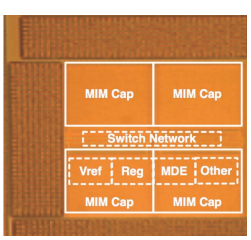

Figure 12. Chip micrograph

Table 1. Performance summary and comparison

Metric	This Work	[6]	[9]
Input Range	2.5-3.6 V	1.8 V	1.2 V
Output	444 mV	0.3-1.1 V	0.3-1.1 V
Load Range	2nW - 250nW	5µW - 1mW	1µW - 0.5mW
Clock Frequency	2 kHz	15 MHz	*NR*
Peak Ripple	< 50 mV	*NR*	*NR*
Peak Efficiency	56%	74%	78%
Efficiency gain vs. linear reg.	4.6X	2.6X	1.8X
Technology	130 nm	180 nm	65 nm
Area	0.26 mm^2	0.57 mm^2	0.12 mm^2

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