Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models

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ABSTRACT

Crosstalk delay-noise which occurs due to the simultaneous transitions of victim and aggressor drivers is very sensitive to their mutual alignment. Hence, during static noise analysis, it is crucial to identify the worst-case victim-aggressor alignment which results in the maximum delay-noise. Although several approaches have been proposed to obtain the worst-case aggressor alignment, most of them compute only the worst-case stage delay of the victim. However, in reality it is essential to compute the worst-case combined delay of victim stage and victim receiver gate [5, 9]. We propose a heuristic approach to compute the worst-case aggressor alignment which maximizes the victim receiver output arrival time. In this work, we use a novel *cumulative gate overdrive voltage* ($CGOV$) metric to model the victim receiver output transition. HSPICE simulations, performed on industrial nets to validate the proposed methodology, show an average error of 1.7% in delay-noise when compared to the worst-case alignment obtained by an exhaustive sweeping.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids; B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms

Algorithms, Design

Keywords

Crosstalk, delay noise, CSM

1. INTRODUCTION

Continuous scaling of device dimensions in the nano-meter regime has led to several key challenges in the timing verification of circuits. As the spacing between adjacent wires continues to shrink, the coupling capacitance now dominates the total wire capacitance. Furthermore, as technology advances, we are seeing increasing chip frequencies and decreasing voltage margins. All of the above trends exacerbate crosstalk noise which occurs due to the charge transfer between simultaneously-switching capacitively-coupled interconnects. Therefore, it has become imperative to accurately model the impact of crosstalk noise on circuit delay while performing signoff timing analysis of nano-meter designs.

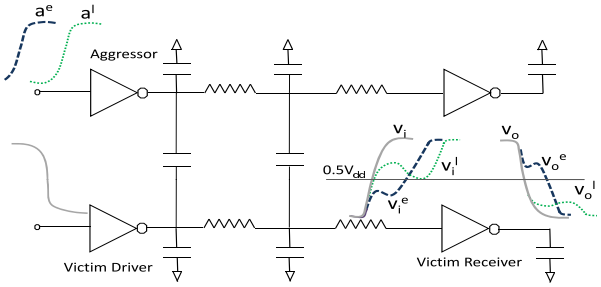

Figure 1: Aggressor alignment maximizes the victim receiver input delay

Besides crosstalk noise, we have several non-linear effects that must be modeled in order to accurately estimate the gate and interconnect delays. These effects include multiple-input switching, resistive and inductive interconnects, power-grid noise and non-linear receiver gate capacitances, etc. Traditionally, cell delays have been computed by using slew/capacitance based look-up tables or k-factor equations, where the output load is usually a lumped capacitance and the input transition is approximated by a ramp or other characterization waveform shapes [1, 2, 3]. In this framework, an iterative effective capacitance ($Ceff$) based technique was developed in [4] to model the resistive shielding effect observed in distributed interconnects. In [5, 11], the authors obtain a more accurate estimate of the crosstalk noise bump by accounting for the non-linearity of victim driver resistance. However, the above modifications are mostly ad-hoc in nature and may not be very accurate when they are all combined together to perform the timing verification of nano-meter designs. In contrast, current source-based models (CSM) have emerged as a more fundamental approach for performing timing analysis since they are independent of pre-characterized ramp input waveforms and lumped capacitive output loading. In [7], a CSM was proposed where the output current depends on the DC voltage levels of the input and the output pins and an extra capacitance was added to the output pin to account for the transient effects. In [9], it was shown that the CSM can be effectively used for performing crosstalk noise analysis.

Traditionally, the objective of delay-noise analysis has been to maximize (or minimize for MIN analysis) the victim stage delay. Under the linear superposition assumption, it was shown in [10] that the victim stage delay is maximized, for a rising victim transition, if the peak of the coupling noise

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bump (Vp) is aligned at the point where the noiseless victim waveform crosses the $0.5Vdd + Vp$ voltage level. However, the true objective of delay-noise analysis is not to maximize the victim stage delay, but to maximize the combined sum of the victim stage delay and the victim receiver gate delay. In other words, the worst-case alignment of aggressors should maximize the output arrival time of the victim receiver gate. We show with an example that maximizing the former quantity does not guarantee maximization of the latter. In Figure 1, we have a capacitively-coupled victim-aggressor network with a lightly loaded victim receiver gate. The victim input transition is fixed and the alignment of the aggressor input transition is varied. The noisy victim waveforms v_i^e and v_i^l correspond to the two aggressor transitions a_i^e and a_i^l respectively. It is can be noted that v_i^l has a later 50% crossing time (t_{50} or *arrival time*) and consequently a greater stage delay than v_i^e. However, the victim transition v_i^l (with the maximum stage delay) results in the output transition v_o^l for which the coupling noise arrives too late after it has finished switching. In comparison, the earlier victim transition v_i^e, which has a lesser interconnect delay, results in the victim output transition v_o^e having the latest arrival time. Hence, maximizing only the victim stage delay can sometimes be inaccurate and the worst-case aggressor alignment should be computed such that it maximizes the victim receiver output arrival time.

It was shown in [5] that the worst-case aggressor alignment is a non-linear function of victim slew rate, noise bump and victim receiver output loading. They proposed the use of pre-characterized look-up tables to identify the worst-case aggressor alignment which however requires additional overhead in cell library characterization. In [9], techniques of constrained optimization were used to obtain the worst-case aggressor-victim alignment with the objective of maximizing the victim output arrival time. However, this may require multiple non-linear simulations and can be expensive in terms of runtime overhead. In this work, we present a heuristic method to find the worst-case aggressor-victim alignment considering non-linear CMOS drivers. We propose the *cumulative gate overdrive voltage* ($CGOV$) metric as a proxy for the total victim receiver output current. We know that the rate of the victim receiver output transition is proportional to the amount of current sourced by the victim receiver gate. Hence, the alignment with the lowest $CGOV$ will result in the slowest output transition having the latest output arrival time. Using the $CGOV$ metric, we propose a heuristic approach to compute the worst-case aggressor alignment which maximizes the victim receiver output arrival time. Since the victim receiver output arrival time is estimated without actually simulating the output waveform, the proposed approach proves to be very runtime efficient. HSPICE simulations performed on industrial nets to validate the proposed methodology show an average error of 1.7% in delay-noise when compared to the worst-case alignment obtained by an exhaustive sweep.

2. PROBLEM DESCRIPTION

In this section, we analyze the problem of computing the worst-case crosstalk delay in a static timing analysis (STA) framework, where every net has a timing window representing the period within the clock cycle within which the net can switch. In [14], it was shown that victim alignment at the latest point in its timing window was optimal and always resulted in the latest victim output arrival time. In this work, we focus on the problem of computing the alignment of aggressors relative to the victim transition such that they satisfy their respective timing window constraints and produce the maximum delay-noise at victim output transition.

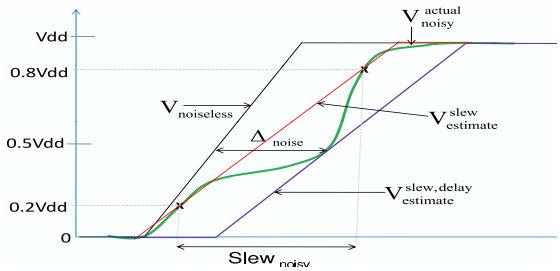

Figure 2: Waveforms at victim receiver input

It must be noted that the problem of computing delay-noise and timing windows are mutually dependent, since delay-noise depends on aggressor timing windows and timing windows are a function of the delay-noise coupled onto them. However, it was shown in [15, 16, 17] that this *chicken-and-egg* problem could be solved by updating the delay-noise and timing windows iteratively. In this paper, we consider the problem of computing the worst-case delay-noise, given the aggressor timing windows at some iteration of the outer loop.

As seen earlier, the worst-case delay-noise should maximize the victim output arrival time and not just the victim stage delay. The computation of victim output transition requires two steps, first the noisy waveform is computed at victim receiver input, second the victim receiver gate is simulated with the noisy input waveform. In cases where the victim net has a significant amount of coupling, the shape of the noisy victim waveform (e.g. V_{noisy}^{actual} in Figure 2) can be quite different from a ramp. [1] Such noisy victim waveforms waveforms cannot be used directly as inputs while simulating the victim receiver gate with traditional look-up table based cell delay models which are characterized with ramp input waveforms. Instead, an *equivalent ramp* is often fitted to noisy victim waveform and then used as the input transition for the victim receiver gate. Several heuristic approaches can be used to fit an equivalent ramp signal. One approach matches the slew rate of the noisy victim transition by fitting a ramp (i.e. $V_{estimate}^{slew}$ in Figure 2) through the 20-80% VDD voltage trip points of V_{noisy}^{actual}. For more conservative delay-noise analysis, the above ramp can delayed (i.e. $V_{estimate}^{slew,delay}$) such that its arrival time matches that of V_{noisy}^{actual}. It can be seen in the figure that $V_{estimate}^{slew,delay}$ under-estimates the actual waveform V_{noisy}^{actual} and results in a pessimistic victim output arrival time. Alternatively, the authors in [12] propose the use of an equivalent ramp which is closest to the noisy victim waveform in a weighted least-square sense. In [13], the authors obtain a *transition quantity* by integrating the area beneath the noisy victim waveform and use it as a metric to obtain an equivalent ramp waveform.

With traditional look-up table based delay models, it is not possible to compute the *exact* victim output waveform with arbitrary input waveforms. Although, aggressor alignment which maximizes only the victim stage delay can be optimistic, the use of equivalent ramp such as $V_{estimate}^{slew,delay}$ often guarantees an extra pessimism in delay-noise. Overall, the use of traditional look-up table based delay models can lead to erroneous results due to the inherent modeling approximations associated with it. This is especially true when there is a significant amount of coupling noise and the shape of the victim waveform significantly differs from a

[1] For simplicity of discussion, we will use a ramp as the representative waveform for all characterization waveform shapes.

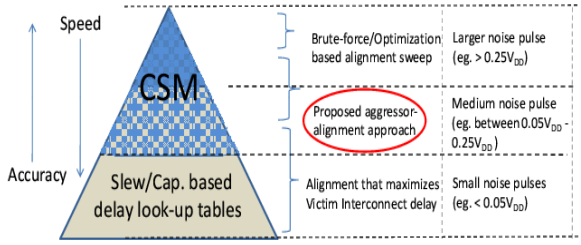

Figure 3: Proposed Methodology

ramp signal. In contrast, using current source driver models (CSMs), accurate victim output waveform can be computed even with arbitrary noisy input waveforms (e.g. V_{noisy}^{actual}). We already know that the aggressor alignment which maximizes the victim stage delay may not necessarily maximize the output arrival time. Therefore, to prevent *optimistic* delay-noise analysis in the CSM framework, we must instead find the alignment that maximizes the output arrival time.

Although, CSMs provide better accuracy over look-up table based delay models, they are computationally more expensive. Also, for victim nets with relatively small amount of coupling noise, delay-noise analysis with traditional models provide sufficient accuracy. Hence, in order to maximize the accuracy of delay-noise engine without significantly adding a runtime penalty, we propose the following noise analysis methodology (as shown in Figure 3). For the commonly occurring case of very small (e.g. $\leq$ 5% VDD) coupling noise bumps, we propose to use look-up table based delay models which are very fast and provide reasonably accuracy. Note that if the coupling noise bump is very small, then the amount of delay noise would correspondingly be small. Therefore, we do not require a very accurate delay noise engine in this region and the aggressor-alignment can be computed very quickly by maximizing only the victim stage delay [16]. However, for victim nets with relatively larger coupling noise, we propose the use of CSMs to accurately model the noisy victim waveforms and the worst-case alignment of aggressors is then computed such that it maximizes the victim output arrival time. In this work, we present a heuristic approach which accurately computes the worst-case aggressor alignment for relatively larger noise bumps (e.g. [5% , 25%] VDD). For even larger noise bumps (e.g. $\geq$ 25% VDD), we suggest the use of more accurate optimization techniques to compute the the worst-case alignment. However, with modern place-and-route tools, it is uncommon to have a large number of victim nets with such high amounts of coupling noise. Hence, we need to use the computationally expensive optimization engine only on a very small fraction of the entire design. Overall, we believe that the proposed methodology produces accurate results with very fast runtime.

The rest of the paper is organized as follows: In Section 3, we first explain the metric which can be used as a proxy for the total victim receiver output current. In Section 4, we then see how this metric is used to compute the worst-case aggressor alignment for both MIN and MAX analysis. In Section 5, we present results and compare the delay-noise obtained by using our proposed methodology with that obtained by doing worst-case input alignment. We finally conclude this paper in Section 6.

3. CUMULATIVE GATE OVERDRIVE VOLTAGE

In this section, we propose a metric to model the total victim receiver output current. The key observation is that the rate of victim output transition directly depends on the amount of current sourced by the receiver gate. Hence, we can use the total victim receiver output current as a proxy for the victim output transition. Therefore, we can solve for the *latest* occurring victim output transition without even simulating the victim output response. We first summarize the relationship between input voltage and the output current sourced by a CMOS inverter for a rising output transition

- The output current sourced by the driver is negligible if input gate voltage (V_{inp}) is less than the threshold voltage (V_{th})
- The output current sourced by the pull-up network of the driver is proportional to the gate *overdrive* voltage $(V_{inp} - V_{th})^{\alpha}$, for some $\alpha \in (1, 2)$ [18]

In this work, the total output current sourced by the CMOS driver is modeled by the *cumulative gate overdrive voltage* ($CGOV$) which is defined as the area between the input waveform and the gate threshold voltage [13] as shown in Figure 4.

$$CGOV = \int_{t_{inp}}^{t_{out}} (V_{inp} - V_{th})^{\alpha}\, dt \qquad (1)$$

Note that t_{inp} is the time when V_{inp} crosses the gate threshold voltage V_{th} which is a function of the threshold voltages of the transistors in the pull-up (pull-down) stack for a rising (falling) output transition. Similarly t_{out} is the time when the output waveform V_{out} crosses the target voltage level (V_{th}^{out}) of the output loading gate. Therefore, $CGOV$ actually models the total output current that is required to switch the output waveform to the level of the target voltage level V_{th}^{out}.

One can note that $CGOV$ for a certain gate is only a function of the gate output loading since it tracks the amount of output current that must be sourced for the output transition to switch upto a certain voltage level. In order to accurately compute $CGOV$, we need to model the dependence of output current on the gate output voltage and must also account for the effects of parasitic Miller coupling between gate input and output nodes. However, we see that even when the above mentioned second order effects are not modeled in equation (1), the $CGOV$ tracks the arrival time of noisy victim output transition very closely.

Consider the aggressor-victim coupled network shown in Figure 1. First, we fix the victim receiver and sweep all the other coupled-circuit parameters, such as victim/aggressor slew rates, driver sizes, victim interconnect coupling/ground capacitance etc. by randomly assigning their values. Then, we perform HSPICE simulations on each circuit and obtain

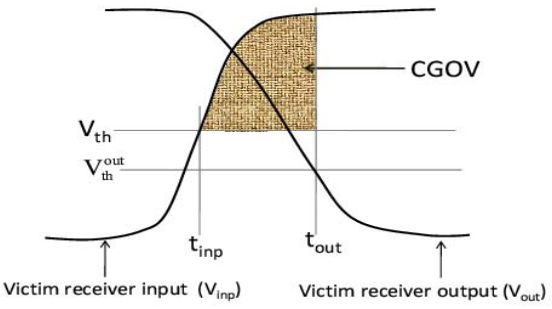

Figure 4: Cumulative Gate Overdrive Voltage

the corresponding noiseless v_i and the noisy v_i^l victim transitions. The histogram of ($\approx$ 1500 data points) noise peaks is shown in Figure 5. Finally, for every circuit, the respective $CGOV$ values were calculated by using equation (1) and integrating up to the arrival times of the corresponding victim output transitions, v_i and v_o, respectively. The gate threshold voltages were assumed to be 0.5VDD. Shown in Figure 5, is a scatter plot of $CGOV$ values obtained for the circuits. On the X(Y) axis, we plot the percentage error of $CGOV$ values with respect to the mean for the corresponding noiseless(noisy) victim transitions.

Since, the slew rate of v_i determines how fast the output v_o transitions, across all the circuits, we obtain different slew rates of the output transition v_o. We know that the output current has a dependence on the output voltage which is not modeled by $CGOV$ and can lead to errors in the computed $CGOV$ values. As seen in Figure 5, the magnitude of error denoted by the spread of 10% ([-3%,7%]) around the mean $CGOV$ is quite small. Also, recall that the objective of computing $CGOV$ is to use it for estimating the noisy victim output arrival time. Therefore, it is necessary for the $CGOV$ values of the noiseless v_i and noisy victim transitions v_i^l to track each other very closely. It can be seen in the figure that the maximum error in the corresponding $CGOV$ values across all circuits (denoted by the vertical distance from the 45^o inclined line) is only 1.23%. Hence, we conclude that the $CGOV$ metric is not very sensitive to coupling noise and remains fairly constant irrespective of the shape of the input transition. This observation allows us to compute $CGOV$ for the noiseless victim transition and use the same $CGOV$ value in tracking the noisy victim output arrival time.

4. WORST-CASE AGGRESSOR ALIGNMENT

A brute-force approach of computing the worst-case aggressor alignment would be sweeping the aggressor transition within its timing window and choosing that transition which results in the latest victim output arrival time. However, this requires multiple non-linear simulations of the coupled victim-aggressor network and is prohibitively expensive. In this section, we show how the worst-case aggressor alignment can be computed more efficiently using the $CGOV$ metric by using only a single non-linear simulation to obtain the noise bump. It was also seen earlier that $CGOV$ is very robust and is fairly insensitive to the aggressor alignment. Therefore, instead of performing multiple nonlinear simulations by sweeping the aggressor transition and simulating the victim output response, we propose to compute

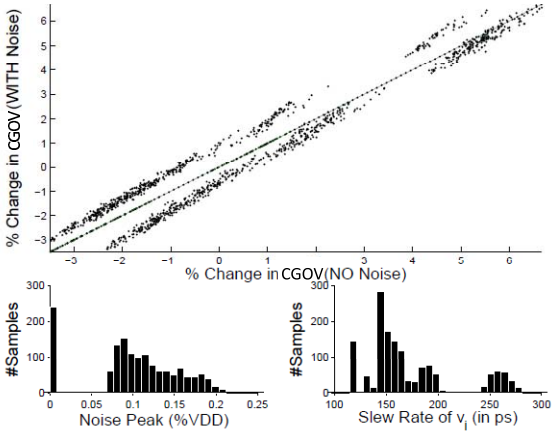

Figure 5: Scatter plot of $CGOV$.

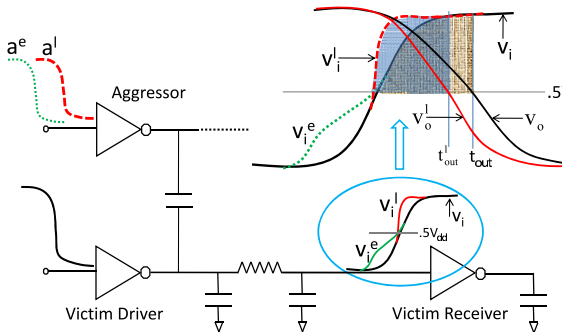

Figure 6: Worst-case alignment for MIN analysis.

$CGOV$ and use it as a proxy for the victim output arrival time.

Consider the case when both the victim and the aggressor drivers have a falling input transition as shown in Figure 6. We perform MIN analysis where we seek to find the aggressor transition which results in the earliest possible victim output arrival time. In order to do that, we first simulate the noiseless victim input and output transitions, v_i and v_o, assuming no switching at the aggressor input. We then compute $CGOV$ for the noiseless victim transition using Equation (1) and integrating up to the noiseless output arrival time t_{out}. In the previous section we showed that $CGOV$ is fairly insensitive to the input waveform shape. Hence, the $CGOV$ for noisy victim waveforms (e.g. v_i^l) can be assumed to be the same as that computed earlier for the noiseless transition v_i. Next, the noisy victim receiver input waveform (e.g. v_i^l) is obtained with a falling transition at the aggressor input. The victim receiver output arrival time can be estimated without actually simulating the victim output response. The unknown victim output arrival time (t_{out}^l) can instead be obtained by using v_i^l and integrating using Equation (1) until the $CGOV$ matches that of the noiseless waveform.

In Figure 6, we see the two noisy victim transitions, v_i^e and v_o^l, corresponding to the early (a^e) and late (a^l) aggressor transitions. It can be seen that the noise aligns early for the victim transition v_i^e and does not really affect the victim waveform above the threshold voltage level (assumed to be 0.5VDD in this example). On the other hand, the noise due to a^l aligns later and affects the victim waveform above the threshold voltage level and forces the output to transition faster. In this example, it can be seen that the later aggressor transition (a^l) results in a faster victim output transition v_o^l having an earlier output arrival time t_{out}^l. Finally, the worst-case aggressor alignment in MIN analysis can be chosen among all feasible aggressor transitions such that it results in the earliest arrival time at the output of the victim receiver. It is easy to see that the same technique can be used in the MAX analysis with mutually opposite aggressor-victim transitions. In this case, we sweep the aggressor transition within its timing window and use the $CGOV$ metric to choose the alignment which results in the latest arrival time (t_{out}) at the victim receiver output.

It is key to note that the proposed approach does not employ a non-linear CSM engine to simulate the victim receiver output response within every iteration. Instead, it computes $CGOV$ and uses it as a proxy for the victim receiver output arrival time. Therefore, this leads to a substantial speedup over approaches which employ expensive non-linear CSM based simulations. We will now see how further speed-ups can be obtained by using a linear superposition based frame-

work to compute the noisy victim receiver input waveforms corresponding to each aggressor alignment.

The proposed algorithm requires the enumeration of aggressor alignment within its timing window. With the use of optimization techniques, the number of such enumerations are typically small. Nevertheless, for every aggressor alignment, we would still need to perform expensive non-linear simulations using the CSMs to obtain the accurate noisy victim waveforms. Hence, to significantly reduce the computation overhead, we use the principle of linear superposition and combine the noiseless victim waveform with the coupling noise to obtain an estimate of the noisy victim response. It is well-known that the use of linear superposition can lead to an underestimation of the coupling noise peak, if the change in noise peak due to the non-linearity of victim driver is not modeled. However, it accurately estimates the pulse width of the noise waveform. Hence, although linear superposition under-estimates the noise peak, it doesn't necessarily under-estimate the time-to-peak of the noise which is needed to estimate the alignment. Therefore, the *CGOV* metric is not very sensitive to the non-linearity of victim driver resistance. In the results section, we show that the average error introduced by the superposition assumption is typically very less ($\approx 1.7\%$). Therefore, we make an engineering decision and use the principle of superposition to compute the noisy victim waveforms. Since, non-linear simulation using CSMs are performed only once in order to obtain the coupling noise and noiseless victim waveform, the proposed alignment approach is overall very fast.

In this paper, we have so far analyzed the case when the victim is coupled to a single aggressor. However, in a typical circuit, the victim net is often coupled to more than a single aggressor. In such cases, it is necessary to find the worst-case alignment of all the aggressors that are coupled to the victim such that it results in the maximum victim output arrival time. A heuristic often used to compute the relatively alignment among aggressors is that they are aligned such that all the noise peaks coincide and produces the largest cumulative noise peak. The cumulative noise bump is then optimally aligned with the victim waveform. In contrast, any other alignment among aggressors would result in a combined noise bump with a smaller noise peak and a wider pulse width. However, it was shown in [5] that using the noise bump with the largest noise peak resulted in an error which was less than 5% across exhaustive SPICE simulations. Therefore, in this work we have focused on the alignment of the cumulative noise bump with the victim transition such that the victim receiver output arrival time is maximized.

5. RESULTS

In this section, we will show experimental results that verify the accuracy and effectiveness of our proposed approach for computing the worst-case aggressor alignment. All experiments were performed on the fully coupled victim-aggressor circuit shown in the Figure 7 in $65nm$ technology node. The non-linear CMOS gates were simulated with detailed internal RC parasitics extracted from an industrial library. For the interconnect wire load model in the $65nm$ technology node [20], we assume a wire resistance $R = 0.5\Omega/\mu m$ and a wire ground capacitance $C_g = 0.2fF/\mu m$. We know that the coupling capacitance C_c is a function of the spacing and the relative amount of overlap between the aggressor-victim nets. If the victim-aggressor nets are routed very closely in the same metal layer, then coupling capacitance could account for a significant portion of the total wiring capacitance. Conversely, the magnitude of the coupling capacitance would be small if the victim-aggressor nets

Table 1: Parameters of the experimental victim-aggressor circuit

Parameters	Set of Parameter Values
Aggressor Driver Strength	(2X , 12X)
Aggressor Driver Input Slew (ps)	(10, 200)
Victim Driver Strength	(2X , 8X , 12X)
Victim Driver Input Slew (ps)	(10, 50, 100, 200)
Victim Interconnect Length (μm)	(5, 50, 100, 200)
Coupling scaling factor k	(0.5 , 1, 1.5, 2)
Victim Receiver Load (fF)	(1 , 10 , 50 , 200)

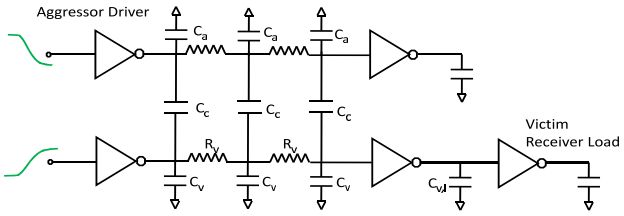

Figure 7: Experimental Victim-Aggressor Circuit

are routed at a relatively farther distance from each other. Therefore, in our experiments we treat the coupling capacitance C_c as a variable which is obtained by appropriately scaling the ground capacitance. In other words, $C_c = k * C_g$, where k is a scaling factor which ranges from $[0.5, 2]$ in our experiments.

The proposed approach of finding the worst-case aggressor alignment is validated on the victim-aggressor coupled circuit shown in Figure 7. However, in reality the representative circuit can have several variable parameters such as the type/strength of the victim-aggressor driver and receiver gates, the input slew rates, the interconnect length, the coupling capacitance scaling factor (k), the amount of receiver loadings, etc. In order to adequately sample the above mentioned parameter space, we perform a total of about 1500 simulations by sweeping the parameter values (shown in Table 1).

In each simulation, we compare the accuracy of our proposed approach with the *golden* aggressor alignment obtained by using HSPICE based brute-force enumeration. The aggressor transition was enumerated with a discretization step size of $2ps$ and HSPICE simulations were performed to simulate the victim receiver output response for every aggressor alignment. Finally the aggressor transition which resulted in the latest victim output arrival time was reported. In comparison, the proposed approach computed the worst-case aggressor alignment by using the *CGOV* metric to predict the victim output arrival time. Once, the aggressor alignment is computed, HSPICE was used to simulate the victim receiver output response. In order to evaluate the accuracy, we express the difference in the victim receiver output arrival time (w.r.t. golden) as a percentage of the worst-case delay noise at the victim receiver output. A histogram of the percentage error in delay noise obtained across all simulations is shown in Figure 8 for MAX analysis, when the victim receiver gate is an inverter. It can be seen that the proposed approach accurately estimates the worst-case aggressor alignment since we observe an average error of 0.75% across all simulations.

Earlier we claimed that aggressor alignment which maximizes the victim receiver *input* arrival time does not necessarily maximize the victim receiver *output* arrival time. To validate the above claim, we performed a similar brute-force enumeration and computed the aggressor alignment which

maximizes the victim receiver input arrival time (referred to *INP Align* in Table2). Using the above computed aggressor alignment, we simulate the victim receiver output transition and finally compare the percentage error in the output arrival time w.r.t golden obtained earlier. The histogram of the errors for inverter receiver gate (Input alignment in Figure 8) shows that about 20% of the cases report an error of 100% in delay noise. These cases occur when the input alignment results in a coupling noise which aligns too late with the victim transition (as shown in Figure 1). Overall, it can be seen that the proposed approach performs much better than the brute-force input alignment enumeration. This establishes the significance of considering the victim receiver gate in the computation of the worst-case aggressor alignment.

We repeat the above experiment for different victim receiver gates and in Table 2 we show the average % error in delay noise w.r.t. golden. It can be seen that the proposed approach accurately computes the worst-case aggressor alignment across different receiver gates. It can be noted that even with the stack-effect, the proposed approach is more accurate than the input alignment enumeration. Across all simulations, the average error of the proposed approach is 1.7% compared to an error 8.49% obtained with the input enumeration approach.

6. CONCLUSIONS

In this paper, it was seen that worst-case aggressor alignment must be computed such that it always maximizes the victim receiver output arrival time. In order to model the victim receiver output waveform, we define and use the cumulative gate overdrive voltage (*CGOV*) metric to model the total victim receiver output current. Since, the victim receiver output transition directly depends on the amount of current sourced by the receiver gate, the alignment with the lowest *CGOV* would correspondingly lead to the slowest transition having the maximum delay. HSPICE simulations, performed on industrial nets to validate the proposed methodology, show an average relative error of 1.7% in delay-noise when compared to the worst-case alignment obtained by an exhaustive sweep.

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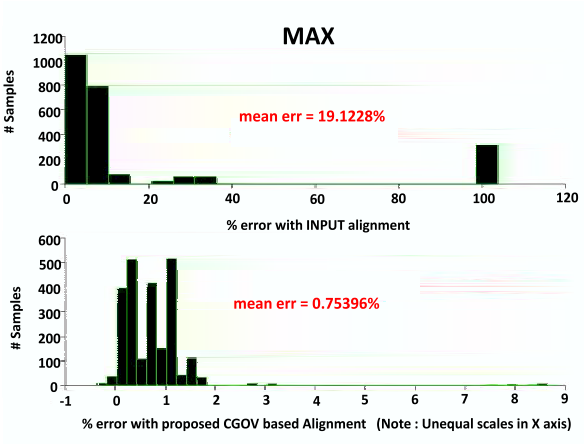

Figure 8: Histogram of % error in delay noise with INVX receiver gate for MAX analysis

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Table 2: Percentage errors in delay-noise wrt golden

	RISE MAX		FALL MAX		RISE MIN		FALL MIN	
Receiver	CGOV Align	INP Align	CGOV Align	INP Align	CGOV Align	INP Align	CGOV Align	INP Align
INV	0.77	7.24	0.75	19.12	-2.32	-6.66	-2.10	-6.36
NAND4X	0.35	7.34	4.41	5.11	-2.99	-12.87	-3.07	-4.50
NOR4X	3.85	5.36	1.38	8.36	-3.35	-7.39	-2.23	-12.31
BUF	0.26	8.34	0.31	8.42	-1.67	-7.20	-1.34	-9.87
AND4X	0.29	8.36	1.86	8.19	-1.51	-6.14	-1.07	-8.75
OR4X	1.46	7.63	0.37	9.92	-0.99	-6.06	-2.23	-12.40