15.8 Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells

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Sensors with long lifetimes create new applications in medical, infrastructure and environmental monitoring. Due to volume constraints, sensor systems are often capable of storing only small amounts of energy. Several systems have increased lifetime through V_{DD} scaling [1][2][3]. This necessitates voltage conversion from higher-voltage storage elements, such as batteries and fuel cells. Power is reduced by introducing ultra-low-power sleep modes during idle periods. Sensor lifetime can be further extended by harvesting from solar, vibrational and thermal energy. Since the availability of harvested energy is sporadic, it must be detected and stored. Harvesting sources often do not provide suitable voltage levels, so DC-DC up-conversion is required.

An 8.75mm^3 sensor platform capable of nearly-perpetual operation is proposed. The system includes a 73kHz near-threshold ARM Cortex-M3 core that is powered by two series-connected 1mm^2 solar cells and a Cymbet thin-film solid-state Li battery through an integrated power management unit (PMU) (Fig. 15.8.1). It is suitable for volume-constrained long-term wireless sensing applications such as intraocular pressure monitoring to detect and track the progression of glaucoma. In the 7.7µW active state, the system collects data from on-chip temperature and capacitance sensors, performs data processing using a 16kb non-retentive SRAM (NR-SRAM) for temporary storage and writes the results to a 24kb retentive SRAM (R-SRAM) (Fig. 15.8.2). Between sensor measurements the system enters a 550pW sleep state by disabling SRAM accesses, power gating the Cortex-M3 and NR-SRAM and switching the PMU to sleep mode. While asleep, the R-SRAM, wakeup controller and sleep timer are powered by a 50Hz switched capacitor network (SCN) that converts energy from the solar cells and battery. If sufficient light is available, solar energy is used to recharge the battery. When the next sensor measurement is scheduled, the wakeup controller switches the PMU to active mode by enabling a 1.2MHz clock for the SCN and a linear regulator (LR). Then power gating is disabled, allowing data collection and processing to begin.

The Cortex-M3 achieves 73kHz operation at 400mV and 1MHz at 500mV while running a 64-point DFT program (Fig. 15.8.3). The energy-optimal point for active mode operation is 2.1µW at 400mV, because further voltage scaling increases total energy consumption due to excessive leakage [4]. During sleep mode, the processor and NR-SRAM are power gated. When the system enters active mode mode, the Cortex-M3 begins program operation with pointers retained through sleep mode that denote the program location and allocated R-SRAM for sensor measurements. The sleep power is 100pW at 400mV and 460pW at 500mV, including R-SRAM, wakeup controller and balloon latch leakage plus sleep timer switching power. The idle processor lifetime is 49 years based on the 12µAh 2.9mm^3 Cymbet battery, which included in the system volume of this work.

A custom SRAM was developed to minimize leakage power during sleep mode while maintaining sufficient speed during active mode (Fig. 15.8.4). The R-SRAM bitcell uses HVT PMOS pass gates for 50% higher sub-V_{TH} performance than HVT NMOS devices. HVT devices and increased gate lengths are used for the cross-coupled inverters. A 4T read buffer is used to prevent erroneous RBL discharge that can occur with the 2T buffer in 8T bitcells [5]. A hierarchical BL scheme enhances read functionality and speed. While sleeping, the BLs are intentionally left floating to reduce leakage by 20% and the WLs are held high to prevent data loss. The read buffer is power gated with an HVT NMOS header, which is overdriven by the battery in active mode to increase speed. Using only the above techniques, leakage power savings are obtained but slow write speed is inevitable. To increase write speed by 250%, the BLs are boosted with V_{BOOST}, which is the readily-available unregulated output of the SCN. V_{BOOST} also reverse body biases unaccessed pass gates to reduce BL leakage. The R-SRAM has a bitcell area of 17.48µm^2 and is measured to consume 3.3fW per bit at 0.4V. This bitcell is 57% smaller and consumes 69% less leakage power compared to [1]. The processor includes 12 2kb banks of R-SRAM that can be shut down individually when unused and 8 2kb banks of 10T NR-SRAM that use only SVT devices and are power gated during sleep.

In the PMU a ladder SCN divides the 3.6V battery voltage by 6, generating V_{SCN} (Fig. 15.8.5). The SCN uses 1.2MHz 1.2V non-overlapping clocks and level converters, for a net 8.3x energy improvement over full-swing clocks. V_{DD} for the clocks it is generated with a 5nA-biased control linear regulator (CLR). Level converters are implemented as SRAM bitcells with zero-V_{TH} (ZVT) pass gates. The PMU down-conversion efficiencies are 2.5x and 1.7x better than ideal linear regulation in active and sleep modes. Since Cortex-M3 workload varies, the SCN is only clocked on-demand (Fig. 15.8.6), reducing clocking parasitics and increasing efficiency by up to 20%. V_{SCN} is kept sufficiently high for the LR dropout by comparing the divided V_{SCN} level to V_{REF}, an 8pA reference with low V_{DD} and temperature sensitivity [6]. V_{SCN} powers the 30nA-biased LR, with output voltage set by V_{REF}. A temperature-compensated voltage reference was also designed to reduce Cortex-M3 frequency variation with temperature. Several previous PMUs for low-power sensor systems either did not have linear regulation, resulting in noisy supply voltages [2], or did not provide high load regulation [7].

During sleep mode the quiescent current of the PMU decreases to maintain efficiency. Since V_{DD} noise is tolerated as long as state is retained, the LR is power gated and V_{DD} is powered directly by the SCN, eliminating bias currents and dropout losses. The SCN is clocked with a 50Hz 63pW leakage-based oscillator (Fig. 15.8.5) [7]. When the inputs to an oscillator delay element switch, all devices are momentarily turned off. The outputs float away from the supply rails, initiating a positive feedback loop that switches the outputs with 2× less frequency variation than an iso-energy current-starved ring oscillator. The bias current on the CLR is reduced to 50pA. Again, the SCN is clocked on-demand to compensate for varying system leakage due to temperature and other environmental changes. The system could run for 5 years on the energy in the battery without recharging with a usage profile where one measurement requiring 10k instructions is taken every hour.

The PMU harvests solar energy with the same SCN used for down-conversion. Two 1mm^2 solar cells are fabricated in a 0.18µm CMOS process, diced and wire bonded in series to the V_{SCN} node of the PMU. The solar monitor examines SCN node voltages and the divided battery voltage level to determine when sufficient sunlight is available to recharge the battery. When this condition is met, the fast SCN clock is enabled and solar energy is up-converted to the battery. Canary solar cells are included in the system to designed to implement a fractional-V_{OC} biasing circuit for optimal solar cell efficiency. When light intensities are insufficient to recharge the battery, solar energy can still be used to power the system. If the sensor system requires 10k instructions per sensor measurement, it can take 15k measurements on a sunny day with no net energy use, offering nearly-perpetual operation for volume-constrained long-term sensing applications.

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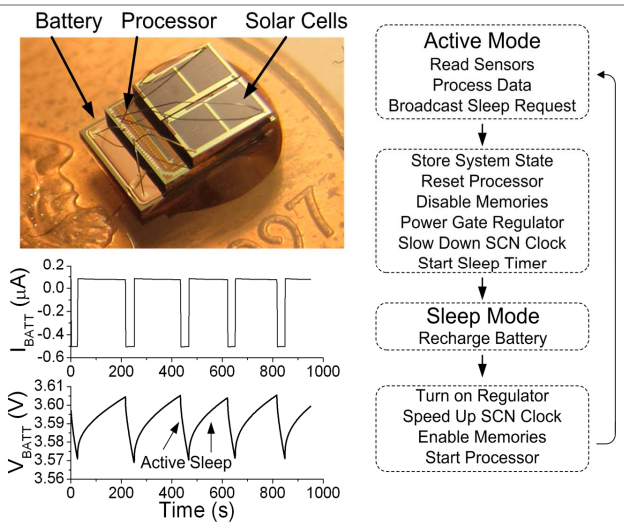

Figure 15.8.1: System photo and measured waveforms for a nearly-perpetual sensor with solar cells, battery, and processor.

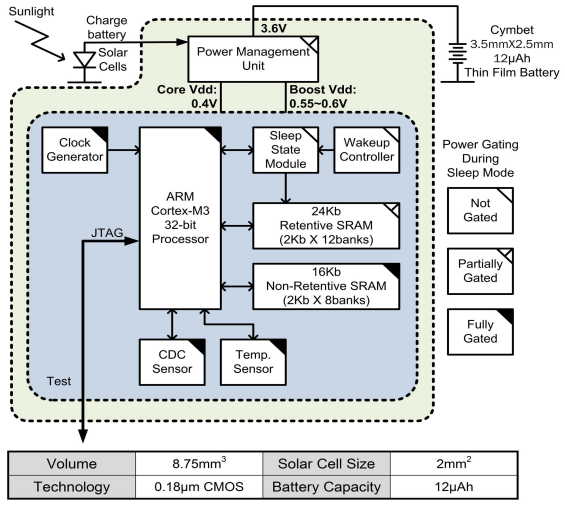

Figure 15.8.2: Sensor data is processed by an ARM Cortex-M3 processor and stored into the R-SRAM during sleep.

	[1]	[2]	[3]	This Work
Process	0.18 µm CMOS	65 nm CMOS	0.25 µm CMOS	0.18 µm CMOS
Vt	0.4V	-	0.55V	0.4V
Vdd	0.5V	0.5V	1V	0.4V/0.5V
Energy	2.8 pJ	27.2 pJ	12 pJ	28.9 pJ/37.4 pJ
Leakage	35.4 pW	1 uW	13-20 nW	100 pW/460 pW
Processor	8 bit	16 bit	8 bit	32 bit
Frequency	106 kHz	434 kHz	500 kHz	73 kHz/1 MHz
RSRAM	0.33 kB	16 kB	3.125 kB	3 kB
System Volume	n/a	n/a	16 mm^3	8.75 mm^3
Idle Lifetime	139 years	42 hours	138 days	49 years

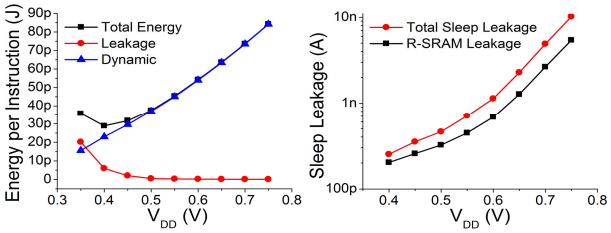

Figure 15.8.3: The Cortex-M3 is measured at 73kHz and 28.9pJ per instruction with 100pW sleep for a 49 year idle lifetime.

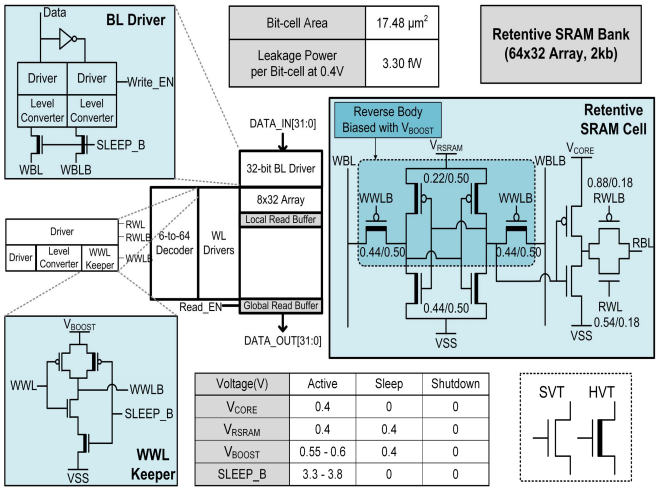

Figure 15.8.4: 64x32 R-SRAM banks use HVT devices for ultra-low sleep power and BL boosting for higher performance.

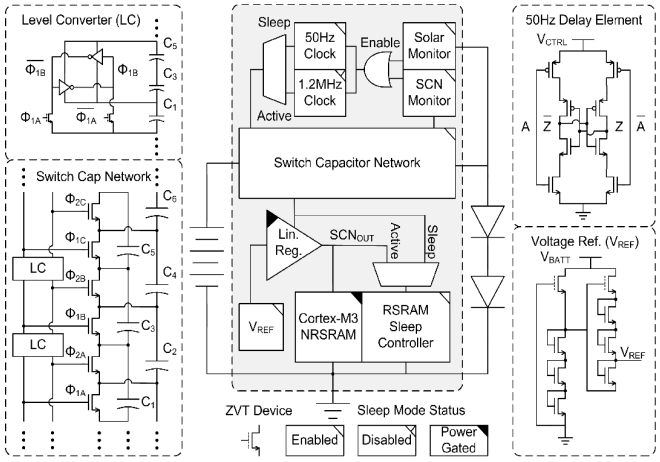

Figure 15.8.5: The PMU is co-optimized for active, sleep and harvest modes. The active lifetime is 5 years without harvesting.

	This Work (Active)	This Work (Sleep)	[2]	[7]
Conversion Ratio	9:1	9:1	4:1	8:1
Efficiency Improvement over Ideal Linear Regulation	2.5x	1.7x	1.9x	4.6x
Load Regulation	1.3%	1.5%	-	3.9%

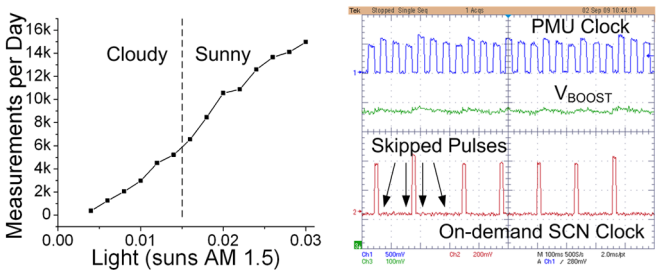

Figure 15.8.6: Energy harvesting enables 15k sensor measurements on a sunny day with no net energy loss in the system.