A Power-efficient 32bit ARM ISA Processor using Timing-error Detection and Correction for Transient-error Tolerance and Adaptation to PVT Variation

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Razor [1-3] is a hybrid technique for dynamic detection and correction of timing errors. A combination of error detecting circuits, and micro-architectural recovery mechanisms creates a system which is robust in the face of timing errors, and can be tuned to an efficient operating point by dynamically eliminating unused guardbands.

Canary or tracking circuits [4-5] can compensate for certain manifestations of PVT variation, however they still require substantial margining to account for fast-moving or localized events, such as Ldi/dt, local IR drop, capacitive coupling, or PLL jitter. These types of events are often transient, and while the pathological case of all occurring simultaneously is extremely unlikely, it cannot be ruled out. A Razor system can survive both fast-moving and transient events, and adapt itself to the prevailing conditions, allowing excess margins to be reclaimed. The savings from margin reclamation can be realized either as a per device power efficiency (higher throughput same VDD, same throughput lower power), or as parametric yield improvement for a batch of devices.

Error-detection in Razor is performed by specific circuits which explicitly check for late arriving signals. Error correction is performed by the system using either stall mechanisms with

corrected data substitution, or by instruction/transaction-replay. Measurements on a simplified Alpha pipeline[2] showed 33% energy savings. In [3], the authors evaluated error detection circuits on a 3-stage pipeline, using artificially induced Vcc droops showing 32% throughput (TP) gain at same Vcc, or 17% Vcc reduction at equal TP.

This paper presents Razor applied to a processor which has timing paths that are representative of an industrial design, running at frequencies over 1GHz, where fast moving and transient timing-related events are significant.. The processor implements a subset of the ARM ISA, with a micro-architecture design which has balanced pipeline stages resulting in critical memory access, and clock gating enable paths. The design has been fabricated on a UMC[6] 65nm process, using industry standard EDA tools, with a worst case STA signoff of 724MHz. Silicon measurements on 63 samples including split lots show a 52% power reduction of the overall distribution for 1GHz operation. Error-rate driven dynamic voltage (DVS) and frequency scaling (DFS) schemes have been evaluated.

The micro-architecture is shown in (Fig. 1). The pipeline is balanced using a combination of up-front micro-architecture design and the low level path equalization performed by backend tools, such that all stages have very similar critical-path delay. The pipeline is conventional except for the S0 and S1 stages, which allow time for Razor qualification before instruction commit. The pipeline includes forwarding and interlock logic, which contributes to both data and control critical paths, including clock gate enables, and memory access paths. Timing errors on these types of paths cannot be recovered using a shadow latch, and error recovery consists of flushing the pipeline and restarting execution from the next un-committed instruction.

The TD (Fig.2) detects errors by generating a pulse in response to a transition at the D input and capturing this pulse it within a window defined by a clock-pulse (CP) generated from

the rising-edge. The sizing of the devices in the inverter and AND gates in the pulse-generators determines the width of the data pulse (DP). A delay on CK defines the width (T_{CK}) of the implicit CP, which is active when N1 and N2 are both on. Detection begins (ends) when the trailing (leading) edge of DP overlaps with the leading (trailing) edge of CP. The error detection window is $T_D+T_{CK}-2T_{OV}$, where T_{OV} is the minimum overlap required. The min-delay constraint is $T_{CK}- T_{OV}$ which is less than the high clock-phase of previous designs [2]. The trade-off is increased pessimism, as the point at which transitions are flagged as errors is moved earlier. For 1GHz operation, this pessimism corresponds to ~5% of the cycle time, compared to the actual frequency where incorrect state starts to be latched.

An error history (EHIST) diagnostic bit was added to each TD using an RS-latch, set whenever an error occurs. Reading out the EHIST allows identification of each TD that triggered over the course of a test.

Fig. 3 shows the die layout and implementation details. Simulation of a typical workload (WTYP) shows power overhead due to TD was 5.7% of the overall power with 1.3% overhead due to min-delay buffers. STA sign-off was 724MHz at the worst case corner (0.9V/SS/125C).

Fig. 4 shows throughput (TP) versus frequency and number of failing TDs as well as EHIST map for WTYP at 1.1GHz and 1.2GHz. The TP linearly increases with frequency until the Point of First Failure (PoFF). Thereafter multiple errors occur due to the balanced nature of the pipeline and the TP degrades exponentially. The PoFF for TYP code occurs at 1.1GHz, a 50% TP increase compared to the design point of 724MHz. Execution is correct until 1.6GHz, after which recovery fails.

DFS experiments used an on-die Adaptive Frequency Controller (AFC) which adapts to the dynamic workload variation by changing frequency in response to error-rate. Fig. 5 shows

the AFC structure and response for a workload with 3 phases – a NOP loop, a combined critical path/power virus loop (PV), and typical workload (WTYP), running at a fixed 1V VDD. Highest frequency is measured in the NOP phase (1.2GHz) and the lowest in the PV phase (1GHz). In the TYP phase, there are 4 distinct frequencies (1143 - 1068MHz). This is due to a wider range of paths being exercised compared to the synthetic test cases.

Fig. 6 shows the same 3-phase workload using an adaptive Razor voltage controller at a fixed 1GHz frequency for 3 samples. It can be observed that using Razor with the worst-case PV code on the slowest (SS6) part requires 1.17V, whilst the typical workload requires 1.07V, which is below the 1.1V overdrive limit of the process. If we consider the parametric yield implications then without Razor conventional margining requires operation above 1.2V (3% VDD margin over PoFF) to achieve 100% yield at 1GHz, for reliable WC operation of SS6. This is unlikely to be sustainable due to power and wear-out implications of excessive overdrive. Fig. 7 shows the comparison between a baseline of 1.2V and Razor tuned voltages. The max power for the 1.2V distribution is due to the FF5 part, and is 52% higher than the Razor distribution, with a spread of 37mW compared to10mW.

An alternative to dynamic adaptation is to discard slower parts or reduce the max frequency specification. As 6 out of 22 of our typical lot samples require more than 1.1V for the PV, discarding slower parts would almost certainly impact yield. Reducing the clock frequency to a point where yield was not impacted would limit the operation frequency to 800MHz. For the same distribution Razor provides potential for an effective 100% yield point at 1GHz, with supply voltage kept at or below 1.1V for all devices, except for extremely rare use cases equivalent to the pathological WC PV code.

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[6] UMC, United Microelectronics Corporation, http://www.umc.com/

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Figure 7: Measured power for SS6, TT9 and FF5. FF5 is the max-power outlier at the 1.2V worst-case voltage point. With Razor enabled, SS6 becomes the worst-case chip due to higher PoFF. 52% savings on the worst-case power is realized with Razor. Limiting the baseline over-drive voltage to 1.1v causes a yield impact as some typical chips fail to operate correctly at 1.1v.

Supplemental Figure 1: Razor voltage controller response during code-transition. a) Error-rate spikes going from NOP to PV. Voltage is increased in proportion to error-rates. b) From PV to the WTYP workload, the error-rate drops to 0. Voltage is gradually reduced until errors resume.

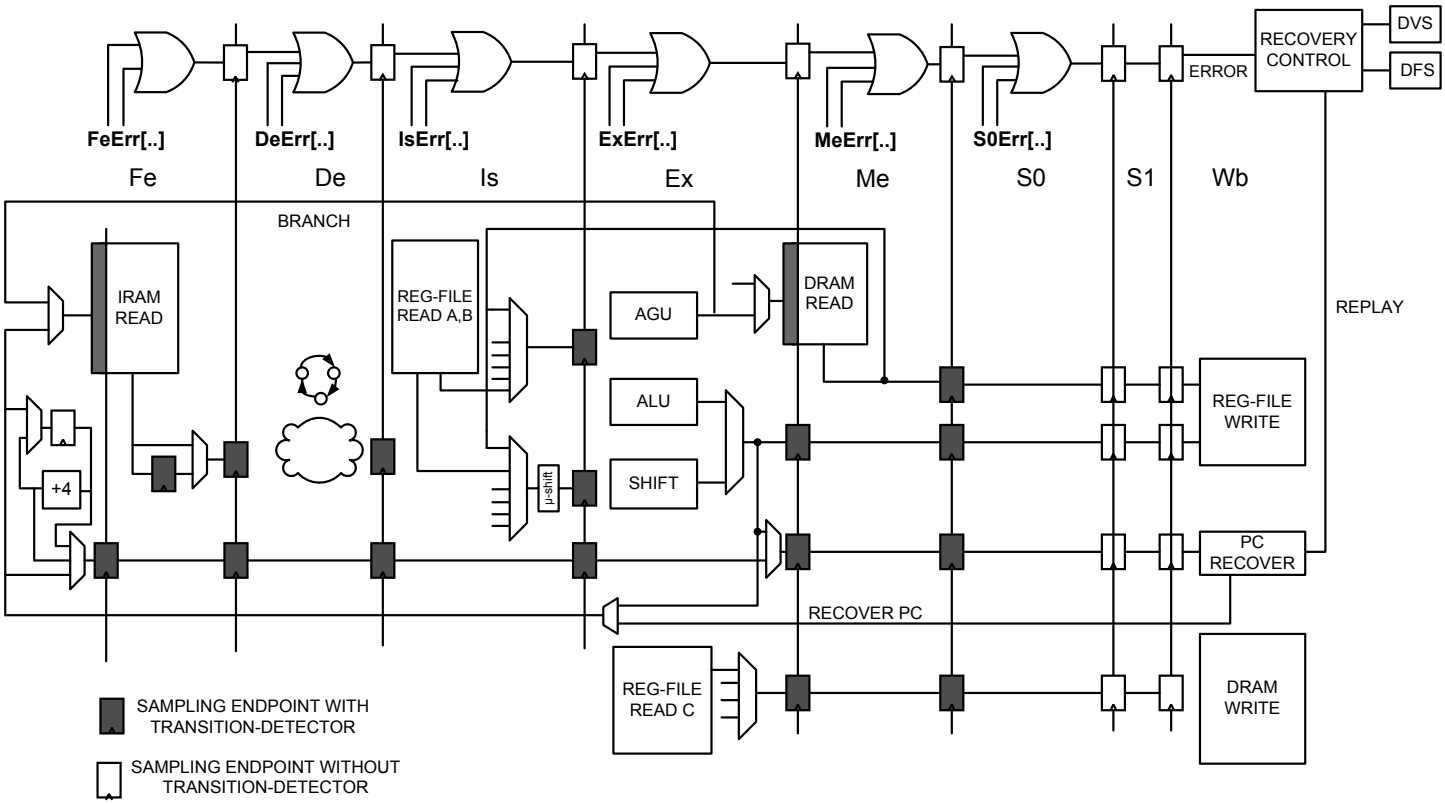


Figure 1: Pipeline diagram of the ARM ISA processor showing error-detecting TD and recovery control

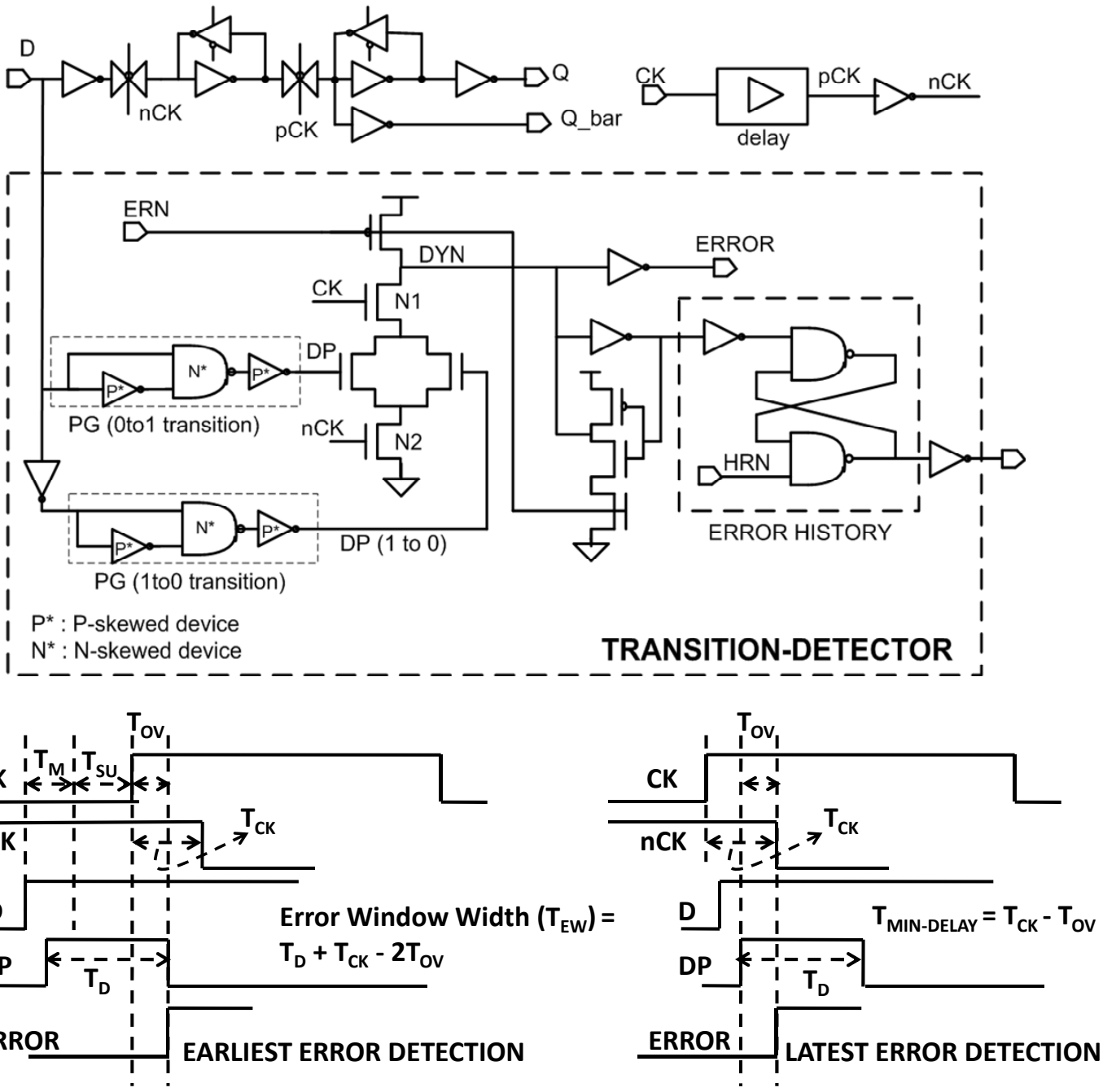
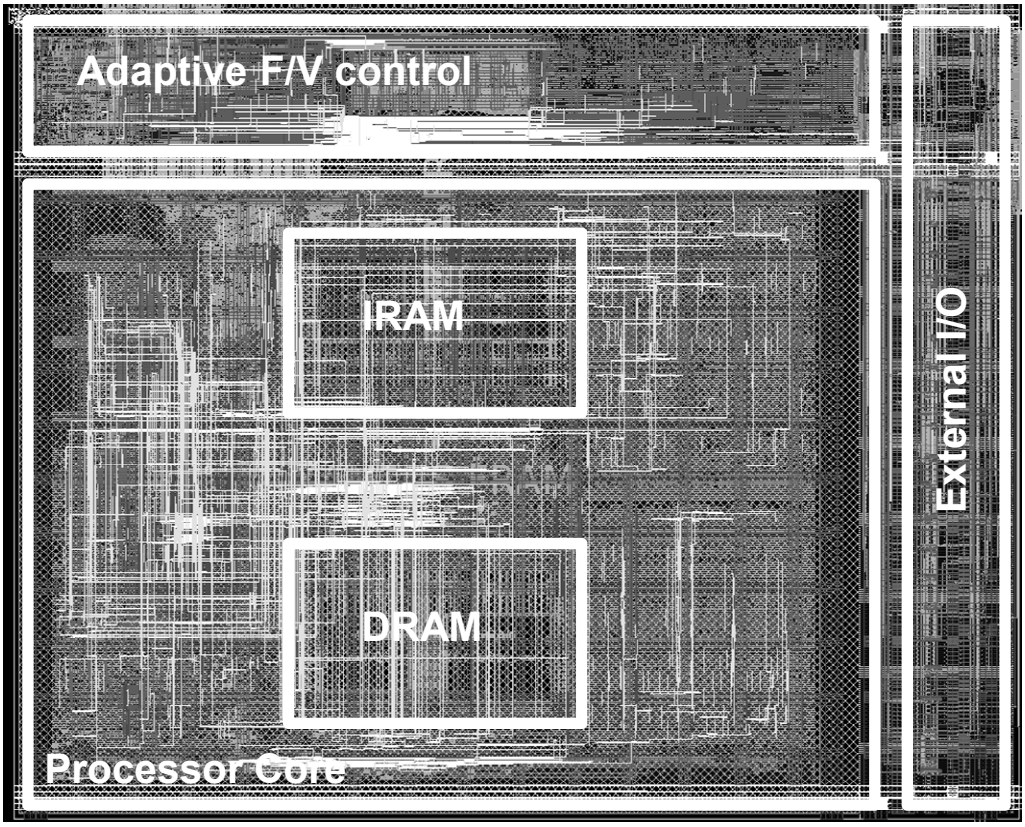
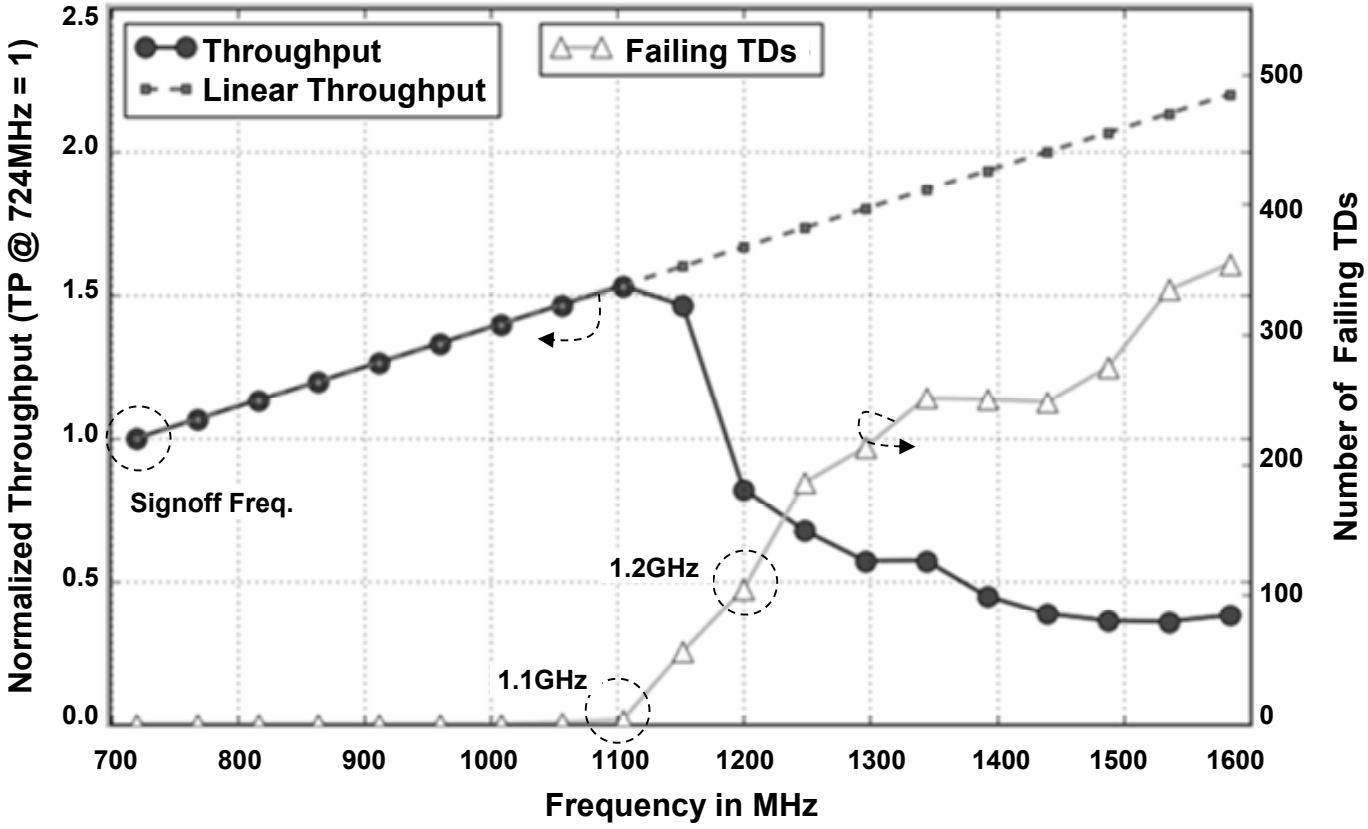


Figure 2: Transition-Detector circuit schematic and conceptual timing diagrams showing principle of operation



Total flip-flops	**2976**
Total flip-flops with TD	**503**
Total ICGs	**149**
Total ICGs with TD	**27**
Total TD for RAMs	**20**
Power Overhead of TD	**5.7%**
Power Overhead of Min-delay buffers	**1.3%**
Process Technology	**UMC 65SP**
Nominal VDD range	**1.0V-1.1V**
IRAM and DRAM size	**2KB**
STA signoff frequency @ 0.9V/SS/125C	**724MHz**
Total die	**63 (20FF, 22TT, 21SS)**

Figure 3: Layout photograph and chip implementation details



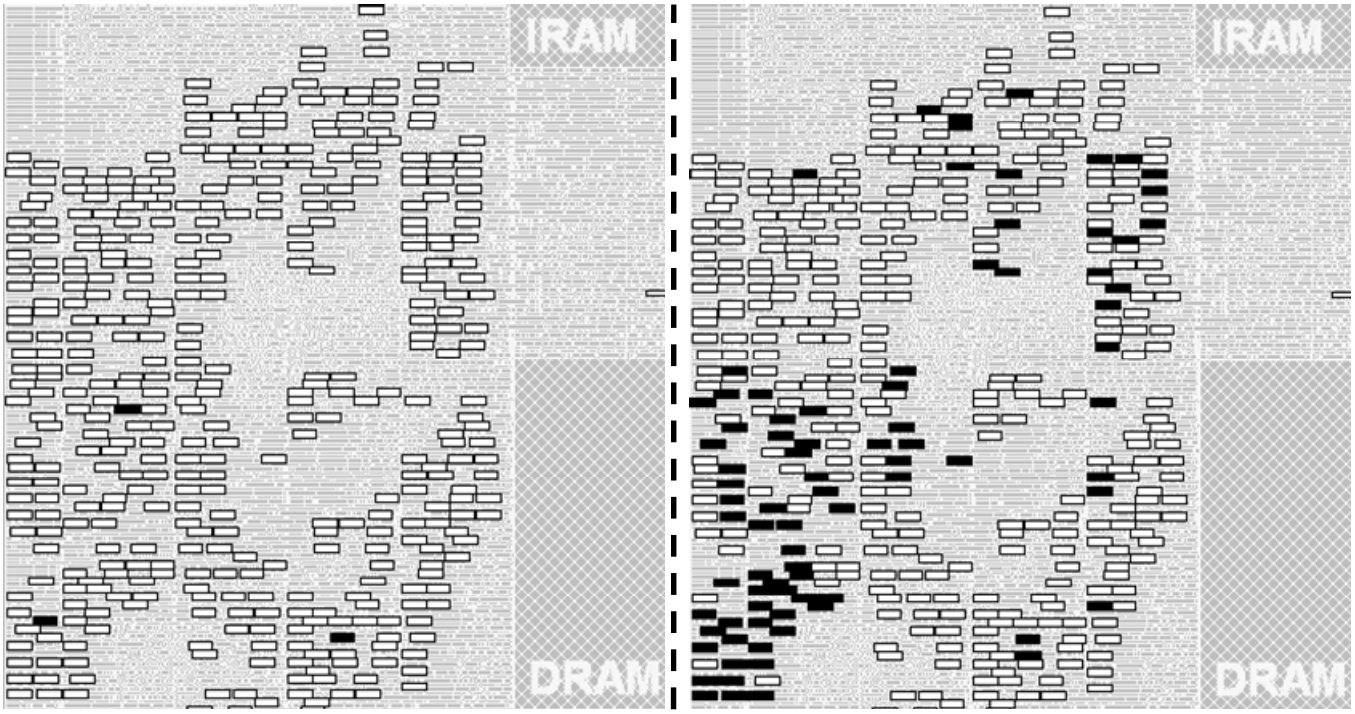


Figure 4: Measured throughput (TP) versus frequency characteristics for a typical workload (WTYP). The PoFF is observed at 1.1GHz where 3 TDs incur errors and maximum TP gain occurs. At 1.2GHz, 122 TDs have timing errors and TP degrades drastically.

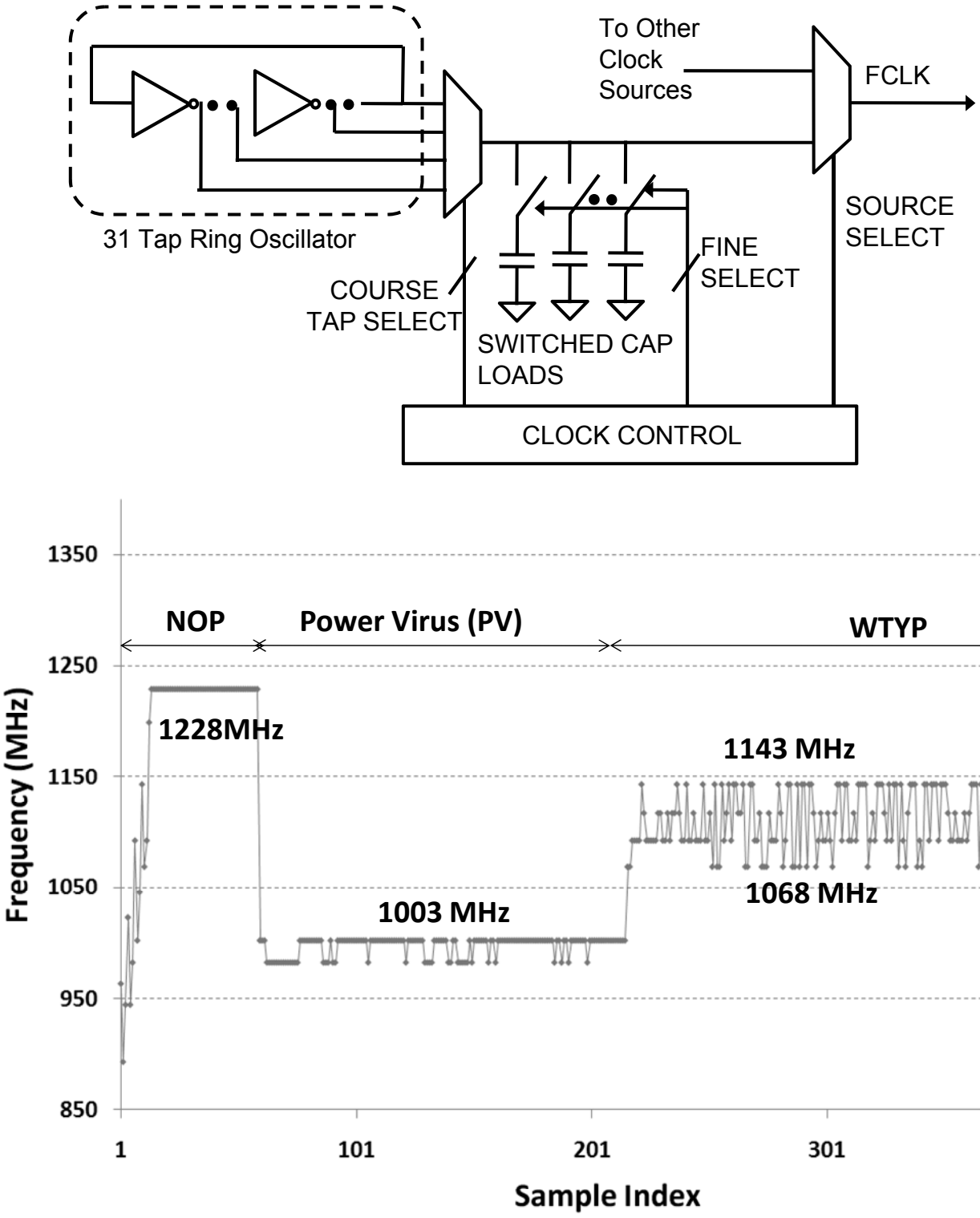


Figure 5: The Adaptive Frequency Controller: Architecture and response. The AFC switches to a 31tap Ring Oscillator (RO) in the adaptive mode. The Clock Control increases frequency by fine-grained 24MHz steps for every 1024 processor cycles without errors. Frequency is reduced by 24MHz for every cycle with error.

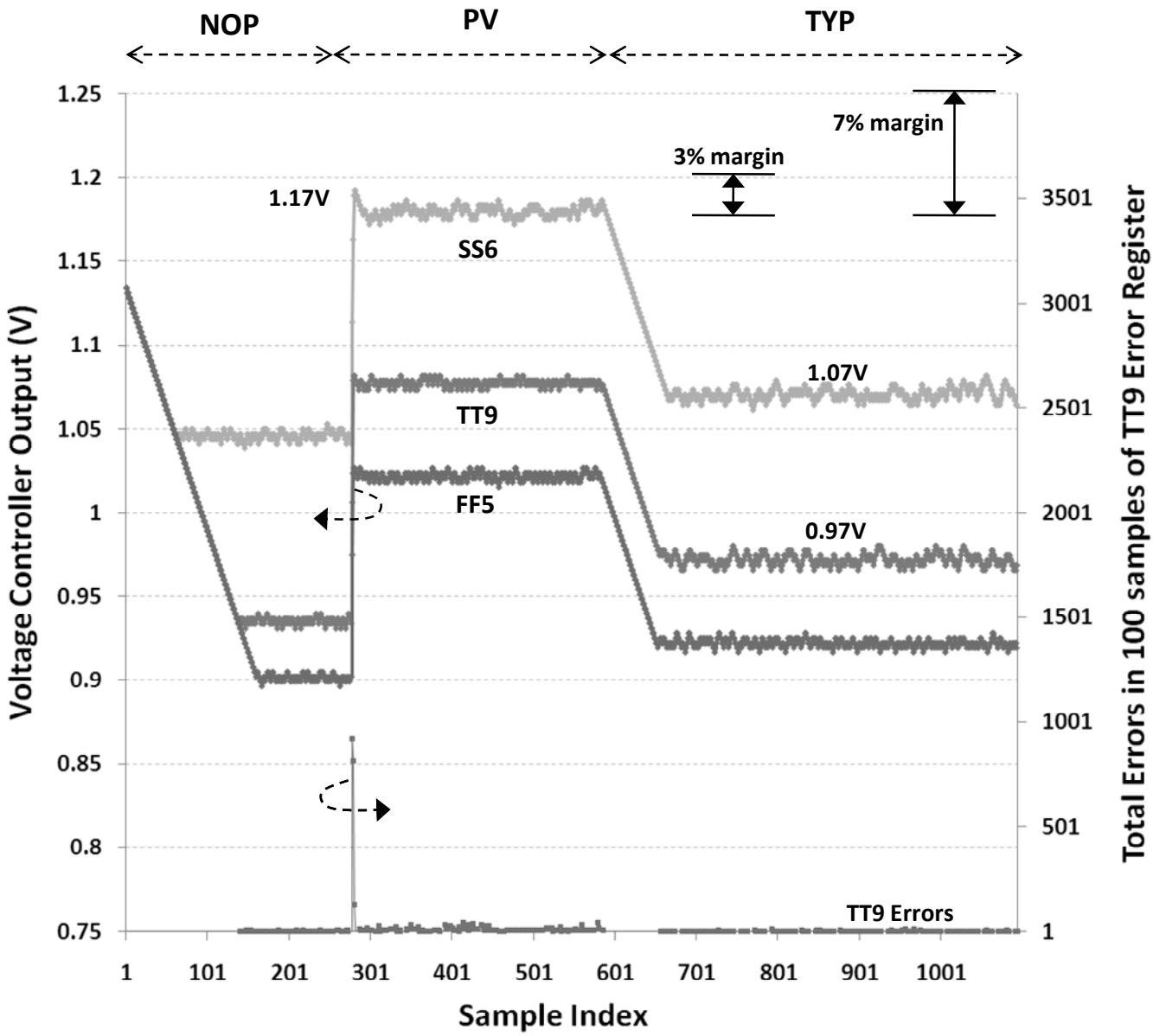
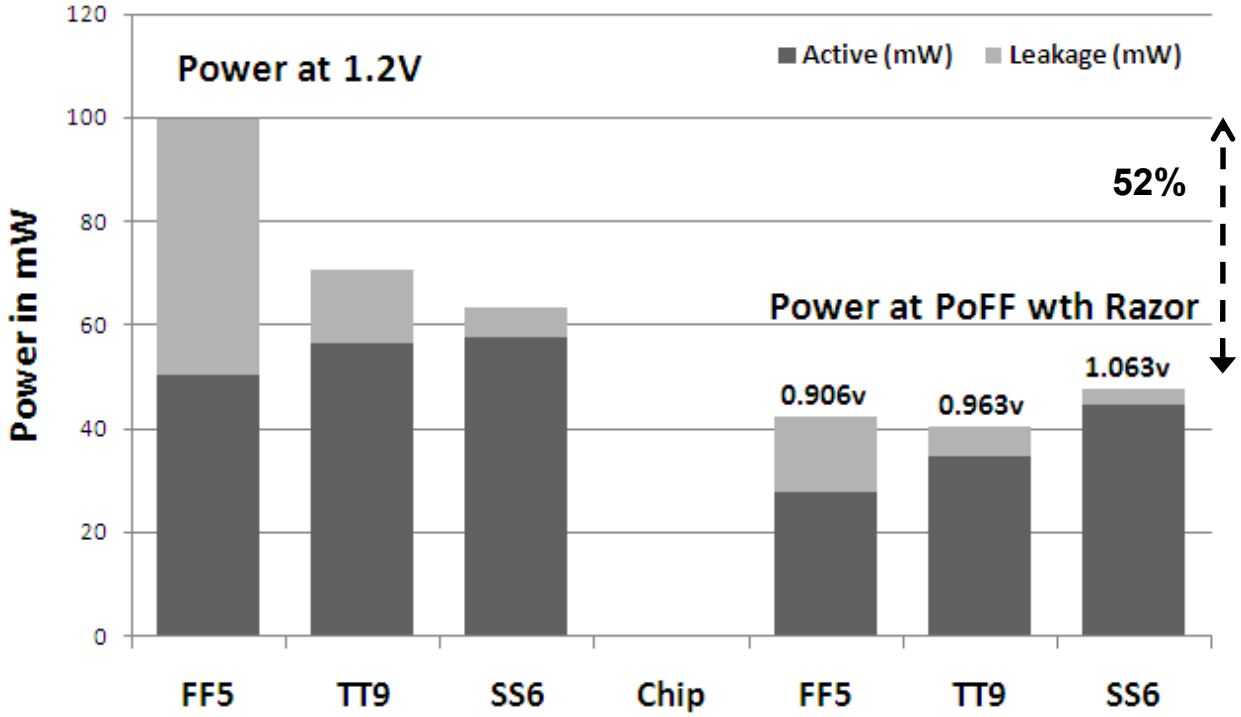
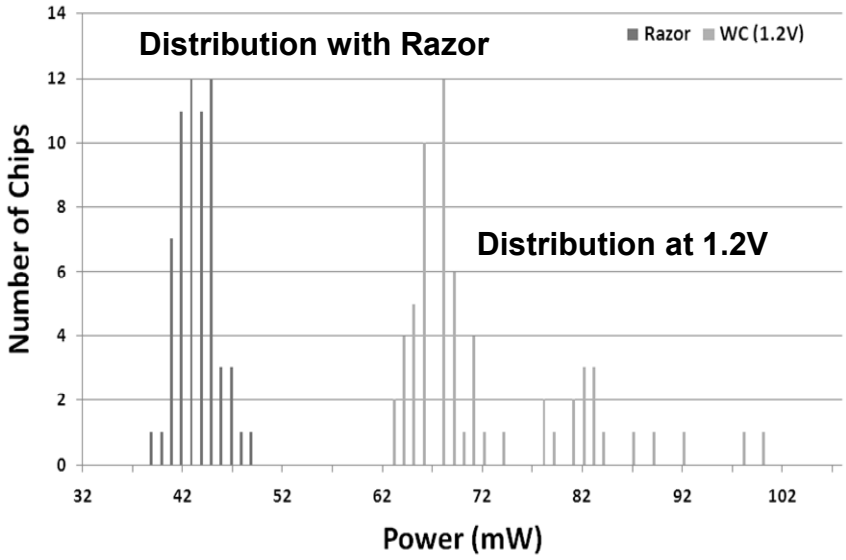


Figure 6: Dynamic Voltage Controller Response. A proportional controller adjusts voltage according to error-rates measured during the execution of the 3-phase code. VDD is increased in large steps in response to the error-rate spike going from the NOP to the PV phase. Additional 3% margin is added for safety to obtain 1.2V as the worst-case voltage.





TT Chip	PV PoFF	1GHz/1.1V
TT5	1.061	Pass
TT7	1.062	Pass
TT19	1.065	Pass
TT17	1.068	Pass
TT8	1.068	Pass
TT9	1.071	Pass
TT31	1.071	Pass
TT47	1.072	Pass
TT34	1.079	Pass
TT3	1.08	Pass
TT18	1.08	Pass
TT32	1.084	Pass
TT16	1.084	Pass
TT10	1.087	Pass
TT33	1.09	Pass
TT45	1.09	Pass
TT30	1.102	Fail
TT15	1.11	Fail
TT26	1.114	Fail
TT2	1.122	Fail
TT27	1.126	Fail
TT28	1.144	Fail

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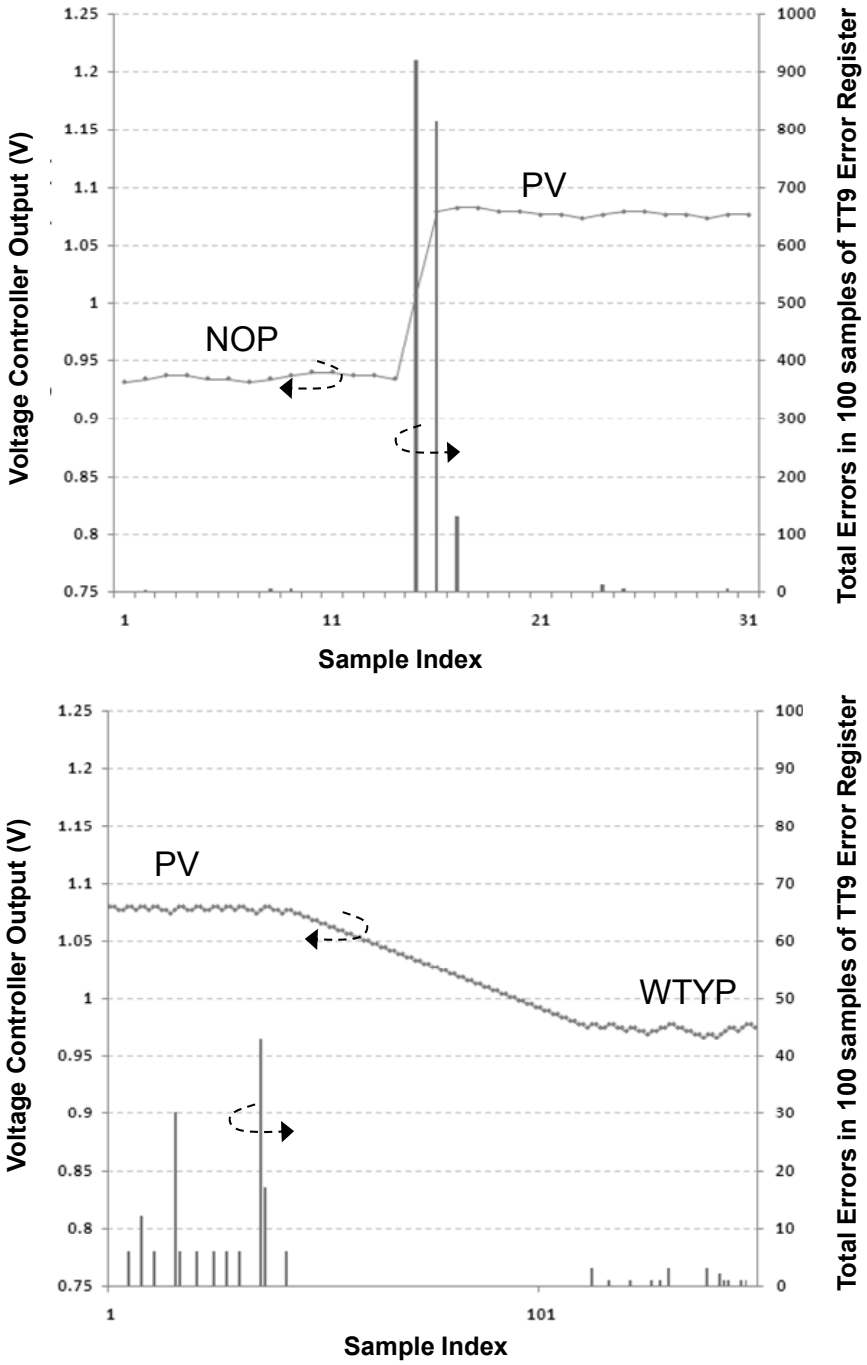

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