Static Electromigration Analysis for On-Chip Signal Interconnects

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***Abstract*—With the increase in current densities, electromigration has become a critical concern in high-performance designs. Typically, electromigration has involved the process of time-domain simulation of drivers and interconnect to obtain average, root mean square (rms), and peak current values for each wire segment. However, this approach cannot be applied to large problem sizes where hundreds of thousands of nets must be analyzed, each consisting of many thousands of RC elements. The authors propose a static electromigration analysis approach. They show that the charge transfer through wire segments of a net can be calculated directly by solving a system of linear equations, derived from the nodal formulation of the circuit, thereby eliminating the need for time domain simulation. Also, they prove that the charge transfer through a wire segment is independent of the shape of the driver current waveform. From the charge transfer through each wire segment, the average current is obtained directly, as well as approximate rms and peak currents. The authors account for the different possible switching scenarios that give rise to unidirectional or bidirectional current by separating the charge transfer from the rising and falling transitions and also propose approaches for modeling multiple simultaneous switching drivers. They implemented the proposed static analysis approach in an industrial electromigration analysis tool that was used on a number of industrial circuits, including a large microprocessor. The results demonstrate the accuracy and efficiency of the approach.**

***Index Terms*—Circuit analysis, circuit simulation, computer-aided design, interconnect reliability, physical design.**

I. Introduction and Previous Work

WIRE WIDTHS have been reduced to deep submicron dimensions in recent years, while their currents have not been scaled proportionally. This has resulted in very high current densities in wires which has made them susceptible to electromigration failures. Electromigration is the process of metal-ion transport due to high current density stress in metal and has been studied extensively [1]–[8]. As the metal-ions migrate, metal buildup or depletion occurs at locations in the wires where there is a divergence in the metal-ion flux. Build up of excessive metal produces so-called hillocks which can result in shorts between wires, while excessive metal depletion can result in changes in the metal wire resistance or even catastrophic disconnections.

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The failure probability of metal wires is typically characterized using test structures that are stressed with dc currents under accelerated electromigration conditions. During normal circuit operation, the signal interconnects in a very large scale integration (VLSI) design are actually stressed with pulsed dc currents, rather that with continuous dc currents. However, it has been shown that, in the absence of Joule heating, the mean time to failure of metal interconnect under pulsed dc currents can be expressed as a function of the average dc current [9]–[11] using Black's equation [2]

$$t_{50} = A \cdot j_{\text{avg}}^{-n} \cdot \exp\left(\frac{Q}{kT}\right) \tag{1}$$

where A and n are empirically determined variables, j_{avg} is the average current density, Q is the activation energy, and kT is the thermal energy. A simple approach to electromigration analysis therefore checks that each individual metal interconnect meets a specified mean time to failure. In this approach, simple design rules are formulated that express the maximum permissible dc current in a metal interconnect as a function of the metal wire width. Although this approach is commonly used in industry, it does not consider the failure probability of the interconnect system as a whole. Therefore, a so-called statistical electromigration budgeting (SEB) [12] approach has also been proposed. In this model, the expected lifetime of the overall system of interconnects is determined from the failure probability of the individual wire segments. In either approach, the electromigration computation requires knowledge of the *average* or *dc* current in each metal interconnect. This current can be obtained by performing a time domain simulation of a transition of an interconnect and integrating the current through the interconnect over the simulation time, as follows:

$$I_{\text{dc}} = \frac{s}{T}\int_0^T i(t)dt \tag{2}$$

where T is the clock cycle period, $i(t)$ is the time varying current, and the switching factor s represents the average number of times that a signal net is expected to transition in a clock period.

In addition to dc current stress induced failure, interconnect can also fail due to excessive Joule heating. High currents in a metal interconnect can generate significant heat due to resistive energy dissipation of the wire. The resulting thermal gradients can induce metal-ion flux divergence which in turn can result in electron-migration failures. High currents will generate the largest temperature gradients, and hence Joule heating was

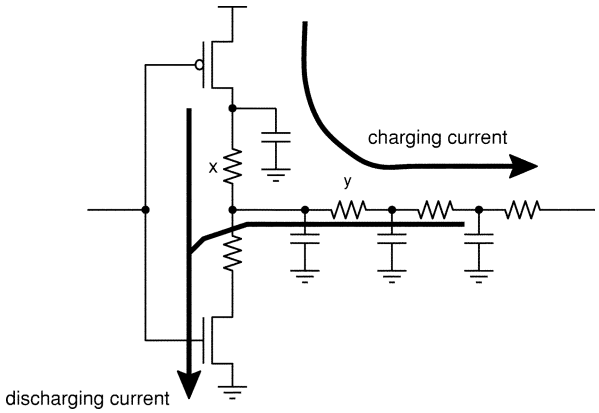

Fig. 1. Unidirectional and bidirectional current flow for electromigation analysis.

found to be a function of the root mean square (rms) and peak currents in a wire segment. Typically, metal failure due to Joule heating is checked using simple rms and peak current limits. The rms current, needed for Joule heating checks, is computed as follows:

$$I_{\rm rms} = \sqrt{\frac{s}{T}\int_0^T i^2(t)dt}. \tag{3}$$

The peak current is simply the maximum current at any point in time during the signal transition. Note that the peak current $I_{\rm peak}$ is always greater than or equal to the rms current $I_{\rm rms}$, which in turn is always greater than or equal to the average or dc current $I_{\rm dc}$.

A current is said to be *unidirectional* if it flows in the same direction through a metal segment during both the rising and falling transition of the signal. In Fig. 1, unidirectional current through segment x for a rising and falling transition is shown. In this case, the $I_{\rm dc}$ current value is nonzero and the likely failure mechanism will be due to dc current stress. On the other hand, if the current flows in one direction during the rising transition and in the other direction during the falling transition, the current is said to be *bidirectional*, as for example the current through segment y in Fig. 1. For this wire segment, $I_{\rm dc}$ is close to zero and the likely failure mechanism is due to Joule heating. In this case, the $I_{\rm rms}$ and $I_{\rm peak}$ currents will determined the lifetime of the segment. Of course, a wire segment may have both significant $I_{\rm dc}$ and $I_{\rm rms}/I_{\rm peak}$ under different driver configurations. Electromigration analysis, therefore, requires the calculation of all three currents, $I_{\rm dc}$, $I_{\rm rms}$, and $I_{\rm peak}$, after which the reliability analysis can be applied using either simple current limit checks or the statistical electromigration budgeting approach. In general, the current limits for $I_{\rm rms}$ and $I_{\rm peak}$ are much higher than for $I_{\rm dc}$ and, therefore, failure due to Joule heating is much less common in a design. Hence, the accuracy required of the $I_{\rm rms}$ and $I_{\rm peak}$ current calculation is lower than that for $I_{\rm dc}$, as long as the error in the computed $I_{\rm rms}$ and $I_{\rm peak}$ currents is conservative.

A dynamic approach to circuit-level electromigration analysis uses simulation of the interconnect with a Spice-level simulation tool to obtain time-varying current waveforms for each interconnect segment. Based on these current waveforms,

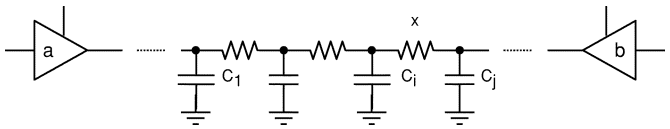

Fig. 2. Worst case driver switching scenarios for a bus line.

average, rms, and peak current values can be easily calculated. These tools incorporate detailed electromigration models and compute the electromigration degradation level of the design. The SPIDER [16] and BERT [17] tools are based on Spice-level simulation. The iTEM tool [15] is based on a fast transistor level simulator using piecewise quadratic transistor models and also accounts for Joule heating. The tool presented in [18] is based on an approximate timing simulator. These approaches, however, are limited in that they only apply to small circuit structures. A chip-level signal net can easily consist of tens of thousands of R/C elements and the number of nets that need to be analyzed can easily reach hundreds of thousands for a large microprocessors. Therefore, Spice-level simulation for all chip-level nets is not feasible. A number of methods for filtering out nets from the analysis using a conservative criteria have been proposed. In [14], a filtering methodology using the so-called "critical threshold" due to stress induced backflow is presented using average currents computations, and in [13] an approach based on lumped capacitance approximations is proposed. However, even after filtering small nets with a conservative filtering criteria, the remaining critical nets will be to numerous to allow Spice-level simulation for analysis of an entire processor. Note also that reduced-order modeling techniques cannot be used for electromigration analysis, since the currents for each element in the net list must be obtained individually.

The analysis is further complicated by the fact that each signal net often has multiple drivers that can switch in different ways. For example, a bus line with two tristate drivers is shown in Fig. 2, driver a being stronger than driver b. Let us consider the current through wire segment x. In order to obtain the maximum average current value for x, the net is driven high with a tristate driver a, while driver b is in tristate mode and then the net is driven low with driver b, while driver a is in tristate mode. During the rising transition, capacitor C_j is charged through x, while in the falling transition, capacitors C_1 through C_i are discharged through x. The same charge transfer would be obtained if drivers a and b were interchanged.

On the other hand, the worst rms current may occur when the net is switched both high and low with either driver a or with driver b. Since driver a is the stronger driver, it will result in a faster transition which increases the $I_{\rm rms}/I_{\rm peak}$ current in x. However, switching the net from driver a charges and discharges capacitor C_j through x, while switching the net from driver b charges and discharges capacitors C_1 through C_i. Depending on the relative size of the drivers and capacitors, it is likely that if x is positioned near the end of the line (near driver b), driver b will result in the maximum $I_{\rm rms}/I_{\rm peak}$ current, while driver a may result in the worst $I_{\rm rms}/I_{\rm peak}$ current if x is positioned closer to the start of the line (near driver a). Therefore, the worst case driver transition depends in a nontrivial way on

the driver strengths and the interconnect topology. In order to determine the worst case driver transition, a dynamic simulation-based approach must simulate all possible rising and falling driver transition combinations (called *switching scenarios*) for an interconnect and therefore incurs a high run time cost. It also requires the user to perform the laborious and error-prone task of writing simulation vectors.

In this paper, we propose a new static approach for electromigration analysis for large circuits. We compute the average, rms, and peak currents for each metal interconnect statically, without requiring the specification of simulation vectors. First, we prove that the charge transfer through interconnect elements can be expressed as a set of linear equations derived directly from the nodal formulation of circuit. Hence, we can compute the exact charge transfer through all interconnect elements by solving a single system of linear equations, avoiding time-consuming time-domain simulation which has typically been used [13]. We also prove the important property that for a linear circuit, the charge transfer through an element is dependent only on the total charge conducted from the driver circuit(s) and is independent of the shape of the driver current. From the charge transfer through a wire segment, we directly obtain the exact $I_{\rm dc}$ current value. We also propose methods for finding approximate $I_{\rm rms}$ and $I_{\rm peak}$ currents based on the charge transfer of the signal net and show how the proposed method can be used in the presence of multiple simultaneous acting drivers.

Finally, we show how different switching scenarios are efficiently evaluated by separating the charge transfer for the rising and falling transitions of the net. This allows the computation of the worst case current values among all switching scenarios in a time linear with the number of independently controllable drivers. The proposed algorithms were implemented in an industrial electromigration analysis tool. We demonstrate the accuracy of the proposed approach by comparing the analysis results with Spice simulations. We also show the efficiency of the analysis for a number of large blocks, including a large processor core. Although in this paper we illustrate the use of our approach on signal nets, the proposed analysis method can also be applied to power supply networks in the same manner.

The remainder of this paper is organized as follows. Section II presents the new linear system formulation for directly calculating charge transfer. Section III presents the approach for finding the worst current values among all switching scenarios. Section IV presents our results and in Section V we draw our conclusions.

II. Calculation of the Charge Transfer

We consider a general interconnect circuit with nodes $N = \{n_1, \ldots n_m\}$, resistors r_{ij}, and capacitors c_{ij} connected between nodes n_i and n_j and one or more driving gates and load gates. Each resistor in the network represents a metal segment or a via between metal layers. Each capacitor represents a load or self-loading of the interconnect, including possible self-coupling capacitors or capacitors in series. The resistors and capacitors are extracted using an extraction tool. A simple example circuit is shown in Fig. 3(a). Our goal is to find the net amount of charge that is transferred through each metal segment or resistor in the interconnect during either a rising or falling transition of the net, which we refer to as the *charge transfer* q_{ij}. It is clear that the charge transfer is simply the integral of the current $i_{ij}(t)$ through an element over time as defined below.

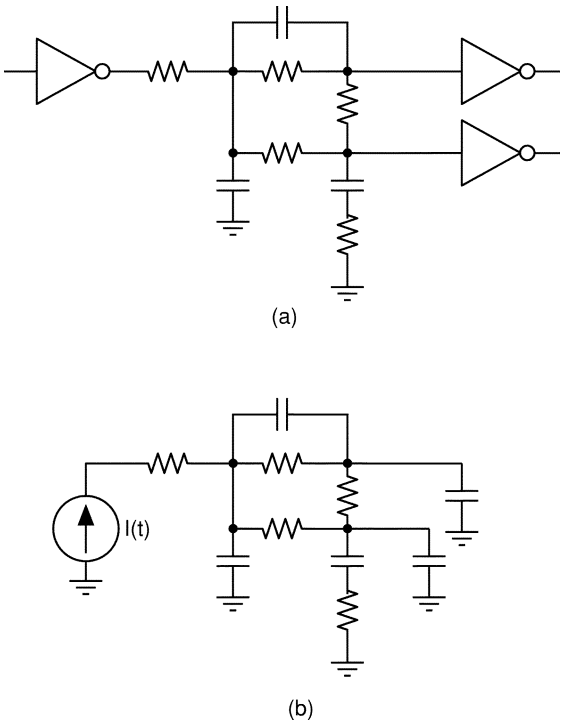

Fig. 3. A circuit and its linear model for electromigration analysis.

Definition 1: The charge transfer q_{ij} though a resistor r_{ij} connected between nodes i and j is

$$q_{ij} = \int_{t=0}^{\infty} i_{ij}(t)dt \tag{4}$$

where $i_{ij}(t)$ is the time-varying current through resistor r_{ij}.

To calculate the charge transfer q_{ij} without performing a time domain simulation, we first construct a linearized version of the circuit, as shown in Fig. 3(b), by replacing the load gates with capacitors and the driver gate(s) with time-varying current sources $I(t)$, such that the behavior of the circuit is unchanged. In other words, the current $I(t)$ is exactly equal to the current produced by the driver gate at each point in time and therefore mimics the driver perfectly without changing the behavior of the circuit. Note that although the example in Fig. 3(b) has only one driver, in general a circuit may have multiple simultaneous switching drivers. After linearizing the circuit, we can represent it with the following standard nodal differential equation:

$$GV(t) + C\dot{V}(t) = I(t) \tag{5}$$

where G is the conductance matrix, C is the capacitance matrix, $V(t)$ are the node voltages and $I(t)$ are the current sources corresponding to the driving gates. We now define the following two useful voltages.

Definition 2: Voltage v_i^0 is the voltage at node i at the start of the transition and v_i^∞ is the steady-state voltage at node i after the transition is completed

$$v_i^\infty = \lim_{t\to\infty} v_i(t) \tag{6}$$

$$v_i^0 = v_i(0). \tag{7}$$

We now observe that for all signal interconnects that are of interest to us, there is no dc path from the signal net to the power supply or ground. This means that at the end of the transition, when the driver gate has reached its steady-state voltage, there is no current through any of the resistors in the circuit. We therefore restrict ourselves to circuits that meet the following condition.

Condition 1: If in the circuit two nodes i and j exist, such that $v_i^\infty \neq v_j^\infty$, then the conductance $g_{ij} = 0$.

Interconnect circuits satisfy condition 1, since there is no current from the driver gate at the end of the transition when the circuit reaches a stable state. This means that the charge transfer from a driver gate d to the interconnect is finite and is calculated as follows:

$$Q_d = \int_{t=0}^{\infty} I_d(t)dt \tag{8}$$

where Q_d is the *driver charge transfer* and $I_d(t)$ is the driver gate current as a function of time. In the section that follows, we show how to compute the charge transfer through a wire based on the driver charge transfer Q_d. Then in the subsequent section, we discuss methods to compute the driver charge transfer.

A. Wire Charge Transfer Computation Formulation

In the following theorem and proof, we show that the charge transfer q_{ij} through a wire segment can be computed by solving a single system of linear equations formulated using the driver charge transfer Q_d, without knowledge of the time varying behavior of the driver currents $I_d(t)$.

Theorem 1: Given a linear circuit that satisfies Condition 1 and the following linear system of equations:

$$G\hat{W} = Q - C\left(V^\infty - V^0\right) \tag{9}$$

where Q is the vector of driver charge transfer (8), G is the conductance matrix, C is the capacitance matrix, and V^0 and V^∞ are the vectors of initial and final node voltages (6) and (7), then, the charge transfer q_{ij} through element r_{ij} is defined as follows:

$$q_{ij} = g_{ij}\left(\hat{w}_j - \hat{w}_i\right). \tag{10}$$

This theorem, therefore, states that if we solve the linear system (9) for $\hat{W}$, we can directly calculate the charge transfer through an element r_{ij} as the difference of the $\hat{w}$ at the two nodes of n_i and n_j multiplied by the conductance of r_{ij}. As shall be come clear, $\hat{w}_i$ can be thought of as the area under the voltage curve of node n_i relative to its final voltage v_i^∞ and $\hat{W}$ is the vector of such voltage areas for all nodes.

Proof: We define $w_i(t)$ as the difference between the voltage value $v_i(t)$ at node i and its stable value at the end of the transition v_i^∞

$$w_i(t) = v_i(t) - v_i^\infty. \tag{11}$$

We then substitute the voltage vector $V(t)$ in the first term of the system of nodal (5) with $W(t) + V^\infty$ and obtain the following linear system of equations:

$$GW(t) + GV^\infty + C\dot{V}(t) = I(t). \tag{12}$$

Since G is a conductance matrix, for every row i the matrix/vector multiplication GV^∞ can be expressed as $\sum_i \left(g_{ij}v_j^\infty - g_{ij}v_i^\infty\right)$. From Condition 1 it follows that all terms in this summation are zero, since either $g_{ij} = 0$ or $v_j^\infty - v_i^\infty = 0$ and therefore $GV^\infty = 0$. After simplifying (12) accordingly and then integrating over time, we obtain

$$\int_{t=0}^{\infty} GW(t)dt + \int_{t=0}^{\infty} C\dot{V}(t)dt = \int_{t=0}^{\infty} I(t)dt \tag{13}$$

and examine each term in turn.

1) For the first term, $\int_{t=0}^{\infty} GW(t)dt$, we define a new variable $\hat{w}_i = \int_{t=0}^{\infty} w_i(t)dt$. Since the node voltages w_i are exponential decaying functions of time, the integral $\hat{w}_i$ is finite and therefore the first term becomes

$$\int_{t=0}^{\infty} GW(t)dt = G\hat{W}. \tag{14}$$

2) For the second term, we get the following:

$$\int_{t=0}^{\infty} C\dot{V}(t)dt = C\left(V^\infty - V^0\right). \tag{15}$$

3) Finally, for the third term, we get

$$\int_{t=0}^{\infty} I(t)dt = Q \tag{16}$$

which is the same as (8).

From (14)–(16) we obtain: $G\hat{W} = Q - C(V^\infty - V^0)$, where we solve for $\hat{W}$.

At the same time, from (4) and (11) we obtain

$$\begin{aligned} q_{ij} &= \int_{t=0}^{\infty} i_{ij}(t)dt = \int_{t=0}^{\infty} g_{ij}\left(v_j - v_i\right)dt \\ &= \int_{t=0}^{\infty} \left(g_{ij}\left(w_j - w_i\right) + g_{ij}\left(v_j^\infty - v_i^\infty\right)\right)dt. \end{aligned} \tag{17}$$

From Condition 1 it again follows that $g_{ij}(v_j^\infty - v_i^\infty) = 0$ and therefore we obtain $q_{ij} = g_{ij}(\hat{w}_j - \hat{w}_i)$ which proves the theorem. □

Note that Theorem 1 is completely general and holds for any number of current sources and all types of capacitors, including coupling capacitors and capacitor dividers, provided Condition 1 holds. To help understand the linear system (9) we can represent it as an "equivalent circuit" shown in Fig. 4, where the driver current source and the capacitors are replaced with "charge sources." The node voltages are replaced with $\hat{w}$, which can be thought of as the area under the voltage curve relative to the final voltage of the node v^∞ and the branch currents are replaced with "charge transfer" q_{ij}.

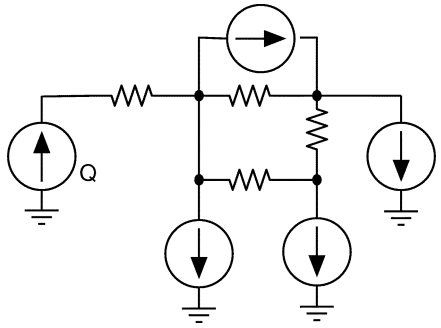

Fig. 4. Circuit representation of charge transfer computation.

As formulated, the linear system (9) will be singular in that the values $\hat{w}_i$ can have an arbitrary offset for each set of nodes belonging to a dc-connected component (DCCC). This can be understood from the equivalent circuit shown in Fig. 4. Each DCCC is only connected to "charge" sources, such that the sum of the total charge injected into and out of the DCCC is zero. Therefore, the values $\hat{w}_i$ of the nodes of the DCCC can have an arbitrary offset, which leads to a signularity of the matrix. This problem can be easily remedied by setting one of the nodes in each DCCC in the system as a reference. Since q_{ij} in (10) depends only on the difference of $\hat{w}$ between two nodes, the reference node in a DCCC and its value do not affect the value of q_{ij} and can be arbitrarily chosen.

From (9) and (10) we can observe that q_{ij} is independent of the shape of the current waveform $I_d(t)$ and is only dependent on its total charge Q_d. We therefore have the following important corollary.

Corollary 1: For a linear circuit satisfying Condition 1 and having one or more current sources $I_d(t)$, all current source waveforms $I_{dj}(t)$ with total driver charge transfer Q_d will result in the same charge transfer for each element in the circuit.

B. Wire Charge Transfer Computation Method

Based on Theorem 1, we propose the procedure shown below in Procedure 1 for calculating the charge transfer through all wire segments of a signal interconnect. Assume we have one or more driver gates d, switching from an initial voltage v_d^0 (typically, but not necessarily, GND or VDD) to a final voltage v_d^∞.

Procedure 1

1) Compute the voltage v_i^0 at node n_i at the start of the transition by setting the voltage at the output of the drivers d to v_d^0 and performing a dc solution.
2) Compute the voltage v_i^∞ at node n_i at the end of the transition by setting the voltage at the output of the drivers d to v_d^∞ and performing a dc solution.
3) Compute the driver charge transfer Q_i for each simultaneous switching driver, as explained in the next section.
4) Form the linear system **(9)**, set one node in each dccc to zero to avoid singularity, and solve for $\hat{w}$.
5) For each element in the circuit, compute q_{ij} using **(10)**.

The above procedure requires a dc solution in Steps 1) and 2). Due to Condition 1, there is no current through any resistor in Step 2) and the dc solutions become trivial through shorting resistors and removing capacitors. In most cases, the dc solution in Step 1) is similarly trivial. Step 4) requires one linear solution. However, since G is a sparse matrix, $\hat{w}$ can be computed very efficiently, even for very large circuits. Therefore, the overall computation of the charge transfer is extremely efficient, compared to performing a nonlinear simulation of the original circuit [such as shown in Fig. 3(a)], while the accuracy of the analysis is not compromised.

C. Driver Charge Transfer Computation

Step 3) in the above procedure requires that the total charge transfer from each simultaneous switching driver is known. If there is only a single driver, its charge transfer Q can be computed through charge conservation from the charge transfer through each of the capacitors

$$Q = \sum_{i=1}^{m} \sum_{j=i+1}^{m} c_{ij} \left(\left(v_j^\infty - v_i^\infty \right) - \left(v_j^0 - v_i^0 \right) \right). \tag{18}$$

However, if there are multiple drivers that switch at the same time, as is often the case, then this total charge Q is divided between these drivers in some manner: $Q = \sum_d Q_d$. In Fig. 5(a), we show an example of a 2-input NOR gate and the associated linearized circuit, where the n-type transistors are folded in the layout. The n-type transistors connected to input b are off and can be modeled as capacitive loads. When input a switches high, its two NMOS transistors turn on, while its PMOS transistor turns off. We, therefore, model these three transistor connections with current sources and need to determine their charge transfer Q_d as shown in Fig. 5(b).

We propose two approaches for determining the charge transfer distribution between multiple simultaneous switching drivers. The most accurate approach is to perform a nonlinear simulation of the gate, with a pi-model [19] representing the interconnect loading. During the nonlinear simulation, we compute the integral of the current through each driver output to obtain its charge transfer which is then used in Step 4) of Procedure 1. Although this requires a nonlinear simulation of the transistors, this simulation is relatively fast since it involves only a small number of nonlinear devices belonging to the driver gate and a small pi-model representing the entire interconnect.

A faster, more approximate approach that avoids this nonlinear simulation makes the simplifying assumption that the short-circuit current is negligible [meaning $I_3(t) = 0$ in the example in Fig. 5(b)]. We then divide the total charge Q computed through charge conservation (18) between the remaining current sources according to their transistor sizes: $Q_d = Q.W_d/\sum_i W_i$, where W_i is the size of transistors i and W_d is the size of the transistor for which we are computing the charge transfer Q_d. This simple approach, although not exact, was found to yield results with less than 4% error in practice, as shown in Section IV. This is due to the fact that the simultaneous switching drivers are, most often, different fingers of a folded device that have identical structure and inputs.

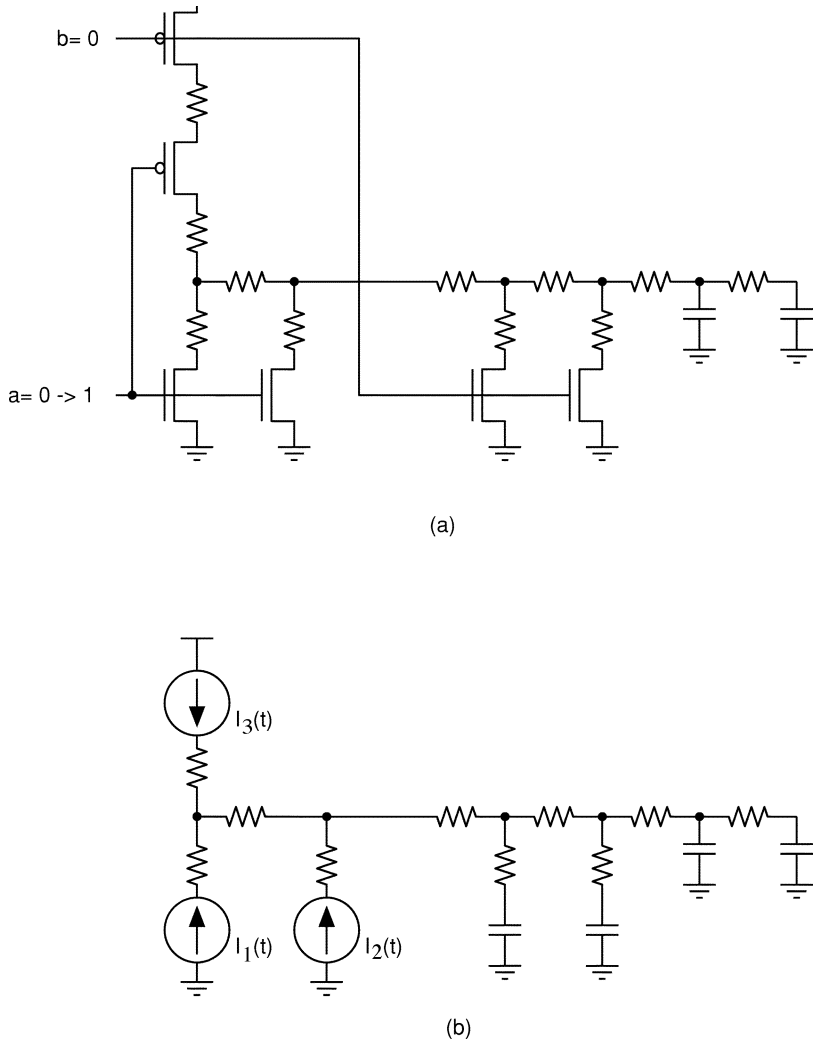

Fig. 5. Interconnect driven by a folded gate and its linear model.

III. Average, RMS, and Peak Current Computation

In the previous section we presented an approach to efficiently compute the charge transfer through a wire segment in response to a rising or falling transition. In this section, we show how to use the charge transfer computation to determine the worst case average, rms, and peak currents for a metal segment. In order to guarantee a repeatable transition pattern, we base our worst case current calculation on the maximum charge transfer during two clock periods where the first period contains a rising or charging transition of the interconnect and the second period contains a falling or discharging transition. Two problems need to be addressed. First, given a particular charging and discharging driver pair we need to compute $I_{\rm dc}$, $I_{\rm rms}$, and $I_{\rm peak}$ from the charge transfers. Second, among all possible charging and discharging driver combinations, we need to determine the worst case pair for each type of current in a metal segment.

In order to efficiently approach this problem, we separately record the charge transfer for rising and falling transitions through an interconnect. The drivers connected to the interconnect are divided into clusters of simultaneously switching drivers, where each cluster is assumed to be independently controllable. Each cluster is simulated in turn for both rising and falling transitions, while recording the minimum and maximum charge transfer in each direction through an interconnect element. The procedure is as follows.

Procedure 2

1) For all wire segments define a reference direction.
2) For (all driver clusters).
3) For (each driver d in a driver cluster) compute *charging* driver charge transfer Q_d.
4) Compute charge transfer through each wire segment using Procedure 1.
5) For (all wire segments i).
6) If (charge transfer is in reference direction) update $\max Q^f_{i,\rm charge}$ and $\min Q^f_{i,\rm charge}$.
7) else update $\max Q^r_{i,\rm charge}$ and $\min Q^r_{i,\rm charge}$.
8) Repeat for discharging transition and update $\max Q^f_{i,\rm discharge}$ and $\min Q^f_{i,\rm discharge}$ or $\max Q^r_{i,\rm discharge}$ and $\min Q^r_{i,\rm discharge}$.

Note that these charge transfers are unsigned quantities and equal to zero if no transfer exists in the specified direction. Also, each charge transfer quantity can be associated with a different driver. Since we simulate each drive only twice (once for the rising transition and once for the falling transition of the net), the

run time complexity is linear with the number of drivers. Based on the maximum and minimum charge transfer in each direction through a wire segment for both rising and falling transitions, we now calculate the average, rms, and peak currents, as follows.

1) Average Current: The average current is defined in (2): $I_{\rm dc} = s/T \int_0^T i(t)dt$, where s is the switching factor and T is the clock period. Typically, the switching factor is obtained from simulations with a cycle based simulator or through propagation of switching probabilities in the circuit. We evaluate $I_{\rm dc}$ over two clock periods, one with a rising and one with a falling transition. If there is nonzero charge transfer in a particular direction for both the rising and the falling transitions, the worst case charge transfer is the sum of both these maximum charge transfers. If there is a zero charge transfer for either rising or falling transition in this direction, the worst case charge transfer is the maximum charge transfer in that direction subtracted with the minimum charge transfer in the opposite direction. We divide the worst case charge transfer by 2 to account for the two transition periods and account for the clock period T as follows.

Procedure 3

1) if $(\max Q^f_{i,\rm charge} > 0$ && $\max Q^f_{i,\rm discharge} > 0) \max Q^f_i = \max Q^f_{i,\rm charge} + \max Q^f_{i,\rm discharge}$
2) else

$$\max Q^f_i = \text{Max}\Big(\Big(\max Q^f_{i,\rm charge} - \min Q^r_{i,\rm discharge}\Big), \Big(\max Q^f_{i,\rm discharge} - \min Q^r_{i,\rm charge}\Big)\Big)$$

3) if $(\max Q^r_{i,\rm charge} > 0$ && $\max Q^r_{i,\rm discharge} > 0) \max Q^r_i = \max Q^r_{i,\rm charge} + \max Q^r_{i,\rm discharge}$.
4) else

$$\max Q^r_i = \text{Max}\Big(\Big(\max Q^r_{i,\rm charge} - \min Q^f_{i,\rm discharge}\Big), \Big(\max Q^r_{i,\rm discharge} - \min Q^f_{i,\rm charge}\Big)\Big).$$

5) $\max Q_i = \text{Max}(\max Q^f_i, \max Q^r_i)$.
6) $I_{i,dc} = s/(2T) \max Q_i$.

2) RMS and Peak Current: The rms current of a wire segment is defined with the integral (3): $I_{\rm rms} = \sqrt{1/T \int_0^T i^2(t)dt}$ and hence requires information about the waveform shape of the time varying current $i(t)$ and not only the total charge transfer. In our approach, we analytically estimate the rms current by approximating the waveform $i(t)$ with a triangular waveform with identical rise and fall times. Fig. 6 shows an example for such current waveform on a resistor for a rising transition where the switching frequency s is equal to one. In this illustration, the charge transfer $\max Q_{\rm charge}$ is defined as the maximum rising/falling charge transfer in either direction: $\max Q_{\rm charge} = \text{Max}(\max Q^f_{\rm charge}, \max Q^r_{\rm charge})$ and $\max Q_{\rm discharge} = \text{Max}(\max Q^f_{\rm discharge}, \max Q^r_{\rm discharge})$. The transition time Tr is the duration of the current pulse for the transition and corresponds to the transition time of the signal. Without a transient simulation of the entire interconnect, we cannot obtain the exact width of the triangular current waveform Tr at each resistor. In our approach, we use the transition time at the output of the driver as an approximation

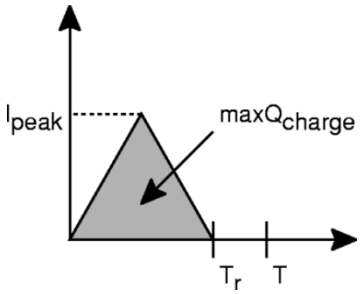

Fig. 6. Triangular current waveform on a resistor.

of the transition time at all the wire segments. Since the transition time at the wire segments will be larger than that at the driver output, our estimation of peak and rms current will err on the side of pessimism. The transition time at the driver output can be obtained from a static timing analyzer or through nonlinear simulation of the driver gate using a pi-load model. It is important to obtain an accurate measure of the transition time since the computed rms and peak currents have square-root and linear dependence on them, respectively. An error in transition time can therefore cause significant error in the computed current densities, especially for the peak current density. Given Tr, we calculate the peak and rms current under the triangular current waveform assumption analytically as follows:

$$I_{\rm peak,charge} = \frac{2 \max Q_{\rm charge}}{T_r}$$

$$I_{\rm rms,charge} = \sqrt{\frac{s}{T} \cdot 2 \int_0^{Tr/2} \left(\frac{4 \max Q_{\rm charge}}{Tr^2}\right) t dt} = \sqrt{\frac{4s\left(\max Q_{\rm charge}\right)^2}{3T_r T}}.$$

For the falling transition, the peak and rms currents $I_{\rm peak,discharge,}$ and $I_{\rm rms,discharge}$ are calculated separately using $\max Q_{\rm discharge}$. The total peak and rms currents are computed as follows:

$$I_{\rm peak} = Max\left[I_{\rm peak,charge}, I_{\rm peak,discharge}\right]$$

$$I_{\rm rms} = \sqrt{\frac{1}{2}\left(I^2_{\rm rms,charge} + I^2_{\rm rms,discharge}\right)}.$$

After the average, rms, and peak currents for all wire segments are computed, the electromigration analysis is performed using either simple current limit checks or using statistical electromigration budgeting [12].

IV. Result

The proposed electromigration analysis approach was implemented in an industrial electromigration checker and was applied on a number of industry circuit designs. Because the analysis requires only one linear solution per interconnect, large chip-level structures could be analyzed efficiently. A commercial extraction tool is used to extract parasitic RC data including the metal width and layer information from the physical layout and the electromigration analysis tool is applied on this data without performing reduction on the RC data.

TABLE I
COMPARISON OF PROPOSED APPROACH WITH SPICE SIMULATION FOR WIRE SEGMENTS OF INDUSTRIAL INTERCONNECTS

Element	Spice (mA)			Proposed Static Approach (mA)		
	I_{dc}	I_{rms}	I_{peak}	I_{dc} (%error)	I_{rms} (%error)	I_{peak} (%error)
R1	0.19	0.50	1.38	0.19 (0.0%)	0.43 (-14.0%)	1.46 (8.7%)
R2	0.06	0.15	0.41	0.06 (0.0%)	0.13 (-13.3%)	0.44 (2.4%)
R3	0.17	0.44	1.23	0.17 (0.0%)	0.39 (-2.3%)	1.32 (7.3%)
R4	0.08	0.20	0.56	0.08 (0.0%)	0.17 (-15.0%)	0.59 (5.6%)
R5	9.15	23.24	68.38	9.34 (2.1%)	21.29 (-8.4%)	72.78 (6.4%)
R6	5.30	13.52	39.80	5.44 (2.6%)	12.38 (-8.4%)	42.34 (6.4%)
R7	1.53	3.89	11.40	1.56 (1.9%)	3.56 (-8.5%)	12.20 (7.0%)
R8	3.94	9.99	19.43	4.01 (1.8%)	9.16 (-8.3%)	31.31 (6.1%)
R9	0.35	0.90	2.58	0.34 (-2.9%)	0.79 (-12.2%)	2.69 (4.3%)
R10	0.05	0.12	0.35	0.05 (0.0%)	0.10 (-16.7%)	0.35 (0.0%)

TABLE II
COMPARISON OF PROPOSED APPROACH WITH SPICE SIMULATION FOR INTERCONNECT WITH VARYING DRIVER SIZE AND LOAD

Driver Size (W/L)	Interconnect Load (fF)	Spice (uA)			Proposed Approach (uA)		
		I_{dc}	I_{rms}	I_{peak}	I_{dc} (%error)	I_{rms} (%error)	I_{peak} (%error)
18	50	31.4	111.2	545	31.0 (-1.3%)	103.3 (-7.1%)	548 (0.6%)
	100	58.4	162.6	605	58.1 (-0.5%)	148.8 (-8.5%)	591 (-2.3%)
	150	84.9	200.8	629	85.1 (0.2%)	182.9 (-8.9%)	603 (-4.1%)
24	50	32.5	123.9	663	32.2 (-0.9%)	116.0 (-6.3%)	675 (1.8%)
	100	59.4	183.4	762	59.2 (-0.3%)	170.0 (-7.3%)	762 (0.0%)
	150	86.3	228.8	805	86.2 (-0.1%)	209.8 (-8.3%)	788 (-2.1%)
36	50	34.9	141.0	820	34.4 (-1.4%)	132.4 (-6.1%)	840 (2.4%)
	100	61.5	212.4	1010	61.3 (-0.3%)	199.4 (-6.1%)	1030 (2.0%)
	150	88.2	268.8	1100	88.1 (-0.1%)	250.7 (-6.7%)	1110 (0.9%)

TABLE III
RUN TIME STATISTICS ON EXAMPLE CIRCUITS

circuit	#nets	Total #RC elem.	Largest net		max # drivers connections	run time (min)
			#R	#C		
Arith	622	73K	347	1,820	38	1.8
Add1	1,923	268K	10,014	29,840	1,088	8.5
Dp1	2,104	319K	10.287	19,624	799	5.0
Add2	4,172	606K	22,294	67,710	2,384	14.8
Dp2	4,598	636K	18,245	46,795	1,509	20.0
uPcore	295K	21.3M	3,766	6,629	511	21.7h

Table I shows the accuracy of our current calculation by comparing it to the result obtained from explicit transient simulations of the interconnect and driver gates using Spice for several large industrial signal net. Our approach estimates average current very accurately, with a maximum error of 2.9%. Since the formulation for charge transfer is exact, the observed deviation is due to error in the modeling of the gate loads with linear capacitors and the distribution of charge transfer between the driver gates. The accuracy of our approach for rms and peak current is also very high with a maximum error of 16.7% and 8.7%, respectively. This error is primarily due to the fact that the actual current waveform is not precisely triangular. However, the observed error is well within the required accuracy for application of the proposed approach in an industrial electromigation analysis tool.

In Table II, we show the results when the proposed method was applied on a circuit with varying driver and load sizes. The circuit consists of a simple inverter driving an interconnect and load capacitance, as shown in Fig. 1. The average, rms, and peak current is reported for the wire segment labeled x. A comparison with explicit transient simulation using Spice is shown for three different driver sizes and load capacitances. The results demonstrate that the analysis has comparable accuracy over a range of driver strengths and load conditions.

Table III shows statistics from our analysis on several circuit designs. It shows that it would be impractical to apply

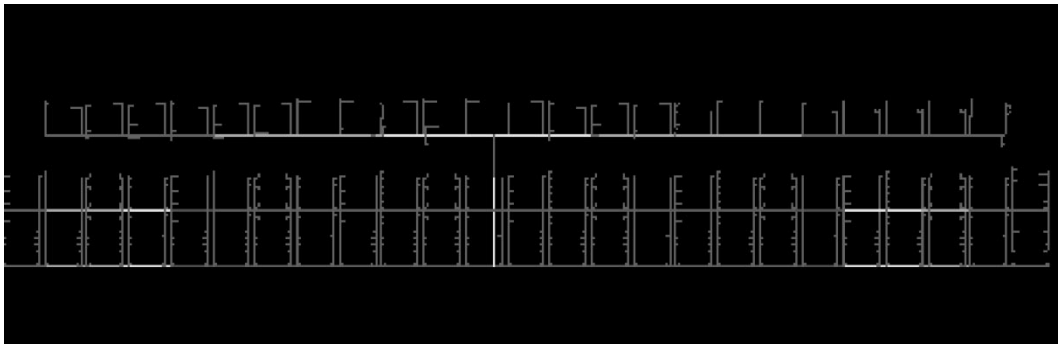

Fig. 7. Current density distribution on a clock net in a dynamic-logic adder (current densities are white for highest to grey for lowest).

brute-force approaches due to the complexity of these designs which results from the number of nets, the number of R/C elements, and the number of possible drivers. On the other hand, our approach successfully analyzed these circuits with very modest run time. Note that in order to demonstrate the efficiency of the proposed approach, a detailed analysis is performed on all the nets in the design and no nets were filtered from the analysis.

Finally, Fig. 7 visualizes a current density distribution for an example which is produced by the electromigration checker for the designer to aid in correcting any violations. The light colors indicate high current densities where the electromigation limits are exceeded.

V. Conclusion

In this paper, we have proposed a static electromigration analysis approach. We showed that the charge transfer through wire segments of a net can be calculated directly by solving a linear system, derived from the nodal formulation of the circuit. We, therefore, avoid the need for time-consuming time-domain simulation. Also, we proved that the charge transfer through a wire segment is independent of the driver current waveform shape and depends only on the total charge transferred from the drivers to the interconnect. We then showed how average, rms, and peak current values for each wire segment can be obtained using the computed charge transfer. We also account for the different possible switching scenarios that give rise to unidirectional or bidirectional current by separating the charge transfer from the rising and falling transitions. We implemented the proposed static analysis approach in an industrial electromigration analysis tool that was used on a number of industrial circuits, including a large processor core. Experimental results were presented to demonstrate the accuracy and efficiency of the approach.

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Aurobindo Dasgupta, photograph and biography not available at the time of publication.