21.5 A 5.58nW 32.768kHz DLL-Assisted XO for Real-Time Clocks in Wireless Sensing Applications

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There is growing interest in ultra-low power wireless microsystems [1]. Synchronization between different nodes in a wireless sensor network plays an important role in the overall node energy budget due to the high power demand of wireless communication. One synchronization approach is to employ a real-time clock (RTC) on each node, with nodes awakening periodically to communicate and re-synchronize. With recent work on ultra-low power microsystems demonstrating average power consumption of several nW [2], there is a need for ultra-low power timers that can synchronize communication events and serve as frequency references for radios.

Ultra-low power silicon-based RTCs can consume sub-nW (e.g., 660pW in [3]), but they suffer from high frequency instability. Crystal oscillators (XOs) provide a more constant frequency but at the expense of higher power consumption, typically in the range of μW to 100s of nW. Previous works on low power XOs focused on minimizing the oscillation amplitude [4-6]. With low oscillation amplitude, energy lost per cycle is reduced such that the circuit has to replenish less energy to maintain the oscillation. However, the voltage amplitude at the input of the driver circuit is also reduced. Therefore the driver circuit strength becomes exponentially weaker as the driver enters the sub-threshold region, making it difficult to maintain stable oscillation. In addition, the circuit consumes a constant bias current, increasing power consumption. The lowest reported power for a 32.768kHz crystal oscillator with this approach is 27nW [5].

To mitigate these problems, we propose the use of an amplifier stage, combined with separate voltage domains for the amplifier and driver stage. It increases the input voltage amplitude to the driver circuit and improves device transconductance. This decouples the XO oscillation amplitude from the driver stage input amplitude and allows lower XO oscillation operation, thereby reducing power loss in the crystal itself. Furthermore, to address the losses in the driver, we use pulse mode charge injection where the driver is only enabled for a short duration when the driver output is near the supply rail. This avoids driver conditions where both high current and high voltage exist across the driver, thereby reducing driver loss significantly. The driver pulse generation is performed using a DLL, which locks to the XO frequency and generates one charge and one discharge pulse per cycle.

The overall block diagram is shown in Fig. 21.5.1. The circuit operates in three different voltage domains internally generated by a switched-capacitor network (SCN). The XO and the output driver (OD) stage operate in the smallest voltage domain, denoted by V_{DD-L} (515mV) and V_{SS-L}(415mV). The voltage across this domain is too small for the other circuits to reliably operate, therefore the front end (FE) and DLL operate in a middle voltage domain, denoted by V_{DD-M} (660mV) and V_{SS-M} (265mV). Input signals to the OD swing full rail, denoted by V_{DD-H} (940mV) and V_{SS-H} (0V), to provide high transconductance.

The FE and DLL schematics are given in Fig. 21.5.2. The FE works similarly to [7]. By dynamically adjusting both NMOS and PMOS body bias, this stage transforms oscillation in the V_{DD-L}/V_{SS-L} domain to the V_{DD-M}/V_{SS-M} domain and is robust to process variation. The body bias adjusting circuit (BAC) consists of three inverter stages with all input and output levels centered between V_{DD-M} and V_{SS-M}. A 60pF stabilizing capacitor limits bias drift when the circuit is off to 10uV/s at 85°C in fast corner simulation. A reference voltage (V_{ref}) is internally generated using a diode-connected transistor stack. Based on simulation, the FE dynamically adjusts switching threshold to the middle of V_{DD-M} and V_{SS-M} at ±3σ process corners and consumes 0.3nW at typical condition in simulation. As for DLL, an odd number of stages are used so that the last stage is 180° out of phase from the first stage to minimize the number of delay cells and power consumption. The BAC and charge pump in DLL is turned off periodically to minimize power consumption. Furthermore, edge detection is performed using simplified FFs rather than standard DFFs. By reducing the number of transistors from 36 to 13, power consumption due to DFFs is reduced by 55%.

The circuit can be configured to pick a pair of outputs from the DLL delay cells to generate pulses of selected length and phase. Two separate pulses are generated for the PMOS and NMOS of the OD. Since this pulse is generated in the V_{DD-M}/V_{SS-M} domain, it is level-converted to V_{DD-H}/V_{SS-H} to maximize OD strength. Two separate level converters (LCs, in Fig. 21.5.3) are used to accommodate the different pulse shapes required for the PMOS/NMOS devices. This allows for level conversion on only one rail; namely, to V_{DD-M}/V_{SS-H} for the PMOS OD, and to V_{DD-H}/V_{SS-M} for the NMOS OD. Due to unequal PMOS and NMOS strength, two different LC designs are used. High V_{th} devices, marked with thick lines, are used to allow robust transitions at 0.85nW for two LCs combined. The LC driving the PMOS operates using a similar principle to [8], employing a delayed feedback signal to minimize contention during transition.

The SCN used to generate intermediate voltage levels is shown in Fig. 21.5.3. All voltage domains generated by the SCN are centered in the middle of the supply rails, and therefore do not share a single ground level. Voltage from V_{DD-M} to V_{SS-M} can be configured to be 1/3, 3/7, 1/2, 3/5 of $V_{DD-H} - V_{SS-H}$ and the voltage from V_{DD-L} to V_{SS-L} can be configured as 1/5 or 1/3 of $V_{DD-M} - V_{SS-M}$ using externally controllable settings in our test chip.

Clock dividers in the V_{DD-M} / V_{SS-M} domain generate signals oscillating at 1/2, 1/4, 1/8, 1/16, and 1/32 of the XO's resonant frequency. The first three signals are used as the operating frequency of the SCN. Also, the divided signals can be logically NAND'd to enable aggressive duty cycling of the DLL charge pump for power savings. Negative-edge triggered DFFs are used together within the clock divider to eliminate glitches at the NAND outputs.

The proposed circuit was fabricated in 0.18μm CMOS technology. Fig. 21.5.4 shows measured results of the DLL-assisted XO (DAXO). For characterization, the chip was initially tested with its internal voltage rails driven from an external voltage sources. The top-left graph shows the case when ($V_{DD-L} - V_{SS-L}$)=150mV. Power consumption in ($V_{DD-M} - V_{SS-M}$) includes FE, DLL, and part of level converters. Rapid increase of power in ($V_{DD-M} - V_{SS-M}$) can be observed as the voltage difference exceeds the threshold voltage of the transistor, coming from increase in static current in FE. On the other hand, the top-right graph shows that lower oscillation amplitude is required for low power consumption, once ($V_{DD-M} - V_{SS-M}$) voltage is under or near threshold. The waveform of the actual circuit is shown on the bottom-left. The waveform shows both terminals of the crystal, along with signals at gate terminals of PMOS and NMOS ODs. The bottom-right graph shows the operating range of different SCN setting. The minimum power of 5.58nW was observed at VDDH=0.94V, room temperature.

Fig. 21.5.5 shows temperature characteristics of DAXO. The crystal itself has a quadratic dependence on temperature. Overlapped with this innate temperature characteristic on the top-left is the result of DAXO and a traditional circuit. The top-right graph shows power consumption at the same temperature range and the bottom graph shows frequency variation of DAXO at room temperature. These graphs show that the DAXO maintains the frequency stability and performance of the crystal while significantly reducing power.

Fig. 21.5.6 shows the performance summary and comparison with previous works. The chip area is 0.3mm^2, including capacitors. The power consumption was reduced by 4.84x compared to the previous best reported circuit. The crystal's frequency performance is maintained through -20°C~80°C.

References:

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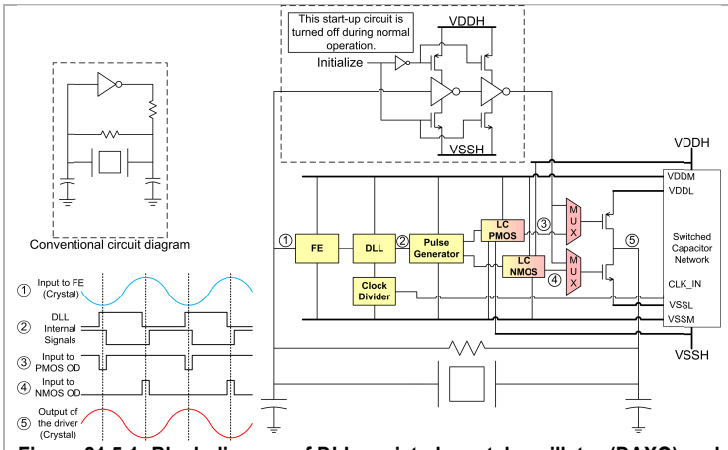

Figure 21.5.1: Block diagram of DLL-assisted crystal oscillator (DAXO) and its concept.

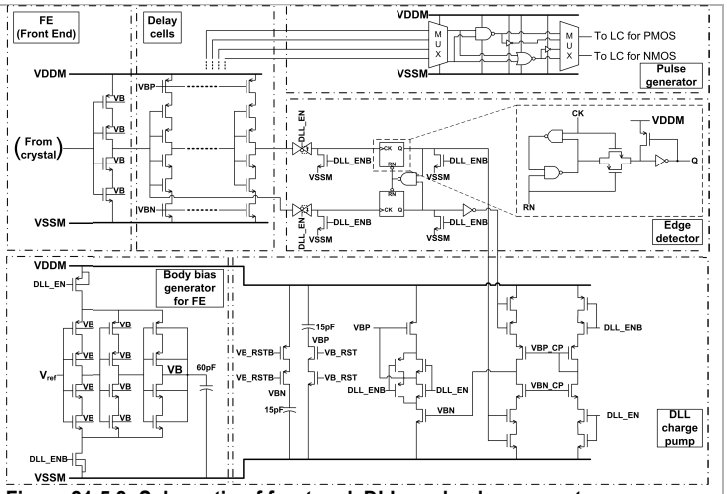

Figure 21.5.2: Schematic of front end, DLL, and pulse generator.

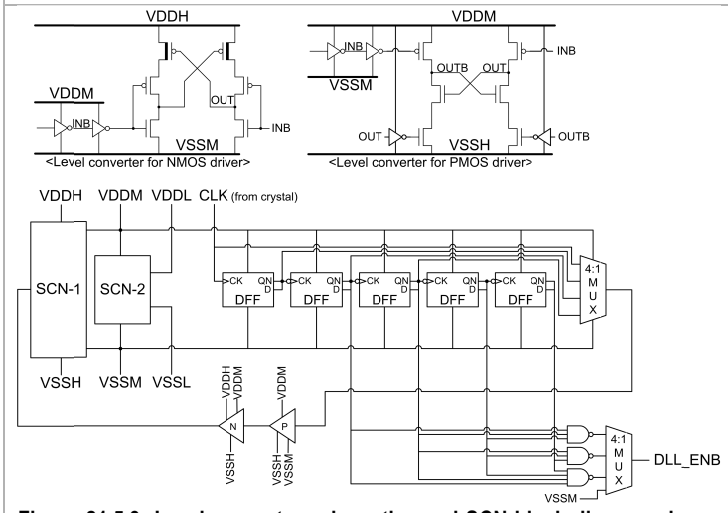

Figure 21.5.3: Level converter schematics and SCN block diagram shown with clock divider.

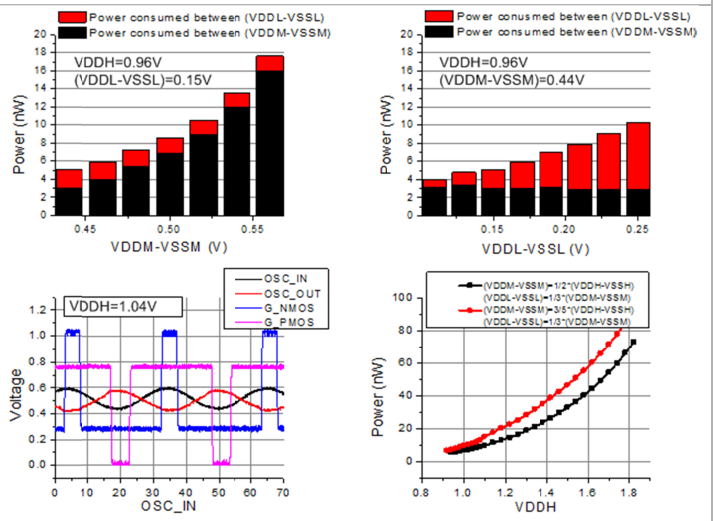

Figure 21.5.4: Measurement results of voltage-overridable DAXO on the top. Operation waveform and power consumption of normal version of DAXO at room temperature are shown on the bottom.

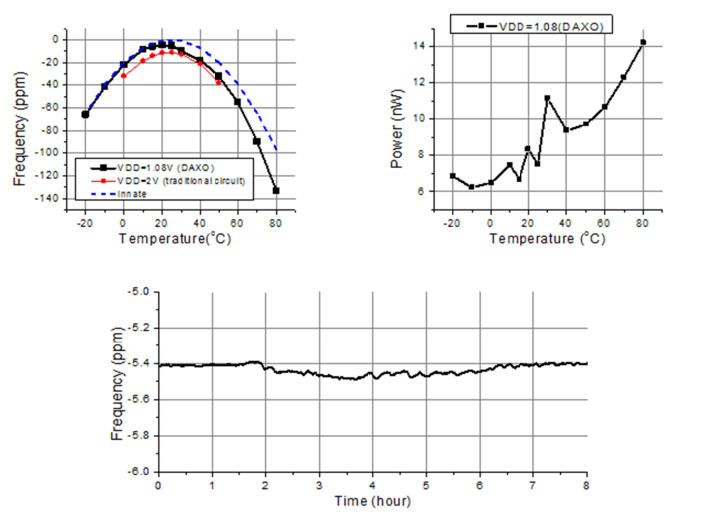

Figure 21.5.5: Temperature characteristics of DAXO at VDDH=1.08V. DAXO maintains frequency stability performance with low power consumption.

Operating frequency	32.768kHz
Area	0.3mm^2
Minimum power consumption	5.58nW
Operating temperature tested	-20°C~80 °C
Frequency drift within testing temperature	-4.56ppm~-133.3ppm (maximum drift from ideal curve: -36.5ppm)
Operating V_{DD-H} range at room temperature	0.92~1.8V
Minimum oscillation amplitude	100mV$_{p-p}$
SCN frequency as tested	4.096kHz (slowest setting available on chip)

	Frequency	Area	Power consumption	Technology
[9]	32.768kHz	N/A	220nW	2μm
[10]	2.1MHz	0.41mm^2	700nW	2μm
[6]	32.768kHz	N/A	27nW (32nW with clock divider)	2μm
This work	32.768kHz	0.3mm^2	5.58nW	0.18μm

Figure 21.5.6: Performance summary of DAXO, including comparison to previous related work on low-power XOs.