

SLC: Split-Control Level Converter for Dense and Stable Wide-Range Voltage Conversion

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Abstract—Ultra-low voltage design makes signal level conversion a critical component in modern low power designs. This paper proposes a static level converter operating in the subthreshold regime, called SLC (Split-control Level Converter). Using a novel circuit structure, SLC effectively eliminates the high leakage and short circuit currents in previous approaches. Designed for 300mV to 2.5V conversion and fabricated in 130nm CMOS, measured results show 2.3×, 9.9×, and 5.9× improvements over conventional DCVS structures in delay, static power, and energy per transition, respectively. Even with the smallest area among wide-range level converters, it also has 5.2× smaller standard deviation in delay and only 5.6% change in FO4 delay with 10% V_{DDL} drop, demonstrating robustness.

I. INTRODUCTION

Level conversion circuits are ubiquitous in modern power-aware systems. The multi-core system in [1] suggests an optimal voltage/frequency mapping among the cores, requiring thousands of level converters (LCs). LCs become more critical as the voltage difference grows, for instance, between aggressively voltage-scaled DSP accelerators [2] and I/O. An extreme case is the wireless sensor node platform in [3], where the core is operated at a subthreshold level while sensors and radio use the battery voltage (3.6V). Due to such significant voltage differences, these applications require wide-range LCs with fast and low power operation. Also, LCs in many sensing applications, such as environmental monitoring, will be exposed to extreme conditions, exacerbating robustness challenges in the LCs. One recent LC

design [4] shows robust operation in wide process/voltage/temperature (PVT) conditions but uses dynamic operation and has a higher design complexity. Further, in systems requiring thousands of LCs, the area in [4], which is comparable to the conventional Differential Cascode Voltage Switch (DCVS) LC, can become limiting.

The conventional DCVS LC in Fig. 1(a), designed for 0.3V to 2.5V conversion in 130nm CMOS, cannot meet these requirements. For correct operation, it is necessary that in all PVT conditions, $I_{NMOS,ON}$ exceed $I_{PMOS,ON}$ to ensure successful discharge of node $n2$ (or $n1$). ZVT (zero- V_{TH}) devices prevent oxide-breakdown in the thin-oxide devices, making it possible to use standard- V_{TH} (SVT) devices with large $I_{NMOS,ON}$ [5], but the exponential dependency of $I_{NMOS,ON}$ on V_{TH} in the subthreshold region ($V_{IN}=V_{DDL}=0.3V$) makes it highly susceptible to variations; its yield is only 64.72% over 100,000 Monte Carlo (MC) simulations at 25°C even with very large pull-down devices of $(W/L)_{M1,M2}=30\mu m/0.12\mu m$. The interrupted DCVS LC in Fig. 1(b) has an additional PMOS M7 (or M8) that is expected to be weakened when $V_{INB}=V_{DDL}$ (or $V_{IN}=V_{DDL}$), thus reducing $I_{PMOS,ON}$. However, this is not effective for $V_{DDL} \ll V_{DDH}$ since $|V_{GS}|$ of M7 (or M8) remains close to V_{DDH} . MC simulations show only marginal improvement over conventional DCVS in this case. Previously proposed LCs either use a sensitive subthreshold analog circuit – i.e., a Reduced Swing Inverter – which has not been fully demonstrated in silicon [6][7], or a high voltage clock ($V_{CLK}=V_{DDH}=2.5V$) that results in high power consumption and a complex synchronization circuit [8],

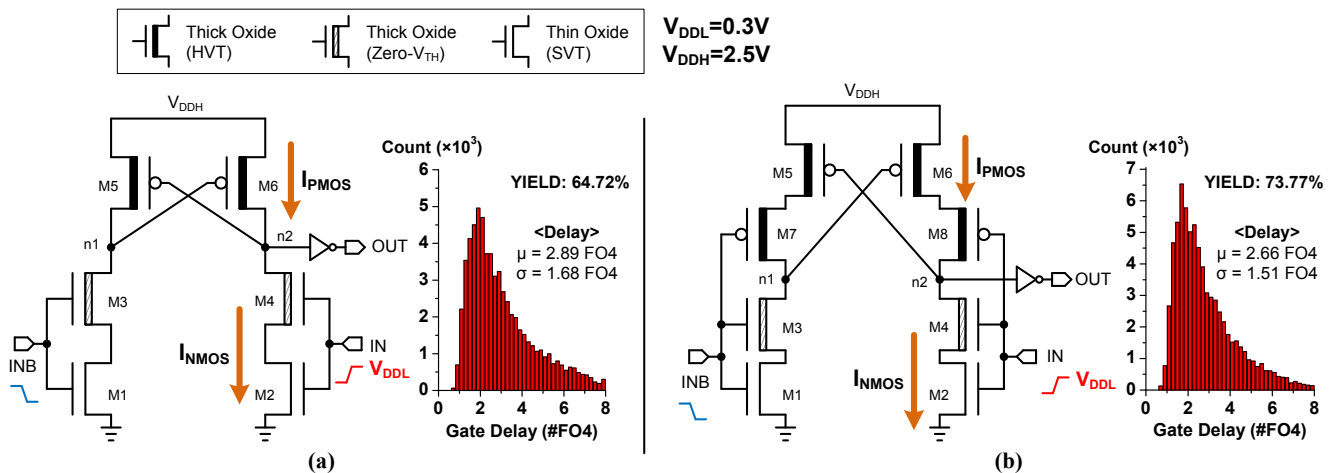


Figure 1. (a) Conventional DCVS LC with Monte Carlo simulation result, (b) Interrupted DCVS LC with Monte Carlo simulation result.

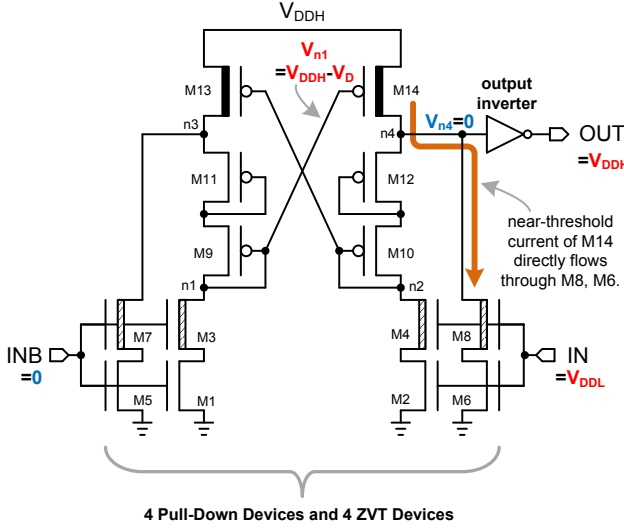


Figure 2. Level converter in [9]; this design always has near-threshold current flowing through one of the SVT transistors.

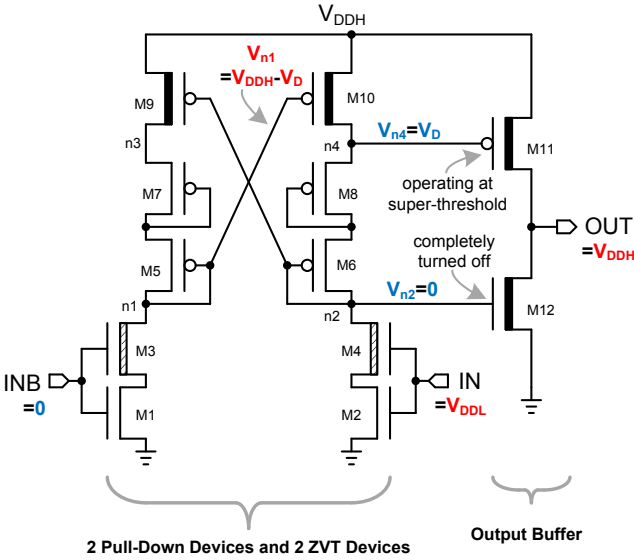


Figure 3. SLC (Split-control Level Converter). In the new output buffer, one output device (M11, M12) is always completely turned off.

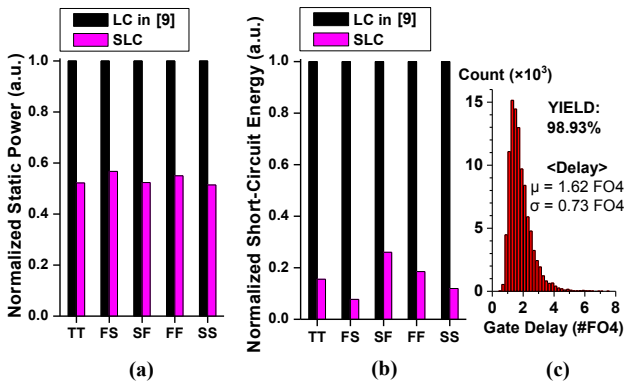


Figure 4. (a),(b) Comparisons between LC of [9] and SLC show that SLC substantially reduces static power and short-circuit energy. (c) 100,000 Monte Carlo simulations of SLC. Average delay and its standard deviation are reduced by 1.8× and 2.3×, respectively, compared to Fig. 1(a).

causing 1016× larger layout size than the conventional DCVS LC.

The LC in [9] is shown in Fig. 2 and includes ZVT devices and additional PMOS diodes to tolerate 0.3V to 2.5V conversion in 130nm CMOS. The diodes (M9-M12) serve as current limiters, effectively reducing $I_{PMOS,ON}$ and hence improving robustness. However, they also prevent nodes $n3$ and $n4$ from fully discharging to ground, hence this design requires additional pull-down devices (M5-M8) that add internal node capacitance. Thus, discharge speed at $n4$ (or $n3$) is slow, causing short-circuit current in the output inverter. Also, $n1$ (or $n2$) is never fully charged to V_{DDH} due to the diode voltage drop (V_D) and causes static near-threshold current as depicted in the figure.

II. SLC (SPLIT-CONTROL LEVEL CONVERTER)

Fig. 3 shows the proposed LC, named SLC (Split-control LC). It includes a new output structure (M11 and M12) to avoid the aforementioned problems. At the beginning of a rising transition at IN, $V_{n1}=0$ and $V_{n2}=V_{DDH}-V_D$, where V_D represents the diode voltage drop through M6/M8 (or M5/M7). Once V_{IN} goes high to V_{DDL} , M2 can easily discharge node $n2$ because of the current-limiting diodes. Node $n4$ is also discharged to V_D , and M11 is strongly on with a large $|V_{GS}|$, quickly charging up the output node while M12 is completely off. The circuit does not require the additional pull-down paths that contain the largest devices in the circuit, which results in at least 1.8× lower static power across process corners as shown in Fig. 4(a). This also results in reduced internal loading at $n4$ and $n3$, speeding transitions at these nodes. In addition, M11 and M12's gate voltages are separately controlled in the output buffer (hence the name Split-control LC). This configuration ensures that the transistor turning off in the M11 – M12 stack always leads the transistor turning on, reducing short circuit current significantly and also improving the charging (or discharging) speed. Overall, Fig. 4(b) shows that the circuit provides a 3.8–12.9× reduction in short-circuit energy consumption across process corners. MC simulations show high yield (98.93%) with much lower delay variability (Fig. 4(c)). Compared to the LC in [9] which has $\mu = 2.02$ FO4, $\sigma = 0.79$ FO4, SLC has improved the delay because of the output buffer.

III. MEASUREMENTS AND COMPARISONS

We compare SLC to the conventional DCVS rather than the design in [9], since the four ZVT devices in the LC of [9] make it slower than conventional DCVS at $>25^\circ\text{C}$ due to increased internal loading. The minimum size requirement of ZVT devices also makes it comparable to the size of the large pull-down devices in DCVS, such that the LC in [9] has only 17% smaller layout size than DCVS despite the use of 15× smaller pull-down devices. Hence, DCVS provides a more challenging comparison point. We measured 40 dies in 130nm CMOS; each die had two DCVS LCs and two SLCs, providing 80 LCs for each type. The LCs were designed for 0.3V to 2.5V conversion. Also, we used the simulated unit-FO4 delay to convert measured delays into FO4 delays. The unit-FO4 delay was simulated at V_{DDL} and the corresponding temperature.

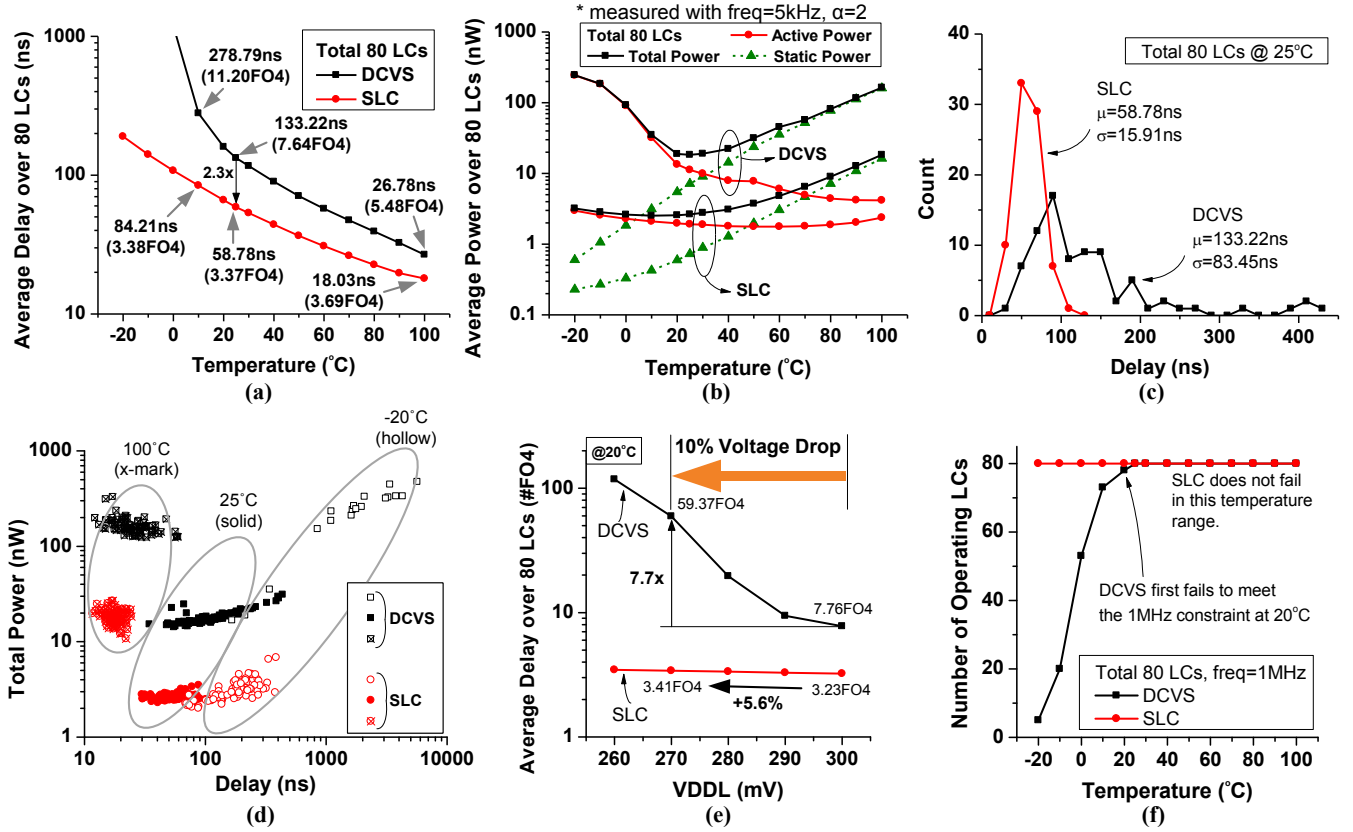


Figure 5. Measured result comparisons: (a) SLC is 2.3× faster than DCVS at 25°C. (b) SLC consumes 724pW static power (9.9× lower than DCVS) and 1.91nW active power (5.9× lower than DCVS) at 25°C. (c) Measured standard deviation of SLC is 5.2× smaller than that of DCVS. (d) SLC has narrower performance distributions and smaller power-delay products across temperature (−20°C, 25°C, 100°C). (e) With 10% V_{DDL} drop, measured DCVS delay degrades by 7.7×, while SLC speed reduces by only 5.6%. (f) SLC maintains robust 1MHz operation across the given temperature range, whereas DCVS severely degrades at low temperature.

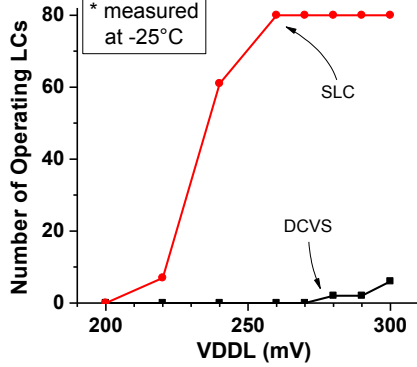


Figure 6. SLC guarantees robust operation even with > 10% V_{DDL} drop at very low temperature (−25°C).

Fig. 5(a) shows that SLC has a delay of 3.37 FO4 at 25°C, 2.3× faster than DCVS. Normalized to FO4 delay, SLC delay varies by only 9.5% over 10-100°C, while DCVS changes by more than 2×. In Fig. 5(b), the new design has 9.9× lower static power at 25°C, mainly due to the smaller pull-down devices. Also, active power is 5.9× lower than DCVS, demonstrating the benefits of reduced contention. Across 10-100°C, the active power of SLC varies by 33%, while DCVS exhibits 7.7× variation over the same range.

Fig. 5(c) shows that SLC has a 5.2× smaller standard deviation in measured delay at 25°C. The measured delay-power scatter plot in Fig. 5(d) demonstrates much better

robustness to process variations especially at the low temperature, since the exponential dependency of $I_{NMOS,ON}$ exacerbates the direct contention in DCVS.

Figs. 5(e) and (f) show the effects of voltage/temperature variations. For a 10% V_{DDL} drop, DCVS LC delay degrades by 7.7×, while SLC speed reduces by only 5.6%. Although the DCVS LC is designed to operate at up to 20MHz at 25°C, some measured DCVS LCs fail to achieve 1MHz operation at 20°C and overall its functionality severely degrades as temperature is lowered. In contrast, SLC operates reliably over the full temperature range of −20 to 100°C. SLC robustness becomes more pronounced in severe conditions, as Fig. 6 demonstrates all measured devices are functional even with >10% V_{DDL} drop at very low temperature (−25°C), whereas DCVS LC is essentially non-functional at this condition. For sensor node applications, it is critical to work in a range of environments to enable true ‘ubiquitous’ networks; hence the robustness of SLC is a key advantage for such systems.

Table I compares SLC with previously proposed wide-range LCs. The static nature of SLC does not require clocks or complex synchronization, achieving 1554× smaller area and 8.9× lower energy/transition compared to [8], which is also fabricated in 130nm CMOS. Fig. 7 shows the die photo; SLC is 35% smaller than the conventional DCVS, making it the smallest LC reported for wide-range (0.3V to 2.5V) conversions.

We incorporated SLC in a previously reported low-power timer [10] and observed 15.8% reduction in switching energy; this improvement is conservative as the new timer includes overhead from an LDO regulator, which was not included in the previous design. Fig. 8 shows the die photos of both timers. The new timer including SLC was successfully incorporated into the wireless sensor node system in the 130nm layer of [3]. This system also uses SLC (ported to 180nm CMOS) for its CPU, memory, and PMU (Power Management Unit) interfaces. This SLC consists of thick-oxide I/O devices ($V_{TH} > 700\text{mV}$) and successfully operates for a 0.6V–3.6V conversion range.

IV. CONCLUSION

A new wide-range level converter called SLC was proposed based on a split output driver topology and demonstrated with comprehensive silicon measurements of 0.3V to 2.5V conversion in 130nm CMOS. Using a novel circuit structure, SLC significantly improves speed, power, and robustness over the conventional level converters even across wide PVT spreads. Compared to recently reported level converters, SLC provides the smallest area with faster speed and the smaller energy per transition.

TABLE I. COMPARISON OF RECENT WIDE RANGE LEVEL CONVERTERS.

	SLC	TVLSI'11 [8]	ESSCIRC'07 [9] (simulation only) ^(a)
Technology	130nm	130nm	180nm
Conversion	0.3V to 2.5V	0.3V to 2.5V	0.3V to 1.8V
Type	Static	Dynamic (2.5V clock needed)	Static
Delay	58.78ns	125ns ^(b)	~600ns
Static Power	724pW	N/A	N/A
Energy per Transition	191fJ	1.7pJ ^(b)	~20pJ
Area	71.94 μm^2	0.1118mm ² (1554 \times larger than SLC)	No silicon implementation

* All comparisons are made at the room temperature.

(a) Test chip was fabricated, but only simulated results were reported.

(b) Calculated from reported numbers

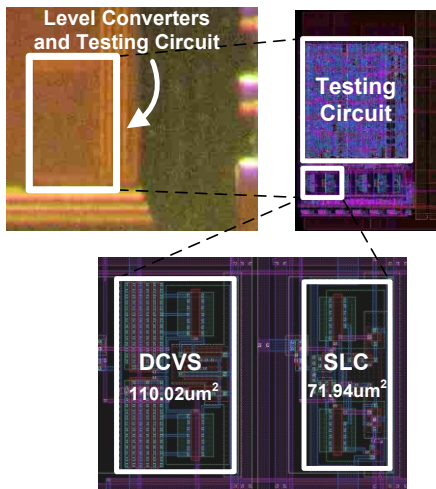


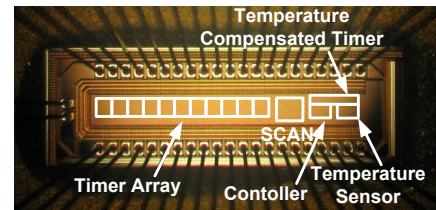
Figure 7. Die photo of SLC with the testing circuit along with close-ups of layouts. The testing circuit includes an internal clock, counters, and scan chains for delay measurements.

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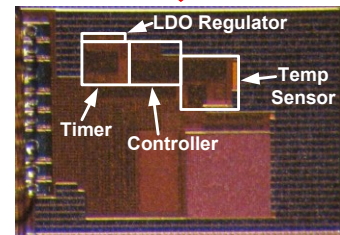
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Previously reported timer in 130nm CMOS [10]
(NOT Including LDO)
660pW/0.36Hz = 1.83nJ/switching



New timer with SLC in 130nm CMOS (including LDO) [3]
8.6nW/5.6Hz = 1.54nJ/switching

Figure 8. Die photos of low voltage timer designs.