21.5 A Fully Integrated Successive-Approximation Switched-Capacitor DC-DC Converter with 31mV Output Voltage Resolution

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Ultra-low power microsystems are gaining interest due to their applicability in critical areas of societal need. Power management in these microsystems is a major challenge as a relatively high battery voltage (ex: 4V) must be down-converted to several low supplies, such as 0.6V for near-threshold digital circuits and 1.2V for analog circuits [1]. Furthermore, the small form factors of such systems rule out the use of external inductors, making switched-capacitor (SC) DC-DC converters the favored topology [2-4].

A key difficulty in SC-converters is their coarse output voltage resolution. This limits the ability of SC-converters to respond to battery voltage droop or to perform effective load regulation. For instance, in the case of ladder SC converter [1], more fine grain output voltage control requires either of impractically large number of stages, or post SC-converter regulation using an LDO [5], significantly degrading efficiency. To overcome this limitation, this paper presents a successive-approximation switched-capacitor (SAR SC) DC-DC converter that allows for fine output voltage control to enable effective load and line regulation in ultra-low power applications. At 4V input voltage, the SAR SC has an output voltage range of 0.4-4V, with 7b 31mV step resolution, achieving 72% peak efficiency in 180nm CMOS.

Fig. 21.5.1 explains the conceptual operation of the SAR SC DC-DC converter. The central idea is to cascade multiple 2:1 SC-stages using configuration switches to obtain a fine grain output voltage (V_{out}). Each SC-stage takes two inputs (V_{high}, V_{low}) and produces an output $V_{mid} = (V_{high}+V_{low})/2$. The ($V_{high}$, V_{low}) inputs of a stage are connected through configuration switches to either (V_{high}, V_{mid}) or (V_{mid}, V_{low}) of the previous stage. In the 4-stage example of Fig. 1, V_{BAT} = 2V is converted to V_{out} = 1.125V with configuration control S[3:0]=1000 and to V_{out} = 1.250 with S[3:0]=1001, providing a 125mV step (no load condition). Hence, the key benefit of the proposed converter is very fine V_{out} resolution over a wide output voltage range while maintaining similar efficiency. Resolution is $V_{BAT}/2^{Num\_Stages}$ (in contrast to V_{BAT} / Num_Stages in a ladder SC) and $V_{out} = V_{BAT}\times Code/2^{Num\_Stages}$ under no load. Fig. 21.5.1 (bottom) shows measured outputs and ideal outputs of the 7b SAR SC from this paper with a resolution of 31.25mV at V_{BAT}=4V. The configuration switches only switch when the configuration vector changes, and hence can be made large to limit resistive loss at minimal switching energy cost.

The 7b SAR SC converter presented in this paper cascades one 4:1 converter and five 2:1 converters (Fig. 21.5.2). Each converter is two-way phase-interleaved. To enable efficient low swing clocks, the first stage is constructed using a 4:1 converter and clock generation uses V_{BAT} and VDD3Q = 3/4 × V_{BAT} as its supply and ground. By using V_{BAT} and VDD3Q, clock swing and frequency automatically increase under heavy loading conditions as VDD3Q droops. This creates negative feedback to automatically mitigate conduction loss. A conventional approach using VDD1Q and VSS would instead experience voltage droop on VDD1Q, yielding a clock frequency / swing reduction with positive feedback, limiting converter operating load range.

Capacitive level shifters are used in each converter to drive the switches. For example, gate voltage G_1 of switch S_1 is referenced to its source (VH[3]) by the cross-coupled PFET structure R_1 and R_2 (Fig. 21.5.2). It then swings low from this reference point through capacitive coupling driven by inverter I_1. Conversely, the gate G_2 of S_2 is referenced to its source VM[3] and coupled high by I_2. Since the cross-coupled PFET level shifter inherently generates two opposite polarities, a two-phase interleaving can be constructed with no effective overhead. Four switch structures are connected in parallel, sized 1×, 1×, 2×, and 4× to implement binary-weighting using the thermometer control code SEN[3:0].

A feedback (FB) and feedforward (FF) controllers are proposed, leverage the fine grain control, and react to load and line variations (Fig. 21.5.3). The FF controller predetermines a conversion ratio M0 by comparing V_{target} with a ramp voltage (V_{RAMP}) that increases by the converter voltage step $V_s = V_{BAT}/2^7$ for each cycle of CLKd, which is 32× slower than the converter switching clock (CLK). V_{RAMP} is generated using 2^7 diode-connected PFETs in series. M0 is the clock cycle count at which V_{RAMP} exceeds V_{target} and is updated every 2^7 cycles.

The M0 configuration code results in an SC output voltage (V_{out}) that matches V_{target} within one V_s under no-load conditions (V_s = 31.25mV with V_{BAT} = 4.0V). Since V_{out} droops in the presence of load, the FB controller adjusts the conversion ratio to maintain a constant output voltage. For this, two trigger voltages VP and VN are generated from the diode stack with separate 2^7:1 muxes, where VP = VF[M0+Δ_{P1}] and VN = VF[M0-Δ_{N1}]. V_{out} is compared with VP and VN at each cycle and the conversion ratio is adjusted to maintain VN < V_{out} < VP. By incrementing/decrementing a 7b CC counter and adding it to M0, the adjusted configuration code M1 (≥ M0) is obtained.

To prevent converter efficiency from being limited by conduction loss (proportional to $V_{ideal} - V_{out}$) the frequency and switch widths are dynamically modulated in a binary-weighted fashion by the FB controller. Two additional trigger voltages VP2 and VN2 are generated, where VP2 = VF[M1-Δ_2] and VN2 = VF[M1- $2\Delta_2$] (using two additional 2^7:1 muxes). In this implementation, Δ_2 is set to 5 and hence $\Delta_2\times Vs$ = 156.25mV. VP2 and VN2 are referenced to VF[M1], which is the ideal (no-load) voltage level of the SC converter at M1. When V_{out} lies within $\Delta_2\times V_s$ of this no-load output voltage (V_{out} > VP2), switching loss dominates and switch size and frequency are reduced by decrementing the switch width and frequency modulation (SWFM) counter (Fig. 21.5.3, top right). Similarly, when V_{out} falls below the no-load output voltage V_{ideal} by more than $2\times\Delta_2\times V_s$ (V_{out} < VN2), conduction loss is dominant and switch size and frequency are increased. By correctly setting Δ_2, switching and conduction losses remain balanced over a large load range, improving conversion efficiency.

Fig. 21.5.4 shows measurements of FB controller operation. As the load current increases from 0 to 300μA (V_{BAT} = 4V, V_{target} = 1.2V), the conversion code increases to compensate for conduction loss. When $V_{out}-V_{ideal} > 2\times\Delta_2\times V_s$ the feedback controller increments the SWFM counter, increasing clock frequency. The counter saturates at a load current of 30μA. Fig. 21.5.5 (top left) shows how the fabricated converter generates target voltages 0.9V, 1.2V, and 1.5V for V_{BAT} ranging from 3.4-4.3V. V_{out} variation depends on VP–VN, set at 3×V_s (93.75mV), and comparator offset in the FB controller. Regulation is within ±81mV of V_{target}. Conversely, load current is swept from 0 – 300μA for V_{target}=0.9V, 1.2V, and 1.5V with V_{BAT} fixed at 4.0V (Fig. 21.5.5 right). The converter achieves peak efficiency of 69%, 65%, and 72% with output voltage regulation within ±54mV, ±41mV, and ±81mV for V_{target} = 0.9V, 1.2V, and 1.5V, respectively. The effectiveness of dynamic SWFM is shown in Fig. 21.5.5 (bottom left) and demonstrates that efficiency >50% is achieved across 2-300μA load using dynamic SWFM compared to 30-300μA for a single setting (SWFM = 3). Transient step response waveforms and a comparison to prior work are shown in Fig. 21.5.6. The fabricated test chip with 2.24nF on-chip capacitance occupies 1.69 mm^2 in 180nm CMOS.

References

[1] Y. Lee, et al., "A Modular 1mm^3 Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting," ISSCC, Feb. 2012.

[2] V. Ng, et al., "A 92%-Efficiency Wide-Input-Voltage-Range Switched-Capacitor DC-DC Converter," ISSCC, Feb. 2012.

[3] Y. K. Ramadass, et al., "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45nm CMOS," JSSC, Dec. 2010.

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[7] M. Seok, et al., "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5V," JSSC, Oct. 2012.

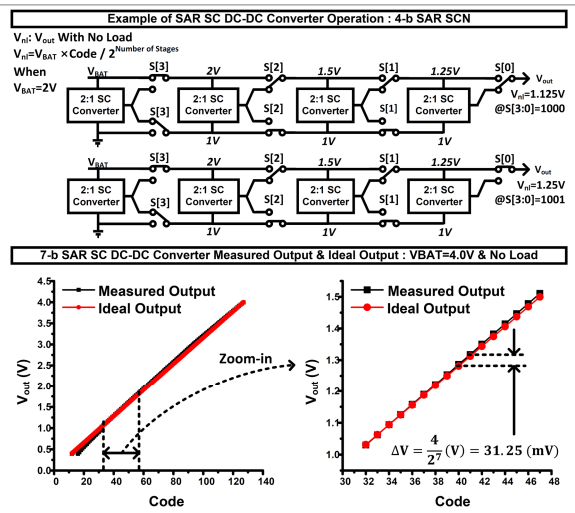


Figure 21.5.1: An example of 4-b SAR SC converter operation (top). Measured and ideal values of V_{out} vs. Code at V_{BAT}=4.0V under no-load condition for the proposed SAR SC converter (bottom).

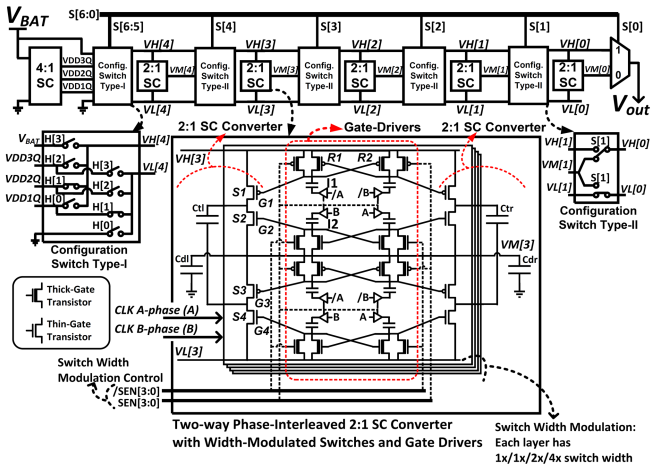


Figure 21.5.2: Schematic of the proposed 7-b SAR SC DC-DC converter (top). Detailed schematics (bottom).

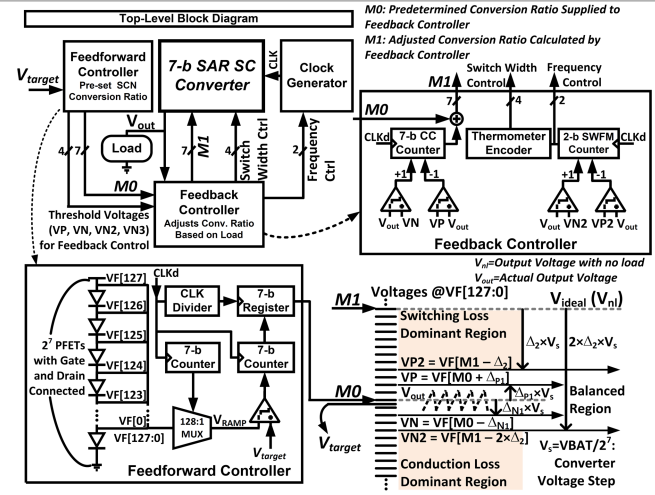


Figure 21.5.3: Top-level block diagram (top left). Feedback controller (top right). Feedforward controller (bottom left). Trigger voltages (bottom right): V_{target} can be generated by ultra-low power V_{ref} circuits [6-7].

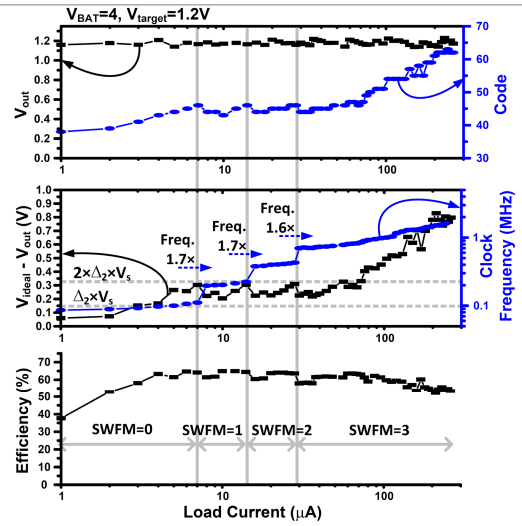


Figure 21.5.4: Measured results. V_{out} and code vs. load current (top). V_{ideal}-V_{out} and clock frequency vs. load current (middle). Efficiency vs. load current (bottom).

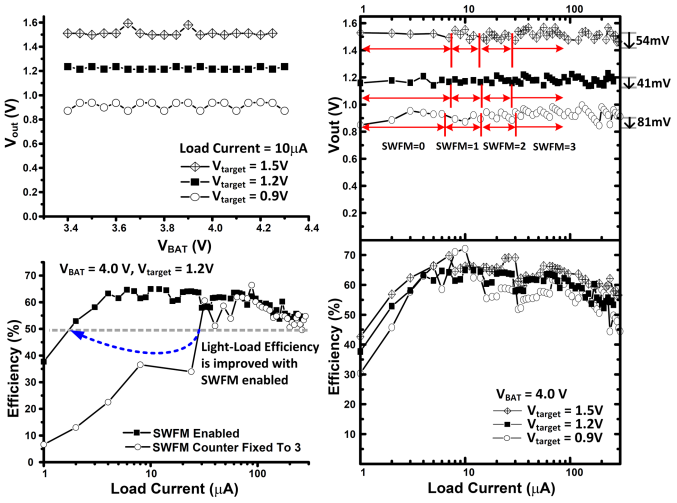
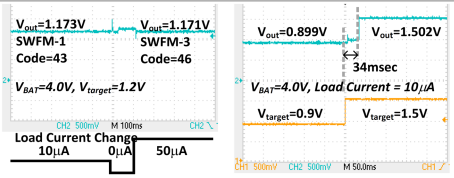


Figure 21.5.5: Measured V_{out} vs. V_{BAT} (top left). Measured V_{out}, and efficiency vs. load current (right). Measured efficiency vs. load current with SWFM enabled, and SWFM counter fixed to 3 (bottom left).



Metric	This work	[2]	[3]	[4]
Input Range	3.4V-4.3V	7.5V-13.5V	1.8V	1.2V
Output	0.9V-1.5V	1.5V	0.8V-1V	0.3V-1.1V
Number of Conversion Ratios	20 for 0.9V-1.5V (117, for 0.4V-4.0V) @V_{BAT}=4.0V	7	1	5
Step size	31.25mV @V_{BAT}=4.0V	N/R	N/R	≥ 0.1V
Output Variation	54mVpp @V_{BAT}=4.0V, V_{target}=1.5V 41mVpp @V_{BAT}=4.0V, V_{target}=1.2V 81mVpp @V_{BAT}=4.0V, V_{target}=0.9V	30mVpp	N/R	N/R
Maximum Load Current	0.3mA	1A	8mA	1mA
Clock Frequency	80kHz-1.7MHz @V_{BAT}=4.0V, V_{target}=1.2V	50MHz	30MHz	15MHz
Peak Efficiency	69% @V_{BAT}=4.0V, V_{target}=1.5V 65% @V_{BAT}=4.0V, V_{target}=1.2V 72% @V_{BAT}=4.0V, V_{target}=0.9V	92%	69%	>70%
Technology (nm)	180	180	45	180
Area (mm^2)	1.69	11.55	0.16	2.56
Capacitor	On-Chip	Off-Chip	On-Chip	On-Chip

Figure 21.5.6: Transient load step response (top left). Transient V_{out} response in the presence of V_{target} change (top right). Comparison table (bottom). N/R = Not reported.