10.9 A 0.45V 423nW 3.2MHz Multiplying DLL with Leakage-Based Oscillator for Ultra-Low-Power Sensor Platforms

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Emerging demands on ultra-low-power wireless sensor platform have presented challenges for nano-watt design of various circuit components. Clock management unit, as an essential block, is one of the most actively researched blocks. It is required to distribute various frequency ranges for energy-optimal operation, e.g., Hz for internal timer [1], kHz for global clock [2], and MHz for fast data transmission or intensive signal processing [3]. However, free-running oscillators are seriously affected by process variations and should be readjusted by post-fabrication trimming. Though a crystal gives a stable frequency, the use of multiple crystals is generally not allowed by limited form-factor and increased cost. Instead, frequency multiplication from one clean reference is more effective way for higher frequency generation. Considering high-frequency clock is only intermittently used in sensor applications, the clock multiplier should provide a fast settling when turned on as well as low-power dissipation. This paper presents a 423nW, 3.2 MHz all-digital multiplying DLL (MDLL) with a digitally controlled leakage-based oscillator (DCLO) and a fast frequency relocking scheme adaptive to the amount of frequency drift during sleep state, which is required for intermittent operation of sensor node platforms.

A commonly used figure-of-merit (FoM) for energy efficiency in clock generation is defined by power consumption per generated frequency (W/Hz) [2]. Since an oscillator consumes the largest power in clock generation, low-power oscillator design is essential for better energy efficiency. For a given target frequency, as it is mainly determined by RC time constant, it is desired to have larger resistance and smaller capacitance to minimize the charging current. The minimum capacitance is achieved by using intrinsic device parasitics only. The use of the minimum capacitance makes it easy to implement a smaller RC time constant with implementable range of resistances. Therefore, it is easier to obtain better energy efficiency for high-frequency (> GHz) clock generation with additional benefits from scaled technology. For low-frequency clock generation (< 10MHz), however, the resistance needs to be unreasonably large if parasitic-only minimum capacitance is to be used. So an extra capacitance should be added for an implementable resistance value. In addition, if an oscillator is used in digital MDLL or PLL, it should be digitally controlled with a fine frequency step. For this purpose, large extra capacitance with fine resolution is conventionally added to cover a wide frequency lock range, and it eventually degrades the energy efficiency. Alternative approach with current-starved charging scheme also consumes a significant DC power in bias circuits. In addition, current mirror array implemented with large-length transistors for small current step causes a huge gate capacitance on the bias node which results in a long settling time during intermittent operation.

Figure 10.9.1 shows the concept of the proposed DCLO which uses leakage current of PMOS device to achieve a large effective resistance. If the drain of PMOS is connected to power, all the device leakages from channel, gate, and junction flow into the capacitor. On the other hand, if the drain is connected to the ground, only small portions of the gate and junction leakages flow into the capacitor since the gate and bulk are tied up to power. So the leakage current can be controlled digitally by simply connecting the drain of PMOS to power or ground. Compared with the gate-leakage based oscillator used for a several Hz-range timer [1], the channel leakage is generally orders of magnitude larger and less process dependent, which makes it more suitable for MHz-range clock generation and controllable oscillator.

Considering the reference frequency (f_{ref}) for sensor platform is usually several tens of kHz, the effect of in-band noise to the total jitter is crucial if clock multiplication is performed using PLL whose bandwidth is limited to $0.1\times f_{ref}$ for the loop stability. Therefore, MDLL is better choice for the clock multiplier in sensor platforms. Figure 10.9.2 shows the top block diagram of the proposed MDLL, which consists of a relaxation-based DCLO, a frequency detector (FD), a lock detector (LD), and an FSM for generating MUX selecting signal (SEL) and update clock ($f_{ref}/3$) of DCLO code. DCLO is controlled in three steps; a coarse binary 6b with SAR, a fine binary 6b with SAR, and a finer thermometer 64b with a shift register (SR). The parasitic capacitance due to transistor arrays (~50fF) provides the minimum charging capacitance. In every N-cycle, FSM sets SEL to inject the f_{ref} into the pulse generator instead of the feedback pulse. Since the edge of output clock is substituted with the clean f_{ref}, accumulated jitter can be eliminated in every reference cycle. FD compares f_{out}/N with f_{ref} and drives DCLO controller. LD checks whether a pre-defined lock condition is met and triggers LOCK which holds DCLO control code.

Figure 10.9.3 shows the lock procedure. After the coarse and fine codes are set, the finer 64b thermometer code is updated according to FD output until the lock condition is met. LD checks the lock condition in every f_{ref} cycle. If the oscillator output drifts, LD releases the LOCK signal and the finer lock step is re-performed. When MDLL is turned off (sleep mode), the coarse and fine codes are stored. After wake-up, the initial output frequency is set by the previously stored coarse and fine codes with the finer code reset to the center code. Assuming f_{drift} is the difference between the initial output frequency after wake-up and the target frequency, $|f_{drift}|$ is compared with $f_{finer\_range}/2$. f_{finer_range} represents the total frequency range to be covered with the finer code. If f_{drift} is small enough to be tracked by the finer control only ($|f_{drift}|<f_{finer\_range}/2$), the locking procedure is performed in the finer step. If not, $|f_{drift}|$ is compared with $f_{fine\_range}/2$, and the locking procedure starts from the coarse step or the fine step depending on the comparison result.

The MDLL is implemented in a 65 nm CMOS. The core area is 0.026 mm^2. With a 32kHz reference, the MDLL generates 3.2MHz (N=100) and consumes 423nW from a 0.45V supply, achieving an FoM of 0.132μW/MHz. Figure 10.9.4 shows measured locking transients after wake-up, for the cases of large (upper) and small (lower) frequency drifts. The proposed f_{drift} adaptive locking can greatly reduce the power consumption for the re-locking with a small drift, which is especially useful for biomedical applications with little change in temperature environment. The measured phase noise (Fig. 10.9.5) clearly reveals the rejection of the in-band noise below 32kHz, which dominates the total jitter. Integrated rms jitter from 10kHz to 1MHz is 7.98ns (2.5% of clock period). Harmonic spurs from reference clock have very little contribution to the total jitter performance (7.96 ns without spurs, calculated). The out-of-band noise is -95dBc/Hz at 1MHz offset, which is similar to that of PLL/MDLL with general inductorless oscillator [4]. This work achieves an FoM which is about 2× better than the previous lowest [5] and over 50× better than previous implementation [6] with similar frequency range. Figure 10.9.7 shows a chip micrograph.

Acknowledgement:
This work is partly supported by NRF under grant No. 2011-0010685 and 2012-0000625, and IDEC of Korea.

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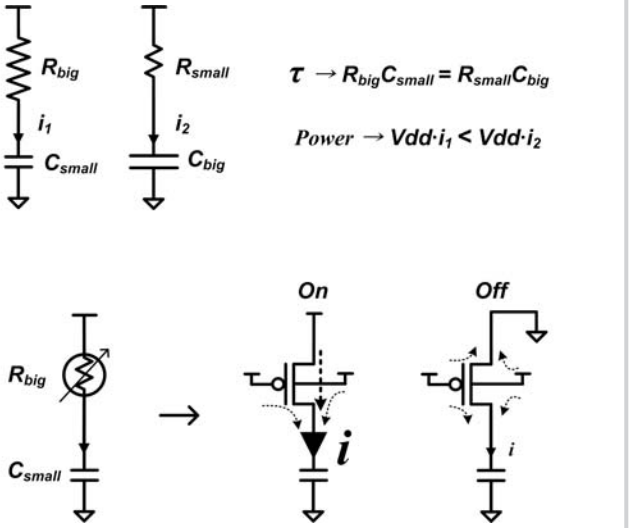


Figure 10.9.1: Concept diagram of digitally controlled leakage-based oscillator.

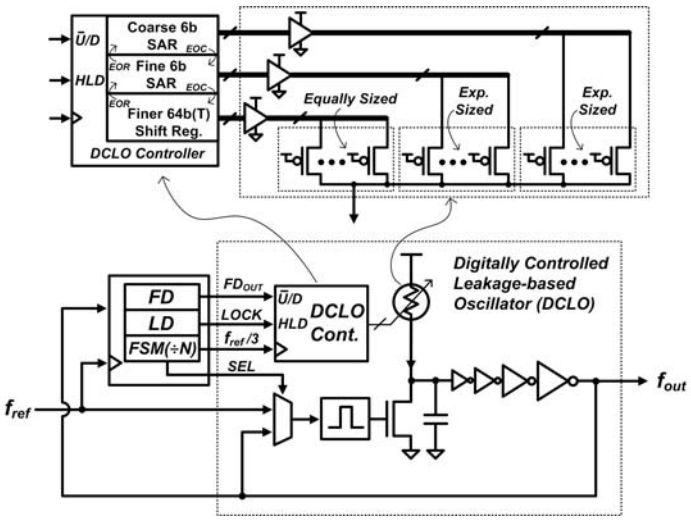


Figure 10.9.2: Block diagram of the proposed all digital MDLL.

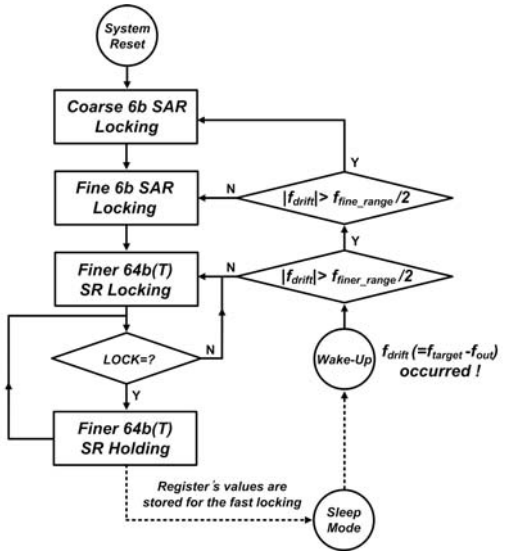


Figure 10.9.3: Lock procedure.

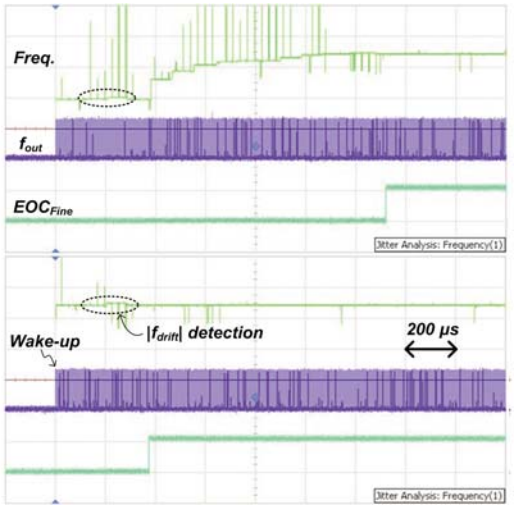


Figure 10.9.4: Measured locking transients after wake-up with (upper) a large frequency drift and (lower) a small frequency drift.

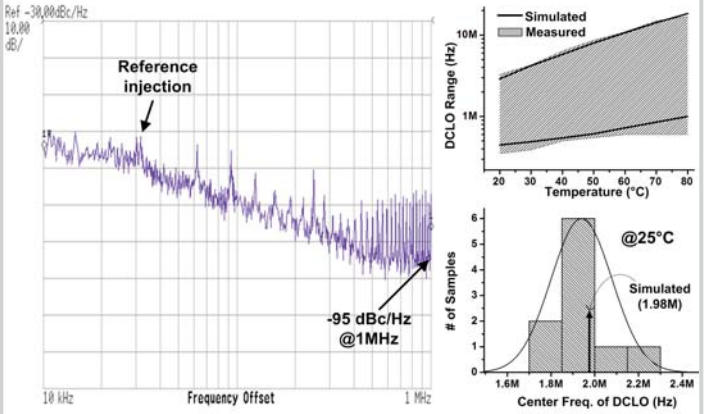
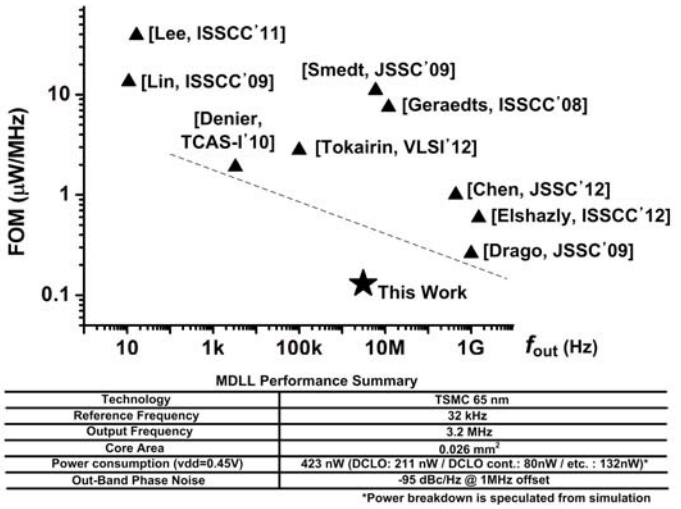


Figure 10.9.5: Measured MDLL phase noise and DCLO characteristics with temperature and process variations.



MDLL Performance Summary

Technology	TSMC 65 nm
Reference Frequency	32 kHz
Output Frequency	3.2 MHz
Core Area	0.026 mm^2
Power consumption (vdd=0.45V)	423 nW (DCLO: 211 nW / DCLO cont.: 80nW / etc. : 132nW)*
Out-Band Phase Noise	-95 dBc/Hz @ 1MHz offset

*Power breakdown is speculated from simulation

Figure 10.9.6: Performance comparison and chip summary.

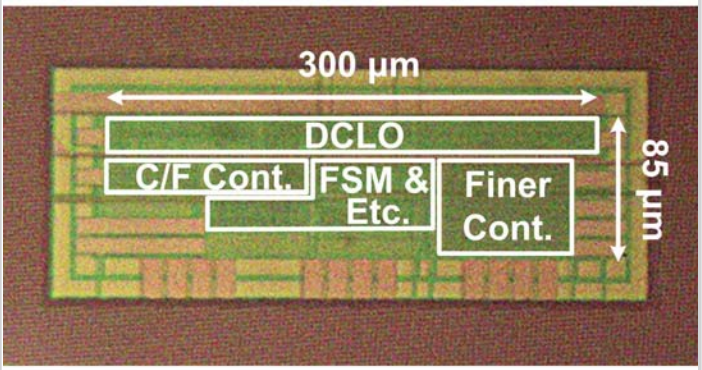


Figure 10.9.7: Chip micrograph.

978-1-4673-4516-3/13/$31.00