Guest Editorial

THE ACM/IEEE Design Automation Conference (DAC) is now celebrating its 40th anniversary. During its history, it has served both the academic and the industrial communities by providing a unique mix of a top-level trade show and a strong, vibrant technical program.

This issue of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (TCAD) includes a selection of some of the best papers that were presented at the 39th Annual DAC, in June 2002. Nominations for the selected papers were first chosen by the DAC Technical Program Committee based on their technical strength, with also some consideration for providing an overview of the broad class of topics included in the DAC technical program every year. The authors of the nominated DAC papers were then asked to submit extended versions of their papers to TCAD, which went through a sequence of rigorous independent reviews and revisions to identify and produce the final selection which is found in this issue.

The first two papers are devoted to embedded systems, in particular to embedded software code generation. DAC has recognized in the last few years the shift from dedicated systems to programmable systems, because of the increasing non-recurrent engineering costs suffered by application-specific integrated circuits (ASICs), due to increasing design team size and skyrocketing mask production cost. The growing emphasis on embedded systems, in which computers are used to perform some control or communication function, is also due to their taking up the role of technology driver that once belonged to PCs. Finally, several solutions to "traditional" CAD problems can be reused profitably to tackle issues in design automation for embedded software, beyond the traditional compiler/linker/debugger chain. As a result, approximately one third of the technical program at DAC is now devoted to embedded systems in general, and to embedded software in particular.

The first paper in this issue is dedicated to the problem of matching complex sequences of code, e.g., those used to compute a numerical approximation of a mathematical function, to special dedicated instructions on an application-specific instruction processor, or to efficient prewritten library routines. The goal is to move beyond purely graph-based pattern matching techniques that have been traditionally used in compilers, and to consider the function which is being computed as the target to match, rather than the sequence of code used by the programmer to model it.

The second paper discusses the very important issue of properly assigning addresses to scalar and vector variables of a given embedded program, so that irregular architectures, such as digital signal processors (DSPs), can access them faster. The reason why address assignment is so significant for DSPs is that the instruction sets of those processors are strongly nonorthogonal. They often are able to address data memories only via special-purpose address registers, which can perform only a limited number of operations, such as modulo addition of small constants. The paper proposes a unified method to handle all known problems that have been formulated for address assignment, in order to achieve significant improvements in terms of code size and execution time.

The third paper addresses the problem of replacing paper catalogues, which have been the traditional tool used by board designers to select integrated circuits, with a web-based technology. The target of this paper is also different from fixed ICs, because it deals with intellectual property blocks to be instantiated in ASIC designs. Such blocks exhibit a large degree of flexibility and variability in order to adapt to different timing and area tradeoffs, different implementation technologies and so on. As a result, the problem of their selection becomes much more difficult, and also involves hard security problems, since the model used for preliminary evaluation must not allow the prospective user to acquire the block without paying for it.

The fourth paper tries, for the first time, to measure the amount of work which has been done at a certain stage of execution by a potentially extremely expensive algorithm: a satisfiability solver. Since all known SAT solvers have an exponential worst-case behavior, the authors argue that it is very beneficial for the user to know how far the algorithm has gone in its search, in order to decide whether or not to stop it and try something else. The "searched space" measure could also be used by automated heuristics in order to trim the search tree by properly selecting the visiting order. SAT is one of the basic engines of most industrial equivalence checking tools, and it is being advocated as a general-purpose algorithm to solve a variety of combinatorial optimization problems in CAD. Thus it is very important to speed up its implementations and provide feedback to users about how long they might still have to wait for an answer.

The fifth paper addresses the problem of functional verification, which has become a critical problem for very large scale integration design as integration levels continue to soar. Specifically, the paper provides an efficient solution to problems encoded using propositional logic. Since no single proof method is adequate for all problems, the paper presents a framework within which multiple proof strategies can be effectively composed into a single, powerful strategy which is applied to combinational equivalence checking and bounded model checking.

The sixth paper addresses the issue of logic circuit synthesis using three-level logic implementations, which allows for significantly more efficient implementations than traditional two-level sum-of-products implementations while presenting a more tractable minimization problem than general multilevel synthesis. The paper develops a new method for the identification of regularity or“auto-symmetry in a three-level Boolean representation using the pseudoproducts form. This allows the construction of so-called restricted”functions which depend on a reduced number of variables and whose optimal solution can be computed with much reduced runtime. It is then shown how, based on the optimal solution of the restricted form of a function, the optimal solution of the function itself can be constructed in linear time. The paper demonstrates that most

Digital Object Identifier 10.1109/TCAD.2003.816086

outputs of classical benchmark circuits exhibit significant autosymmetry and makes an argument that, in general, most functions of interest also have this feature.

The seventh paper addresses the necessity for abstract modeling of analog blocks in system-level simulations of complex communication systems. Such models allow significant improvement in simulation efficiency and also enable tradeoff analysis during system-level design. More specifically, the paper develops a new approach for constructing behavioral models for harmonic oscillators and sets of coupled harmonic oscillators through a sequence of transformations of the circuit equations. The approach has the benefit that it separates the slow and fast varying components of the oscillator behavior, which allows an increase in the simulation time step, thereby further improving simulation efficiency.

The final paper addresses the domain of efficient interconnect modeling through the use of reduced-order modeling approaches, which have become commonplace in CAD tool flows. The paper is focused on truncated balanced realization (TBR) algorithms which have been shown to achieve a smaller model size than methods using efficient Krylov-subspace iterations, but have the critical problem of not necessarily preserving the passivity of original system. The paper overcomes this difficulty by presenting a new TBR-like method which maintains the efficiency of the reduced order model, but also guarantees the passivity of the obtained model.

DAVID T. BLAAUW, *Guest Editor*
Department of Electrical Engineering
and Computer Science,
University of Michigan,
Ann Arbor, MI 48109 USA

LUCIANO LAVAGNO, *Guest Editor*
Department of Electronics,
Politecnico di Torino,
10129 Torino, Italy

David T. Blaauw (M'01) received the B.S. degree in physics and computer science from Duke University, Durham, NC, in 1986, and the M.S. and Ph.D. degrees in computer science from the University of Illinois, Urbana, in 1988 and 1991, respectively.

He was with the Engineering Accelerator Technology Division, IBM Corporation, Endicott, NY, as a Development Staff Member, until August 1993. From 1993 to August 2001, he was with Motorola, Inc., Austin, TX, where he was the Manager of the High Performance Design Technology Group. Since August 2001, he has been a member of the faculty at the University of Michigan, Ann Arbor, as an Associate Professor. His work has focused on VLSI design and CAD with particular emphasis on circuit analysis and optimization problems for high-performance and low-power designs.

Dr. Blaauw was the Technical Program Chair and General Chair for the International Symposium on Low Power Electronics and Design, in 1999 and 2000, respectively, and was the Technical Program Co-Chair and member of the Executive Committee of the ACM/IEEE Design Automation Conference in 2000 and 2001.

Luciano Lavagno (S'88–M'93) graduated in electrical engineering from Politecnico di Torino, Torino, Italy, in 1983. He received the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley, in 1992.

From 1984 to 1988, he was with CSELT Laboratories, Torino, Italy. In 1988, he joined the Department of Electrical Engineering and Computer Science, University of California, Berkeley, where he worked on logic synthesis and testing of synchronous and asynchronous circuits. He is a co-author of two books on asynchronous circuit design and a book on hardware/software codesign of embedded systems and has published over 100 journal and conference papers. Between 1993 and 1998, he was an Assistant Professor with Politecnico di Torino, and between 1998 and 2001, he was an Associate Professor with the University of Udine, Udine, Italy. From 1993 to 2000, he was the Architect of the POLIS project (a cooperation between the University of California, Berkeley, Cadence Design Systems, Magneti Marelli, and Politecnico di Torino), developing a complete hardare/software codesign environment for control-dominated embedded systems. He is currently an Associate Professor in the Department of Electronics, Politecnico di Torino, Italy, and a Research Scientist with Cadence Berkeley Laboratories, Berkeley, CA. He has also been a consultant for various EDA companies, such as Synopsys and Cadence. His research interests include the synthesis of asynchronous and low-power circuits, the concurrent design of mixed hardware and software embedded systems, and dynamically reconfigurable processors.

Prof. Lavagno has served on the technical committees of several international conferences in his field (e.g., the Design Automation Conference, the International Conference on Computer-Aided Design, the International Conference on Computer Design, and the Design Automation and Test in Europe) and of various other workshops and symposia. He received the Best Paper Award at the 28th Design Automation Conference, San Francisco, CA, in 1991.