# 15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR

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**Abstract**

An incremental zoom-in capacitance-to-digital converter (CDC) is proposed. By using a 9b SAR, the OSR can be reduced to only 32, significantly improving conversion energy. We show how the OTA in the SAR is bypassed for the CDC further reducing energy and propose a novel matrix based 512-element unit-cap structure for dynamic element matching. The CDC achieves 94.7dB SNR and 33.7μW power consumption with 175fJ/conv-step at 1.4V supply.

**Introduction**

Capacitive sensors are widely used in wireless microsystems to measure pressure, proximity [1] and humidity [2]. In these types of applications battery life is very limited, requiring low conversion energy despite the need for high resolution. SAR CDCs have obtained conversion energies as low as 7.9pJ/c.s. [3], but with limited resolution (ENOB=6.9b). On the other hand, ΣΔ converters can obtain much higher resolution (up to ENOB=13.8b), but at the cost of higher conversion energy (FoM=21pJ/c.s.) [1].

To maintain high accuracy while reducing conversion energy, we propose a zoom-in, incremental ΣΔ CDC. The zoom-in nature restricts the converter to near-DC inputs [4], which is appropriate for sensor nodes where environmental parameters (and hence capacitance readings) change very slowly. A zoom-in ADC with 6b SAR and an over-sampling ratio (OSR) of 2000 was previously proposed in [5]. However, due to the modest SAR accuracy, the ΣΔ power remained dominant. In this work, we focus instead on a CDC and also increase the accuracy of the SAR to 9 bits with an OSR of only 32 to create a more balanced and lower overall power budget.

While significantly reducing conversion energy, a 9b SAR faces two key challenges: 1) due to the increased importance of SAR power, the OTA that traditionally operates during the SAR phase becomes a major contributor to power. To address this we leverage the unique structure of the CDC and by-pass the OTA in the SAR phase, eliminating its power consumption during this phase. 2) With a 9b SAR, the dynamic element matching (DEM) during the ΣΔ phase requires a 512 element capacitive-DAC (CDAC). This incurs significant area and power overhead. Hence, we propose a new matrix based unit-cap structure with integrated row/column addressing.

**Proposed Technique**

Fig. 1 describes the overall structure of the proposed CDC. During the initial SAR phase, the integration path is bypassed and the 9b SAR creates the integer output component, N. This is followed by a high resolution 2nd order incremental ΣΔ converter that produces the fractional output component, F. For a CDC, the sensed capacitor ($C_{sensor}$) is an off-chip component and an on-chip CDAC is used as a reference (Fig. 2). In the sampling phase (Fig. 3), $n_{cs+}$ and $n_{cs-}$ nodes are set to the common node voltage (VCM) and GND, respectively, and all bottom plates of the CDAC are set to VDD. At the beginning of the SAR phase, $n_{cs-}$ becomes VDD, and a half of the CDAC bottom plates are set to GND. After a comparator determines MSB value of N, the other bottom plates are determined using successive approximation, which results in a near VCM final value for $n_{cs+}$.

Asynchronous logic gates [6] are used for fast conversion, which allows the SAR conversion to finish within a cycle of global clock, and reduces the static power during SAR conversion by 90%. In order to provide 50% operating margin (-1<F<1) for ΣΔ phase, 0.5-bit is shifted during sampling and the ΣΔ operates with (N-1,N+1) [5]. The 0.5-bit shift is implemented with an additional unit-size capacitor ($C_u$) of the CDAC. The bottom plate of $C_u$ is set to GND during sampling and to half VDD during the SAR phase. Since the OTA is bypassed during initial SAR operation, the SAR bits are obtained with negligible energy compared to bits from the subsequent ΣΔ stage. The comparator is a two-stage sense amplifier [6] with ~100μV resolution for the 9b SAR conversion. The maximum SAR resolution is constrained by CDAC mismatch and comparator noise.

After the SAR phase, the 2nd order incremental converter provides added resolution based on the SAR result (Fig. 2). The architecture is a 2nd order feed-forward structure, similar to [4]. The SAR output error is already small due to its 9b resolution. As a result, any path mismatch between the SAR and ΣΔ will cause the ΣΔ stage output to stick at all ones or all zeroes. By using the same path between SAR and ΣΔ, we minimize the mismatch effect. φ1 and φ2 are 150kHz non-overlapping clocks. OTAs are cascoded inverter amplifiers as in [5]. $OTA_1$ and $OTA_2$ consume 12μW and 1μW, respectively.

In order to suppress CDAC mismatch, we employ 1st order dynamic element matching (DEM) with a new indexing structure (Fig. 5). DEM uses unit-cap rotation, with every cycle using the next neighboring capacitors. In a conventional design, 512 control lines are required to control the 9b CDAC. The activity ratio of all the lines is 0.5 because of DEM operation. These lines are long and exhibit strong mutual coupling, resulting in a large power overhead. To reduce both power and area, we introduce a matrix unit-cap organization. Each unit-cap is enabled when it falls between the asserted column/row *start* and *end* signals. Row and column decode logic generates the *start* and *end* signals (each a 1-hot encoding). The end index changes at the rising edge of φ2, which reflects the output of the comparator-updated at φ1. The start index is copied over from the end index at the rising edge of φ1, which results in turning off of all capacitors. Each unit-cap bottom plate signal is latched with a delayed clock. Signal *carry_in* is used to invert the unit-cap selection, which is necessary when selected unit-caps wrap around from the end to the beginning of the matrix. The complete CDAC is constructed from four 7b unit-cap matrices organized in a common centroid (CC) layout.

The logic controller and digital loop filter are fully synthesized. Since the clock is slow (150kHz), minimum-size standard cells are used to reduce clock power. The digital loop filter (Fig. 4) is a second-order digital integrator which mimics the analog integral path.

**Measured Results**

The proposed CDC is implemented in 180nm CMOS. Fig. 6 shows how output codes (N.F) are generated. The SAR output has only a 1 code error and this error is tolerable in the ΣΔ converter. CDC linearity test is performed by changing input voltage. In Fig. 7, almost all errors are within ±50 ppm (=14.3b) when DEM and CC indexing modes are ON. When CC indexing is OFF, CDC deviates from the ΣΔ working range more often, resulting in spur harmonics. When DEM is OFF, SAR and ΣΔ use different CDAC elements and it loses all bits from the ΣΔ operation because of capacitor mismatch. SNR and FoM across OSR and sampling rate are shown in Fig. 8 and Fig. 9. SNR is obtained through the ratio of effective output range rms value and output rms noise. Fig. 10 shows power consumption across sampling rate with 11% being consumed by synthesized digital logic for signal control and decimation filters. . In pressure testing with a MEMS capacitive absolute pressure sensor [7], we obtain 0.28mmHg resolution. Fig. 13 compares to other CDCs in the literature. This work achieved 94.7dB SNR, 0.16fF resolution, and 175fJ/c-s FoM at 32 OSR and 4.29kS/s

**References**

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[2] Z. Tan, et al., VLSIC 2012, pp. 24-25.
[3] K. Tanaka, et al., ASSCC 2007, pp. 244-247.
[4] J. Markus, et al., TCAS-I, 2004, pp. 678-690.
[5] Y. Chae, et al., JSSC, 2013, pp. 3019-3027.
[6] P. Harpe, et al., JSSC, 2011, pp. 1585-1595.
[7] SCB10H, http://www.muratamems.fi

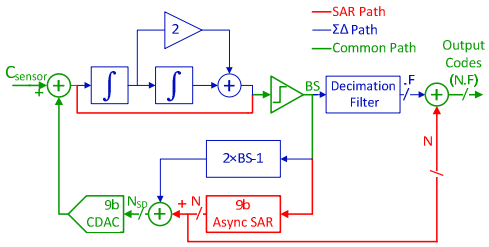


Fig. 1. Block diagram of CDC.

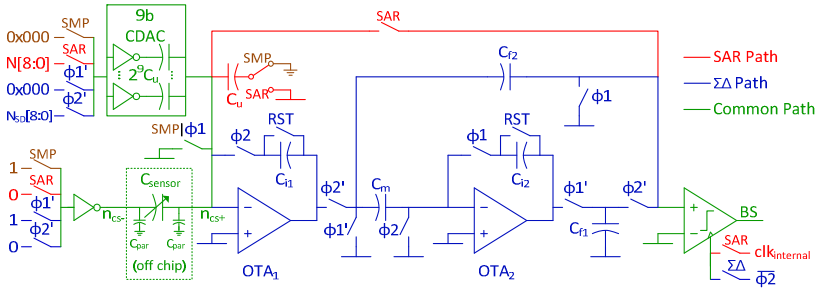


Fig. 2. Circuit diagram showing integration of 9b SAR and ΣΔ structure.

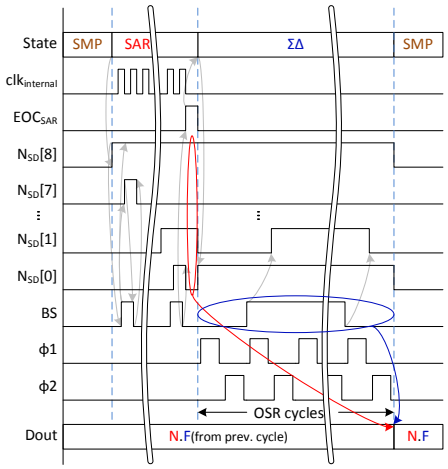


Fig. 3. Waveform of operation.

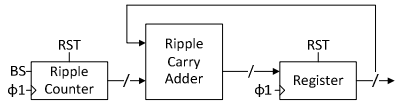


Fig. 4. Decimation filter.

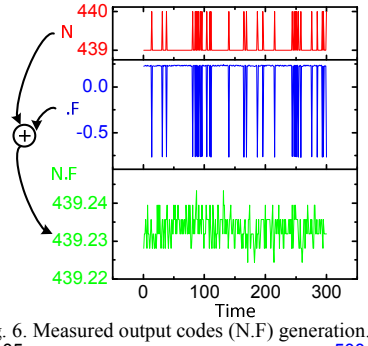


Fig. 6. Measured output codes (N.F) generation.

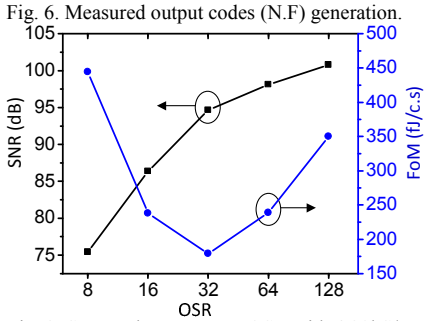


Fig. 8. SNR and FoM across OSR with 4.29kS/s.

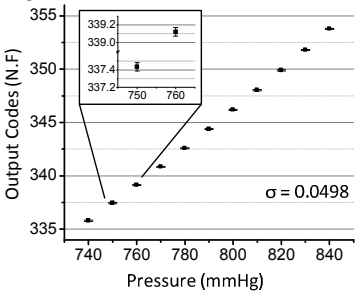


Fig. 11. Pressure sensor test with CDC.

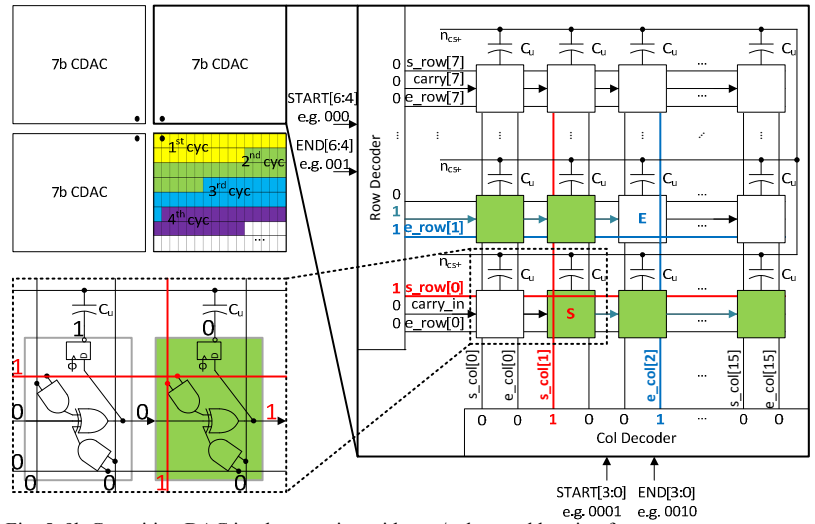


Fig. 5. 9b Capacitive-DAC implementation with row/column addressing for common centroid layout and dynamic element matching.

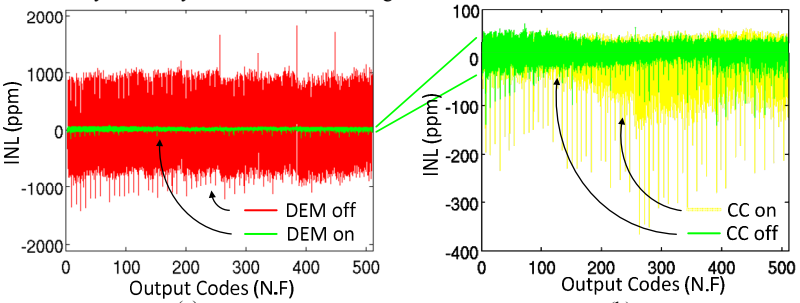


Fig. 7. INL across modes (a) dynamic element matching on/off with common centroid indexing on, (b) common centroid indexing on/off with dynamic element matching on.

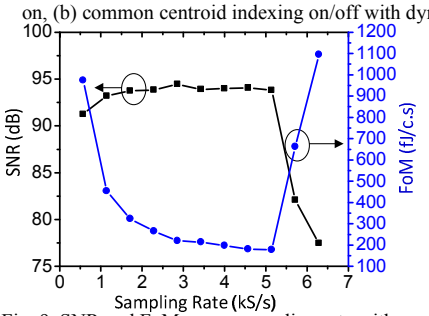


Fig. 9. SNR and FoM across sampling rate with 32 OSR.

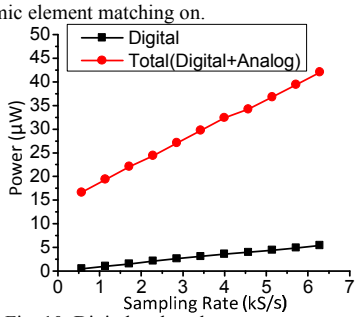


Fig. 10. Digital and analog power across sampling rate with 32 OSR.

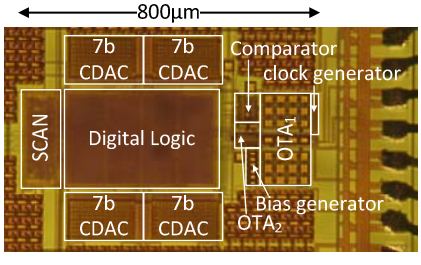


Fig. 12. Die photo.

| | This Work | [1] | [2] | [3] |
|---|---|---|---|---|
| Technology(μm) | 0.18 | 0.35 | 0.16 | 0.18 |
| Method | Incremental ΣΔ + Zoom in SAR | ΣΔ | ΣΔ | SAR |
| Input Range(pF) | 0 ~ 24 | 8.4 ~ 11.6 | 1.2 ~ 1.8 | N/A |
| Meas. Time(μs) | 230 | 20 | 800 | 4 |
| Power | 33.7 μW | 14.9 mW | 10.3 μW | 240 μW |
| SNR(dB) | 94.7 | 84.8 | 69.6 | 43.2 |
| FoM(pJ/c-s) | 0.175 | 21 | 3.4 | 7.9 |

$$\text{SNR} = 20\log\left(\frac{Full\ Range\ /2\sqrt{2}}{Resolution}\right) \qquad \text{FoM} = \frac{Power\ \times\ Meas.\ Time}{2^{(SNR-1.76)/6.02}}$$

Fig. 13. CDC comparison table.