

System-On-Mud: Ultra-Low Power Oceanic Sensing Platform Powered by Small-Scale Benthic Microbial Fuel Cells

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Abstract—A self-sustainable sensing platform powered entirely by small-scale benthic microbial fuel cells (MFCs) for oceanic sensing applications is presented. An ultra-low power chip featuring an ARM Cortex-M0 processor, 3 kB of SRAM, and power management unit (PMU) is designed to consume 11 nW in sleep mode for perpetual sensing operation. The PMU includes a switched-capacitor DC/DC converter designed for efficient energy harvesting and step-down conversion for a wide range of input and output power. A small-scale MFC with 21.3 cm² anode surface area was connected to the PMU to charge a thin-film battery of 1 mAh capacity. A 49.3-hour long-term experiment with 8-min sleep interval and 1-s wake-up time demonstrated the sustainability of system-on-mud concept. During sleep mode operation, the system charges the 4 V battery at 380 nA from the micro-MFC generating 5.4 μW of power, which allows up to 20 mA of active mode current with net energy neutrality.

Index Terms—Capacitive power management, energy harvesting, MFCs, microbial fuel cells, oceanic system, sensor node, switched-capacitor DC/DC converter.

I. INTRODUCTION

BENTHIC microbial fuel cells (MFCs) generate energy through the metabolic process of bacteria in marine sediment. To generate power, an anode of the MFC must be in contact with bacteria in anaerobic condition while a cathode floats in the water column where it is exposed to oxygen (Fig. 1) [1], [2]. Electrodes with larger surface area can generate higher power. However, with larger electrodes, the anode becomes a limiting factor since it is more challenging to maintain the anaerobic condition; incomplete anode burial and insertion is one of the most common cause for failures of MFCs deployed on the field. Moreover, large-size MFCs are not practical since

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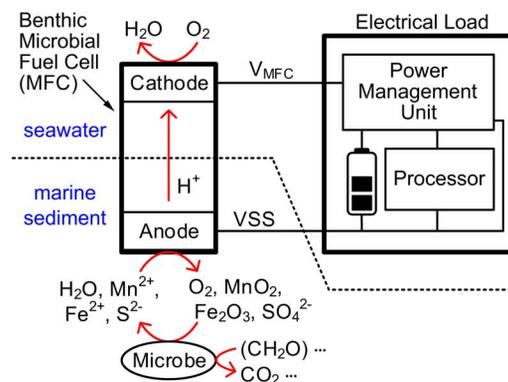


Fig. 1. Sensor system operating off a benthic microbial fuel cell.

human divers and/or sophisticated deployment technologies are required to bury them in the ocean floor.

In contrast, centimeter-scale MFCs can take advantage of easy burial and convenient deployment with lower failure rates. MFCs in this scale have been successfully deployed and tested [3], [4], but could only provide 1–100 μW of power, which is not suitable for continuous operation of most commercial electronics. For practical usage, energy harvested from such low-power source should be stored in a battery and high-power circuits should be duty-cycled to meet the energy budget provided by the energy source.

However, harvesting energy from an MFC for battery-operated system is a nontrivial challenge due to the voltage difference between the MFC (typically 0.4–0.8 V) and a commercially available battery (>1.5 V). Connecting the MFCs in series is not a viable option since MFCs operate as an open system in the marine environment. Therefore, the following aspects should be considered for energy harvesting from MFCs: 1) a DC/DC up-converting harvester is required to bridge between the MFC and a battery, 2) the conversion ratio of the harvester should be reconfigurable since the input voltage is changing according to the environment (i.e. amount of active bacteria in sediment), and 3) all these features should be implemented within a power budget suitable for < μW-level harvesting.

Energy harvesting circuits for large-scale MFCs that generates mW-level power have been previously reported in literature [5]–[10]. However, the energy harvesting circuits alone consume at least 10 s of μWs (20 μW in [6]) in these systems,

which is not acceptable for the MFCs generating μW s of power or less.

In this paper, a self-sustainable sensing system is proposed for an MFC in small scale (21.3 cm^2) with low power ($5.4 \mu\text{W}$). Low power consumption in sleep mode (11 nW) and reconfigurable PMU allows adjustment of the system active time according to its available power.

The paper is organized as follows. Section II describes the system overview for the oceanic sensing platform. Section III discusses the switched-capacitor (SC) DC/DC converter designed in this work. Section IV shows the measurement results and the paper is concluded in Section V.

II. SYSTEM OVERVIEW

A. Small-Scale Microbial Fuel Cell (MFC)

A micro-MFC was set up for experiments in the laboratory environment inside an aquarium ($45 \times 90 \text{ cm}^2$). Sediment from the Marine Corps Recruiting Depot marina in San Diego, CA, USA, was collected during low tide. The aquarium was filled with the 15 cm-deep sediment. 25 cm of salt water above the sediment was continuously exchanged with surface water pumped from the San Diego Bay.

The MFC is comprised of a graphite rod anode and a carbon fiber brush cathode. The graphite rod anode was 1.9 cm in diameter. The anode length of 7.5 cm with a respective surface area of 21.3 cm^2 was evaluated as anodes for a MFC supplying power to the electronics. Electrical contacts for the anode were created by drilling a small hole (0.08 cm) located 1.3 cm from one end, through which titanium wire was threaded through the hole and tightly twisted for secure contact. The carbon-fiber brushes used as a cathode for the MFC has length of 12 cm with diameter of 12 cm and consisted of carbon fiber fixed in a titanium wire stem. The cathode was oversized to ensure that the device would be anode limited, in order to observe the limitations of 21.3 cm^2 anodes.

Initially, the anode was pushed into the sediment vertically with the titanium wire oriented towards the top of the sediment to emulate the deployment of a dart type MFC. The cathode was hung vertically in the overlying water. In order to condition the MFC for use with the electronics, it was operated under varying conditions to maintain a cell voltage greater than 0.5 V. It was left under open circuit conditions for 24 hours followed by sequential loading of a passive resistor. After 12 days, the MFC was maintaining a voltage ranging from 0.6–0.7 V.

B. Electronics

A custom ultra-low power chip (CTRL chip) was designed to harvest energy from benthic MFCs and perform processor operations. Fabricated in a commercial 180 nm CMOS technology, this chip is part of a 1.0 mm^3 die-stacked sensor node system [11]. As the main processing and housekeeping chip of the system, the CTRL chip features an ARM Cortex-M0 processor, 3 kB of SRAM, I²C interface for external sensor components, sleep controller, optical programming interface, power-on reset detector (POR), brown-out detector (BOD) and a power-management unit (PMU) (Fig. 2). Various leakage power reduction techniques limit the overall chip power consumption

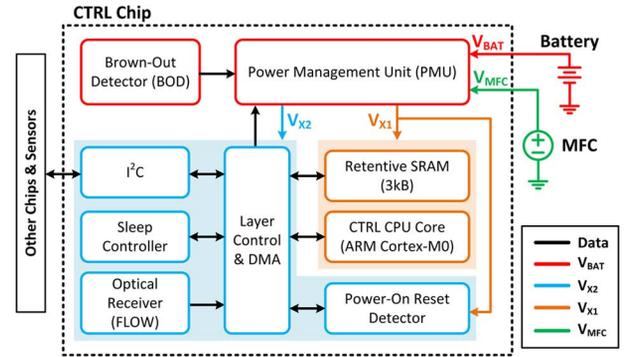


Fig. 2. CTRL chip block diagram and external connections.

to only 11 nW in sleep mode, making it ideal for sensor applications with a duty cycled usage scenario.

The processor core operating at 400 kHz can configure the sleep controller to schedule sleep/wakeup cycles of the whole system. In sleep mode, I²C controller, layer controller, and the core are power-gated. The SRAM is used for storing both instructions and data. Since the custom 8-T SRAM cell has an ultra-low leakage power [12], the SRAM does not need to be power-gated. Hence, the custom SRAM retains its states as long as 0.7 V supply is present, avoiding the need of a non-volatile memory.

The main data interface of the CTRL chip is a modified I²C protocol [11], which is compatible with the standard I²C protocol. The core can generate I²C messages through the layer controller to talk to other off-chip I²C-compatible components as memory-mapped I/O operations. I²C is also used to load the program instructions onto the memory. When wired I²C connection is impractical, the optical receiver can be used to program the chip with light. This option can be attractive for underwater operations, in which exposed wired connection can lead to corrosion or other physical damage.

As the energy storage device, a rechargeable thin-film Li-ion battery with nominal voltage of 4.0 V is chosen. High battery voltage increases storage capacity of the battery which allows the sensor to operate longer during times of low or none harvesting. Also, Li-ion battery can be made in a small form factor (110 mm^3). Compared to super capacitors, a battery has a lower self-discharge rate (1% per year) and a faster voltage ramp up during initial charging, which allows quick initial system boot up.

The PMU is responsible for harvesting energy from the MFC (V_{MFC}) and charging the battery. It also converts a nominal battery voltage of 4.0 V to V_{X1} and V_{X2} (nominally 1/6 and 2/6 of V_{BAT} , 0.67 V and 1.33 V, respectively), that are used to power different components of the chip [13]. Fig. 3 shows PMU state transitions in response to battery voltage change. When the battery voltage stabilizes above 3.4 V, the PMU enters Operational Mode and the system is activated. During Operational Mode, the system switches between Sleep and Active Modes based on the user-defined program.

The BOD continuously monitors the battery voltage, and when it detects that the battery voltage has dropped below 3.1 V, it signals PMU to enter Deep Sleep Mode to prevent the battery from over-discharging. During Deep Sleep Mode, all supply voltages are turned off and the system only consumes 185 pW. Since SRAM is also powered down in this mode,

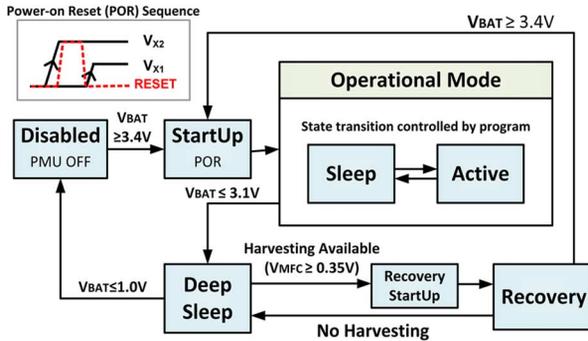


Fig. 3. State diagram of PMU depending on harvesting conditions and battery voltage.

its content is lost and the chip needs to be re-programmed. Harvested energy availability is monitored while the system is in Deep Sleep Mode. The system enters Recovery Mode when sufficient power is available. In this mode, the battery is recharged from the harvesting source until the battery voltage increases above 3.4 V. At this point, the system returns to its normal Operational Mode.

III. SWITCHED-CAPACITOR DC/DC CONVERTER

In this work, a switched-capacitor (SC) DC/DC converter is designed as an energy harvester and a step-down converter in the PMU. As an energy harvester, it transfers energy from a benthic MFC (~ 0.4 V) to a lithium thin-film battery (~ 4.0 V). On the other hand, as a step-down converter, it delivers power from the battery to loading circuits such as a processor and memory (0.67 V/ 1.33 V).

Boost and buck converters with off-chip inductors are one of the common solutions for such voltage up/down conversion. However, inductive converters suffer from low efficiency for high conversion ratio and low output current [14]. Therefore, a SC converter is selected for higher efficiency at high conversion ratio ($6\times$ – $10\times$) and low output current (down to nA). In addition, on-chip capacitors eliminate the need for off-chip components, allowing easier system integration and manufacturing cost reduction.

One of the key requirements of the converter is maintaining reasonable step-down conversion efficiency for a wide range of output current. This is because the output current can vary from several nA in sleep mode to tens of μA during active mode. Such duty-cycled operation is a key feature of ultra-low power sensing systems to lower average power consumption [11], [12]. Another key requirement is the ability to harvest energy from a harvesting source with wide range of input current. Harvested power from a benthic MFC can vary as environmental conditions change. Anode contact area to sediment, amount of active bacteria in sediment, and surface condition of cathode affect the amount of available power from MFC and change from time to time.

Therefore, SC DC/DC converters that can address these two key requirements are designed for the MFC-powered sensing platform. The SC converter topology used in this work is identical to the converter structure presented in [13]. However, the converter in [13] was not optimized for power conversion in extremely low, nA-level current where efficiency loss at gate driver and clock generator become significant. Therefore, details on lower power gate driver and clock generator scheme

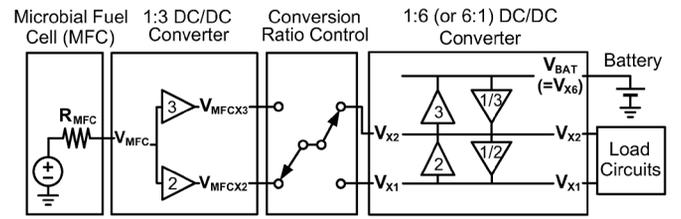


Fig. 4. Block diagram of the switched-capacitor DC/DC converters in the sensing platform.

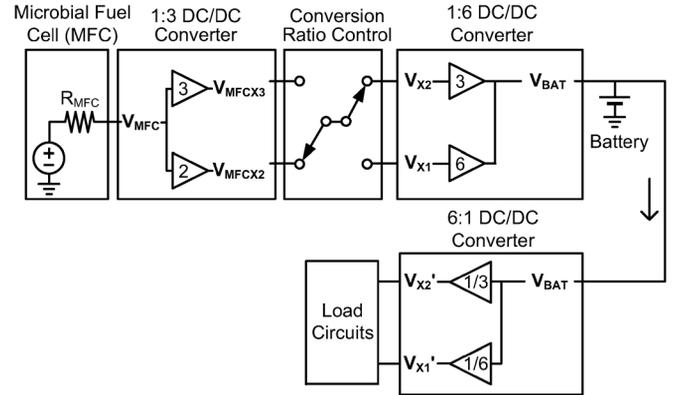


Fig. 5. Block diagram using separate 1:6 and 6:1 converters.

as well as detailed design consideration and analysis on the topology will be discussed in this section.

A. Converter Design

Fig. 4 shows a block diagram of the SC DC/DC converter. For energy harvesting, the 1:3 DC/DC converter generates $2\times$ and $3\times$ voltages (V_{MFCX2} and V_{MFCX3}) from the MFC voltage (V_{MFC}), and a 1:6 DC/DC converter transfers charge from V_{MFCX2} or V_{MFCX3} to battery (V_{BAT}). The voltage conversion ratio from the MFC to the battery is determined by the connection between V_{MFCX2}/V_{MFCX3} and V_{X1}/V_{X2} , allowing conversion ratios of 1:9, 1:12, and 1:18.

Also, the 1:6 DC/DC converter is used as a 6:1 step-down converter to deliver power from the battery to V_{X1} and V_{X2} for low-voltage and low-power operation of analog and digital circuits in the sensing system. Such configuration allows efficient use of capacitors in the converters by utilizing a 6:1 down-converter as a 1:6 up-converter, eliminating the need for two separate up-conversion and down-conversion networks as shown in Fig. 5.

Fig. 6 shows the circuit diagram of the 1:6 SC DC/DC converter. A ladder topology is chosen to provide multiple of output voltages in step-down conversion. Other SC-based converter topologies such as Dickson and series-parallel cannot easily offer more than one stepped-down output voltages. The bottom plates of flying capacitors (C_{FLY}) are connected together in order to store more charges, thereby decreasing output resistance [15].

For the capacitors, metal-insulator-metal (MIM) capacitors are used since logic circuits such as the processor and memory cells can be placed underneath to maximize area utilization. In this converter, the voltage assigned to capacitors is not limited by the maximum allowable voltage for the MIM capacitor since it is larger than the possible maximum voltage, battery voltage.

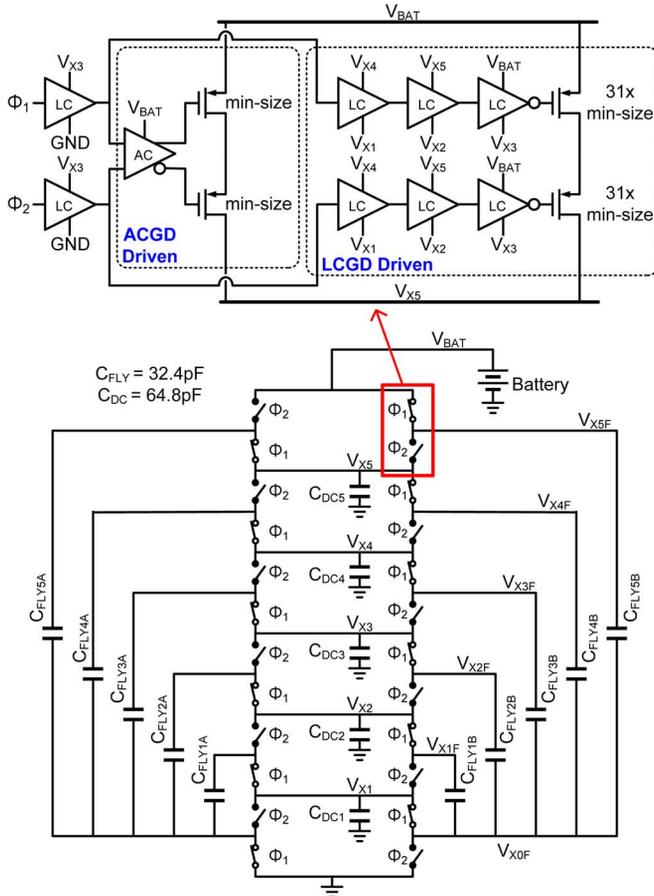


Fig. 6. Circuit diagram of the 1:6 DC/DC converter.

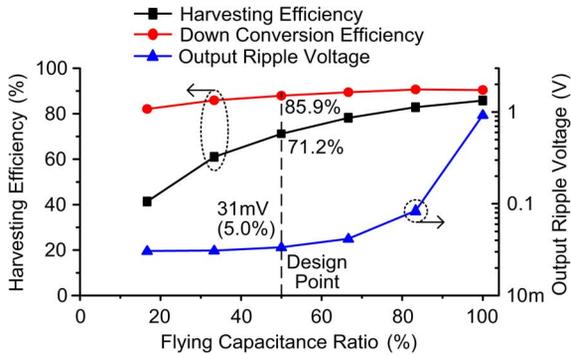


Fig. 7. Conversion efficiency and output ripple voltage over different ratio of flying and decoupling capacitance for the fixed total capacitance.

The converters are implemented in 2 interleaved phases to achieve low ripple voltage at the outputs. By using complementary switch control signals (Φ_1, Φ_2), the 2 phase converter can be implemented with minimal overhead.

Decoupling capacitors are also employed for smaller ripple at outputs. However, given the fixed total area of capacitors (0.9 nF at 0.6 mm²), increasing decoupling capacitance can degrade energy harvesting efficiency since flying capacitance used for transferring charge from harvesting source to battery is decreased. Fig. 7 clearly shows this tradeoff between conversion efficiency and output ripple in simulations: with larger flying capacitance, efficiency improves at the cost of larger ripple. To keep both efficiency and ripple at reasonable level, 50% of total

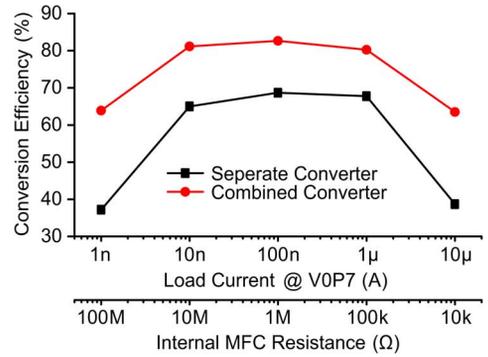


Fig. 8. Comparison of the combined and separate converters.

capacitance (324 pF out of 648 pF) is assigned as decoupling capacitors in the proposed converter.

The proposed topology combines a step-down converter and a step-up converter, which can benefit from direct charge transfer paths from the MFC to load circuits without charge storage in the battery as shown in Fig. 4. Whenever a charge is transferred through a switch, there is conduction loss due to voltage drop across the switch. With separate step-up/step-down conversion as shown in Fig. 5, charges have to be transferred all the way to the battery through the step-up converter and then to load circuits through the step-down converter, which is through up to 26 switches. In the combined topology, charges are directly delivered to load circuits from the MFC through as few as 6 switches. The difference in the number of switches that charges are transferred through impacts the amount of conduction loss and hence harvesting efficiency. Fig. 8 compares the simulated conversion efficiency of combined (Fig. 4) and separate converters (Fig. 5). In these simulations, the MFCs with smaller input resistance are assigned for larger output current. The proposed combined converter shows >13% efficiency increase compared to the separated converter.

One drawback of this topology is that it is difficult to optimize both step-down conversion and energy harvesting operations simultaneously. There can be an optimal switching frequency for step-down conversion where down conversion efficiency is the highest for a given output current. On the other hand, there can be another optimal frequency for energy harvesting where the highest harvesting efficiency can be achieved for a given harvesting condition. These two optimal frequencies do not necessarily match, hence both operations cannot be optimized simultaneously. However, it is clear which operation should be optimized in each operation mode of the sensing system. In active mode, output power consumption (40 μW) is typically much higher than harvested power (5 μW), so more energy is consumed from battery rather than harvested from MFC. Therefore, operation at optimal step-down conversion efficiency is desired. In contrast, during sleep mode, standby power of the system (11 nW) is typically lower than harvested power. Therefore, the switching frequency should be set for the optimal harvesting efficiency. Moreover, most of the energy is harvested in sleep mode since the proposed sensor system spends most time in sleep modes (8 min per cycle) and wakes up for very short time (1 s per cycle). Therefore, optimization of energy harvesting in sleep mode is a critical factor for achieving energy-autonomous operation.

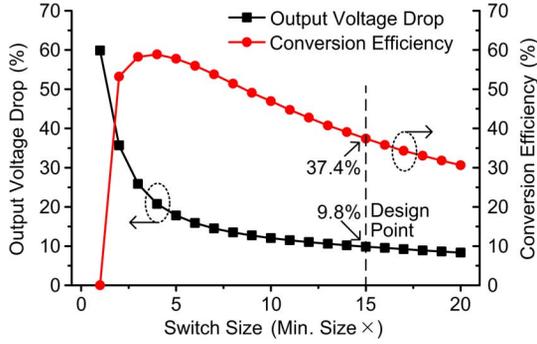


Fig. 9. Output voltage drop and step-down conversion efficiency with different switch sizes.

When there is non-zero output current for a SC DC/DC converter, capacitor charging/discharging losses and resistive conduction losses incurs voltage drop at the output. This voltage drop can be represented as follows:

$$v_{drop} = i_{out}R_{OUT} \approx i_{out}\sqrt{\left(\frac{k_1}{C_{fly}f_{sw}}\right)^2 + (k_2R_{on})^2} \quad (1)$$

where R_{OUT} is output impedance due to the losses, k_1 and k_2 are constants depending on the converter topology, and R_{ON} is switch on-resistance [14], [15]. This equation clearly shows that the switching frequency (f_{sw}) should be increased for larger output current (i_{out}) to regulate output voltage drop with a given flying capacitor value and topology until resistive conduction losses become dominant. Here, MIM capacitors are used for maximum area utilization to maximize C_{fly} so that f_{sw} could be minimized to reduce switching loss. Size of each flying capacitor is 32.4 pF.

Since the input or output power can vary significantly in this system, two different switch sizes are used to achieve efficient conversion. First, for low input and output power, the minimum-size transistors are used to minimize switching loss. As will be seen in Fig. 16, up to 3 MHz for $3.6 \mu\text{W}$, the converter efficiency is not limited by conduction loss from the small switches. For high input and output power, faster switching frequency is used to suppress capacitor charging and discharging losses ($k_1/C_{fly}f_{sw}$) according to (1). In addition, larger switches are also necessary for less resistive conduction losses (k_2/R_{on}) to decrease the total R_{OUT} .

Fig. 9 shows the output voltage drop and step-down conversion efficiency with different switch sizes for a given output power of $40 \mu\text{W}$, which is the typical output power of proposed system in active mode. Switching frequency is fixed to 4 MHz in this simulation. With larger switches, conduction loss decreases, and switching loss increases due to larger parasitic capacitance, resulting in lower conversion efficiency. Therefore, NMOS transistors with $15\times$ min-size ($31\times$ for PMOS) are utilized as switches in high power operation to limit the output voltage drop to 10%.

Additional sizes can be added for switches to obtain optimal efficiency at multiple input/output conditions. However, parasitic capacitance (C_{db} and C_{sb}) of the unused transistors causes switching loss, which can decrease conversion efficiency in low-power condition.

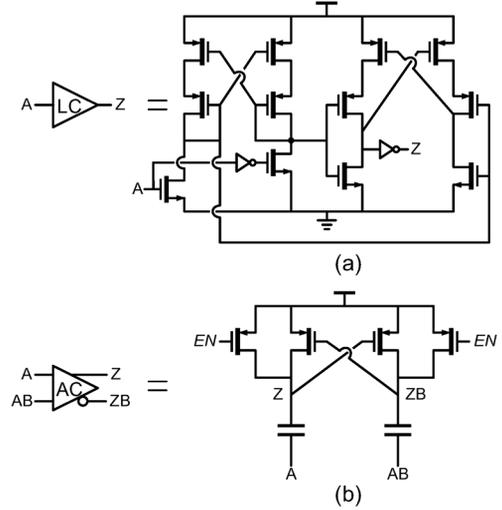


Fig. 10. Gate drivers (a) level-converter-based gate driver (LCGD). (b) AC-coupling-based gate driver (ACGD).

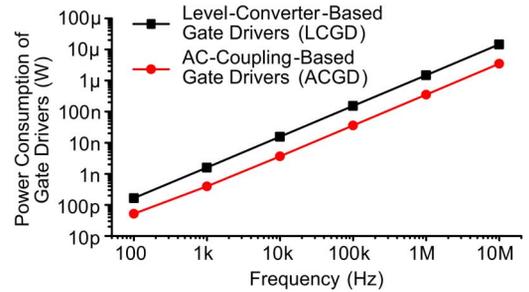


Fig. 11. Switching power consumption from gate drivers.

B. Gate Drivers

The SC DC/DC converter in previous design [13] utilizes level-converter-based gate drivers (LCGD) as shown in Fig. 10(a). The LCGD is based on the level converter in [16], which is typically used for interfacing digital circuits in two different voltage domains. Due to robust operation as a digital logic gate, the output of LCGD is guaranteed to have full supply voltage swing. This property makes the LCGD an attractive option for handling large input or output current.

However, switching overhead for LCGD is significant since it is a ratioed logic—whenever the inputs switch, the pull-down current of the NMOS has to overcome the pull-up current of the PMOS in the first stage. For improving efficiency with low input or output power, an AC-coupling-based gate drivers (ACGD) [17] is introduced as shown in Fig. 10(b). The ACGD scheme relies on AC coupling of inputs to efficiently generate gate driving signals without the ratioed logic. In simulation, switching ACGD for a cycle consumes 12.5 fJ whereas LCGD requires 202 fJ. Fig. 11 shows power consumed for gate driving when the 1:6 DC/DC converter is constructed only with ACGDs or LCGDs assuming the driven gates are identically sized. It shows ACGD consumes $\sim 4\times$ lower power than LCGD.

Although ACGD can efficiently generate gate driving signals, its driving capability is limited compared to the LCGD due to its coupling nature. Fig. 12 shows gate driving voltage for driving minimum-size transistors as function of coupling capacitance and switching frequency with ACGD. Reasonable coupling capacitance value is required to guarantee strong gate

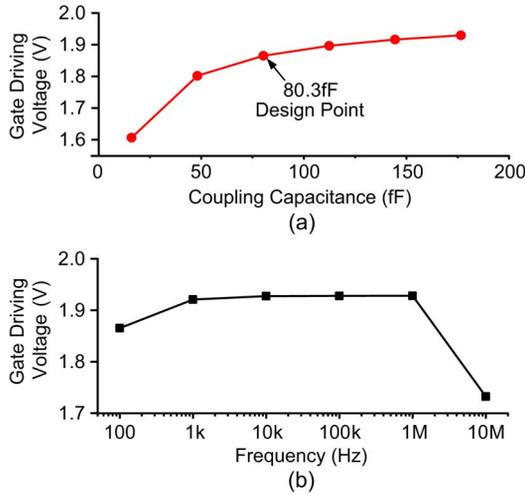


Fig. 12. Gate driving voltage of the ACGD as function of (a) coupling capacitance; (b) switching frequency.

driving voltage. To keep coupling capacitor value small for efficient operation, minimum-sized switch is paired with ACGD. In the final 1:6 DC/DC converter design, ACGDs with minimum-sized switches and LCGDs with $31\times$ -size switches are connected in parallel as shown in Fig. 6 so that efficient low-power conversion is achieved with ACGDs and high-power conversion is obtained with LCGDs.

C. Clock Generator

The amount of charge that can be transferred through the switched capacitor converter is proportional to the capacitance of flying capacitors and their switching frequency. Since the capacitance value is fixed in design time, the switching frequency needs to be adjusted to accommodate variation on input or output power during operation. Therefore, a variable-frequency clock generator is a key element for efficient operation. However, designing an efficient clock generator for the converter transferring from nW to μ W of power is a non-trivial challenge since it has to meet following conditions: 1) a wide range of frequency should be covered; 2) power consumption should be scaled with the output frequency especially at low frequency to maintain reasonable efficiency at nW order; 3) output should have full-voltage swing (2 V) to avoid efficiency degradation with ACGD.

A current-starved ring oscillator is a typical solution for energy-efficient broad-range clock generation. The output frequency is directly proportional to bias current controlled by starving transistors. Hence, the power consumption of the oscillator is scaled with the output frequency. However, the total power consumption of the clock generator suffers from short-circuit current through an output buffer, typically series of inverters, in low frequency regime where voltage transition slew is very low due to extremely starved driving current. As a result, power consumption is not scaled below certain frequency, as shown in Fig. 13. Furthermore, generating bias voltages of starving transistors for very low frequency is challenging since it typically operates transistors in deep sub-threshold mode where transistors are very susceptible to

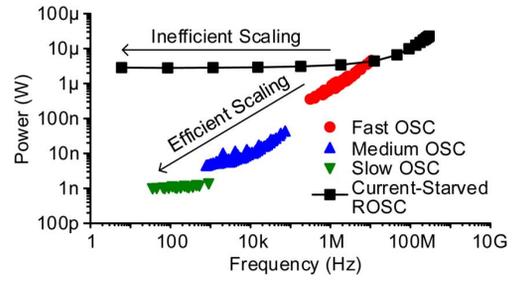


Fig. 13. Power consumption of clock generators with various types of oscillators.

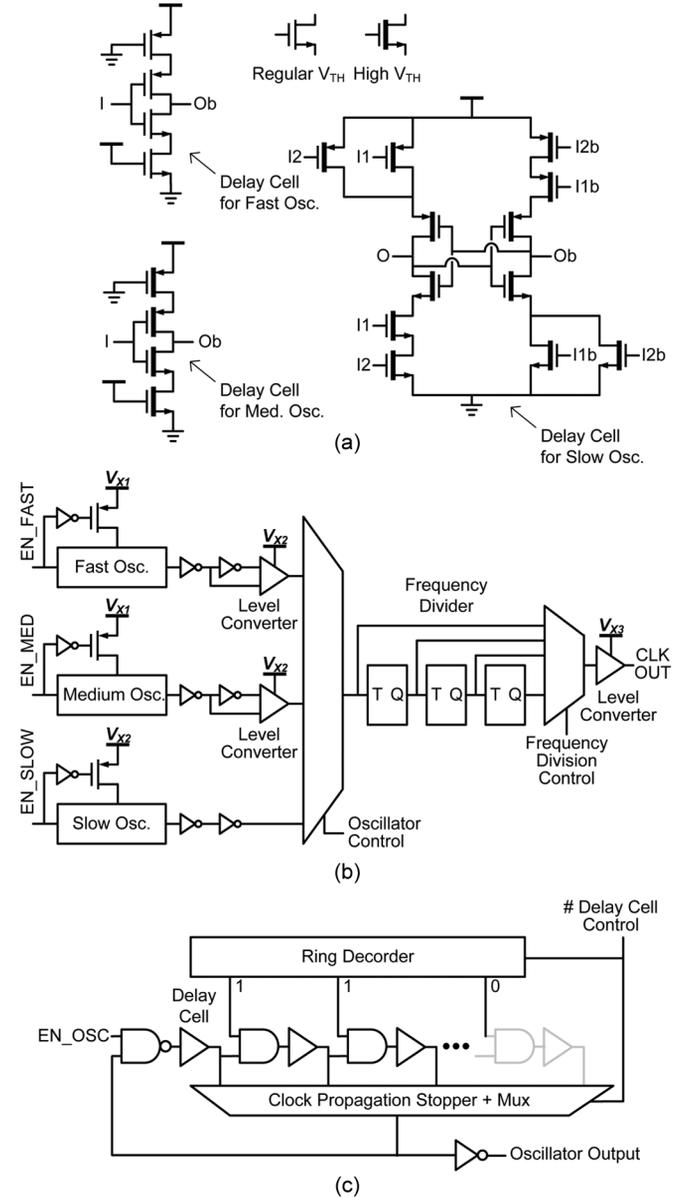


Fig. 14. Wide-frequency-range clock generator. (a) Delay cells. (b) Clock generator block diagram. (c) Proposed oscillator structure.

variation. Clearly, new oscillator topology is required for low output or harvested power.

For energy-efficient slow clock generation, an oscillator can be operated at low voltage (V_{X1}) to reduce dynamic energy consumption. With such low supply voltage, starving current with

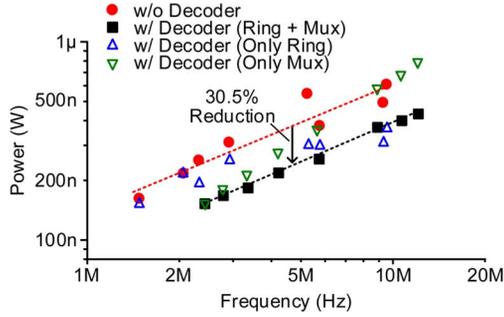


Fig. 15. Power consumption of oscillators with power reduction decoders.

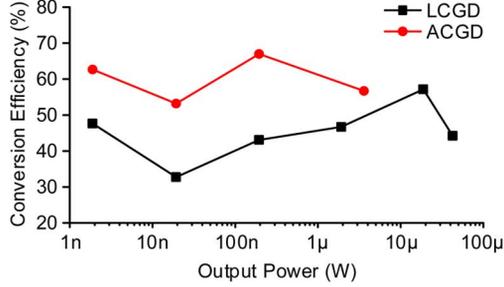


Fig. 16. Simulated conversion efficiency of the designed 6:1 step-down converter.

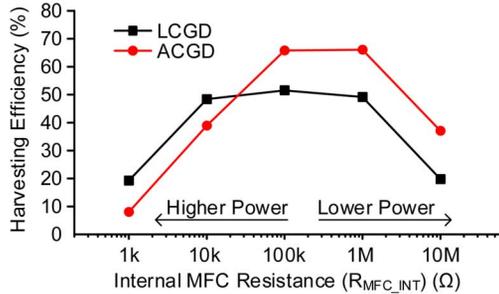


Fig. 17. Simulated harvesting efficiency of the designed energy harvester.

partially off header/footers is unreliable. Instead, starving current with narrow and long always-on transistors as shown in Fig. 14(a) can be a reliable solution since the full V_{GS} swing makes it less susceptible to variations. The output of the oscillator is then buffered with series of inverters [Fig. 14(b)]. Buffering at V1 domain can suppress short-circuit current if supply voltage is lower than sum of threshold voltages of NMOS (V_{THN}) and PMOS (V_{THP}). The buffered output can be level-converted to the desired voltage level (V_{X2} then V_{X3}).

By employing two device flavors (regular and high V_{TH}) for current-starved delay cells, efficient frequency scaling could be achieved down to 800 Hz as shown in Fig. 13. However, current starving approach cannot achieve efficient scaling below this point. For slower frequency, leakage-based oscillators [18] are selected to efficiently generate slow clocks: their delay cell's output voltages rapidly escape the voltage range between V_{THN} and $V_{DD} - V_{THP}$, where short-circuit current can occur.

A clock generator that combines the three ring oscillators is designed as shown in Fig. 14(b). The number of delay-cell stages can be controlled to tune frequency. For energy-efficient scaling of the clock generator down to nW power regime, unnecessary switching activities in the oscillator are suppressed. A ring decoder is added as shown in Fig. 14(c) and stops propagation of unnecessary switching activities to the next delay-cell stage and multiplexer inputs. Fig. 15 shows that it can reduce 30% of power consumption in the fast-type oscillator.

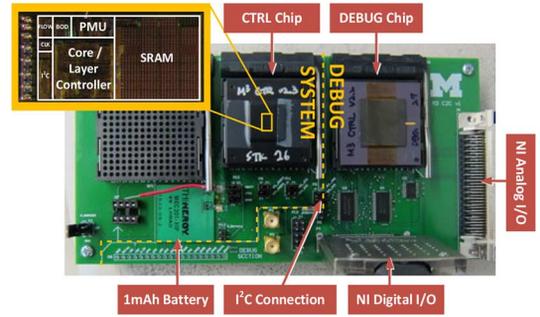


Fig. 18. PCB board used for integration testing and die photograph of CTRL chip. Dashed line indicates boundary between SYSTEM and DEBUG sections.

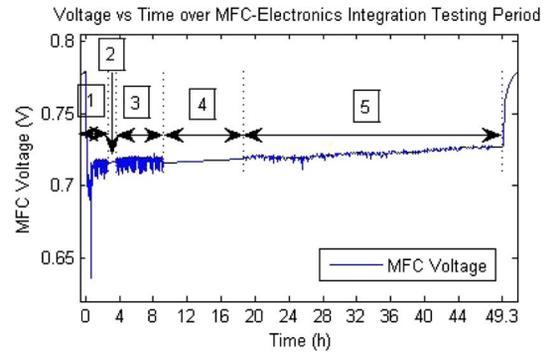


Fig. 19. MFC voltage versus time (in hours).

D. Simulated Performance

Fig. 16 shows simulated step-down conversion efficiency with two different types of gate drivers discussed in Section III-B. For clock generation, the clock generator discussed in Section III-C is used, and its power consumption is taken into account for converter efficiency calculation. For a given output power, the highest conversion efficiency is plotted with switching frequency control, allowing that the output voltage drop is limited to 10% of the no-load output voltage (0.67 V). The ACGD with minimum-sized switches exhibits higher efficiency compared to LCGD as expected. However, ACGD fails beyond $4 \mu\text{W}$ output power due to weak conduction of minimum-size converter switches. Larger converter switches driven by the LCGD can be used for $> 4 \mu\text{W}$ output power, resulting in reasonable converter efficiency of 40~60%.

Fig. 17 shows simulated energy harvesting efficiency with two different types of gate drivers. Since an energy harvester should consider efficiency of both an energy source and a step-up converter, the following definition is used for the harvesting efficiency [19]:

$$\text{Harvesting Efficiency (\%)} = \frac{P_{BAT}}{P_{S,MPP}}, \quad (2)$$

where P_{BAT} is power delivered to battery and $P_{S,MPP}$ is the maximum available power from the energy source. In this simulation, the conversion ratio of 1:9 is used (connecting V_{MFCX3} to V_{X2} in Fig. 4), and power overhead for clock generation is taken into account. For low harvested power ($R_{MFC_INT} > 20 \text{ k}\Omega$), higher efficiency could be achieved with ACGD due to its small switching overhead. However, LCGD performed better with high harvested power ($R_{MFC_INT} < 20 \text{ k}\Omega$) since conduction loss of small switches in ACGD become significant.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR WORKS

	This work	[5]	[6]	[7]	[8]	[9]	[10]
MFC anode size (cm ²)	21.3	691.2	1,829 [†]	265	2,000	100,000	N/A
MFC output power (W)	5.4 μ	1m	1.7m	5.8m [†]	2.4m [†]	150m	7.5m [†]
Energy harvester type	Capacitive	Capacitive & Inductive	Inductive	Inductive	Capacitive & Inductive	Inductive	Inductive
Circuit implementation	180nm CMOS	Discrete	Discrete	Discrete	Discrete	Discrete	Discrete
Harvested power (W)	1.52 μ	0.22m [†]	0.35m [†]	N/A	1.68m [†]	67.5m	5.5m [†]
Energy storage device	Rechargeable lithium-ion battery (4.0V, 1mAh)	Super cap. (2.2F)	Capacitor (N/A)	Super cap. (4F)	Super cap. (10F)	Super Cap. (58F)	Super cap. (1F)
Load components	Processor, Memory, Optical Receiver, etc.	Hydrophone	LED	Wireless temperature sensor	Wireless temperature sensor	Beacon or Unmanned underwater vehicle or hybrid sensor	Test resistor

[†] Calculated based on the data in the papers

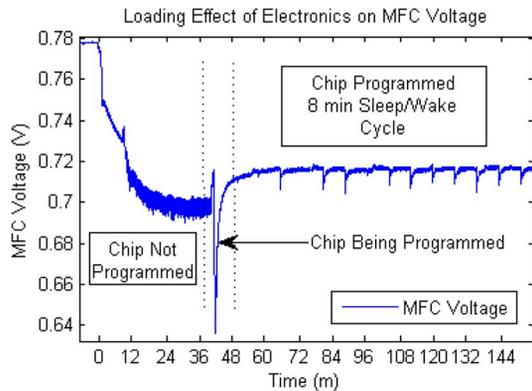


Fig. 20. The MFC voltage versus time (in minutes) during the early period of electronics integration, Region 1 of Fig. 19.

IV. EXPERIMENTAL RESULTS

A PCB board was designed for system integration testing with two sections: SYSTEM and DEBUG (Fig. 18) [20]. The SYSTEM portion was designed to mimic the die-stacked system in [11], by replacing the inter-layer bond-wire connections with PCB traces. It includes the CTRL chip, a commercial 4 V 1 mAh thin-film battery, and additional sockets for other sensing modalities such as pressure or temperature sensors. The DEBUG section of the board houses a DEBUG chip, which is a variant of the CTRL chip that has additional peripheral circuitry for debugging purposes. Its main role in this system is twofold: programming the CTRL chip and monitoring the I²C wires to observe the status of the CTRL chip. The only electrical connection between the DEBUG and CTRL chips are the two I²C wires and ground. Once the CTRL chip is programmed, the DEBUG section can be disconnected for field deployment of the system.

Fig. 19 shows the measured MFC voltage versus time over the 49.3 hour period, broken into five different regions. The MFC voltage was sampled at 2 samples per second in regions 1–4. Region 2 is a period of data acquisition failure that lasts for 1.5 hours. In Region 3 the data acquisition software is restarted and the sample rate continues to be 2 samples per second. Region 4 shows another data acquisition failure that lasts for 9.5 hours (overnight). In Region 5 the data acquisition software was restarted and the sample rate changed to 1 sample per 5 minutes to avoid further data acquisition failures. This region extends to the end of the long term experiment at hour 49.3, at which point the electronics are intentionally disconnected. The MFC voltage

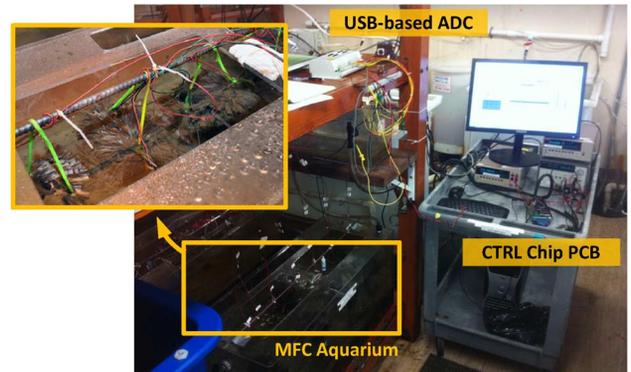


Fig. 21. Experimental setup of chip-on-mud system integration testing.

then begins to approach the open circuit voltage. This long term experiment was halted due to collaboration time constraints.

Fig. 20 shows Region 1 in more detail, showing the loading effect of CTRL chip's PMU on the MFC, with the voltage dropping from 0.78 V to 0.70 V. When the DEBUG chip is used to initially program the CTRL chip, large current is drawn by the I²C unit and layer controller, resulting in a further MFC voltage drop to 0.64 V. Upon completion of the initial programming, the chip goes into sleep mode and the MFC voltage rises to 0.72 V. Afterwards, voltage spikes begin to appear at uniform intervals, corresponding to the CTRL chip's duty cycle in which the chip wakes up every 8 minutes, executes the program for 1–2 seconds, and then goes back to sleep.

The voltage of the battery at the beginning of the long term experiment was 4.0908 V. At the end of the experiment, the battery voltage was recorded at 4.0932 V. This increase in energy stored in the battery over the course of the experiment confirms the capability of MFCs as a power source to keep the integrated system self-sustainable. The average current generated by the MFC during the integration period was 7.5 μ A. With the average MFC voltage being 0.72 V during integration, this corresponds to 5.4 μ W of power generation. The harvested current into the battery from the PMU harvesting circuit was 380 nA during sleep mode. With a usage scenario of waking up every 10 minutes for 10 ms to retrieve data from a sensor and storing it, the battery can supply 20 mA of current during the active mode without losing net energy. Fig. 21 shows the experimental setup in a wet laboratory.

Table I shows summary of this work and comparison with the other prior works powered by MFCs. The proposed system was

powered by the smallest MFC, whose anode is $12.4\times$ smaller and output power $185\times$ smaller than other prior works. To implement the self-sustainable sensor platform with such a small MFC, the SC-based harvester was designed as an integrated circuit. The proposed system was the first MFC-powered system with rechargeable battery and voltage level monitoring. The system was also equipped with a processor and memory with I²C interface which allows it to be potentially used as generic platform and expanded with various sensing modalities.

V. CONCLUSION

The proposed system-on-mud platform offers perpetual oceanic sensing solution thanks to energy harvesting from micro-MFCs and ultra-low leakage standby mode. The switched capacitor DC/DC converter in this system enables to cover a wide range of input and output power from a variety of environment and load condition. In a long-term experiment, the energy autonomous operation of micro-MFC powered system is demonstrated.

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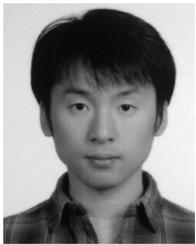


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