Digitally Controlled Leakage-Based Oscillator and Fast Relocking MDLL for Ultra Low Power Sensor Platform

Dong-Woo Jee, *Member, IEEE*, Dennis Sylvester, *Fellow, IEEE*, David Blaauw, *Fellow, IEEE*, and Jae-Yoon Sim, *Senior Member, IEEE*

***Abstract*—This paper presents an all-digital multiplying delay-locked loop (MDLL) with a leakage-based oscillator for ultra-low-power sensor platforms. The proposed digital control of channel leakage current achieved ultra-low-power consumption in frequency generation with a fine resolution. The leakage based oscillator was modeled as an RC-based oscillator, analyzed, and the analyses were verified by simulation. The proposed oscillator was applied to the MDLL with a fast frequency relocking scheme which adaptively performs an optimal lock process according to the amount of frequency drift during the sleep state. The MDLL was implemented in 65 nm CMOS and consumed 423 nW for 3.2 MHz generation, and had an energy efficiency FoM of 0.132 μW/MHz.**

***Index Terms*—Clock multiplier, fast lock-time, leakage current, multiplying delay-locked loop, oscillator, phase noise, sensor platform, ultra-low-power.**

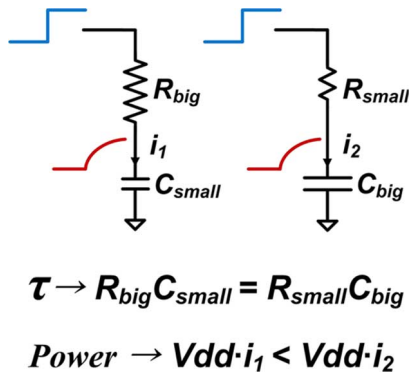

Fig. 1. RC combinations for the same time constant with different power consumption.

I. Introduction

POWER consumption has been a key performance metric in the design of ultra-low-power sensor platforms. Along with reduction of the supply voltage, design of circuit schemes that support extensive intermittent operation has been the most effective way to achieve low-power consumption [1]. To realize various duty-cycling scenarios for energy-optimal operation, the system needs to employ several clock sources that have different frequency ranges, ranging from several hertz for the internal timer to several gigahertz for RF transceivers.

Sensor platforms are turned off in most of the time with the minimum standby power dissipation and turned on by a wake-up control from an internal timer [2], [3]. The timer runs all the time and dominates the total standby power. When the system wakes up, a clock in the kilohertz range starts to run and becomes the global system clock for normal operation [4]–[7]. The system often requires high speed data transmission or intensive signal processing [8]. For this purpose, higher frequency clock in the megahertz range can be used. For wireless communication, a gigahertz clock source [9], [10] for RF modulation is turned on for a short period of time.

A common approach to generate various clock frequencies is to use multiple internal oscillators. However, the frequency of a free-running oscillator is highly sensitive to PVT variations, so significant design efforts with feedback control and post-fabrication trimming are required for each oscillator. In addition, the use of multiple external crystals is generally not adopted due to limited form-factors and increased cost. Therefore, clock multiplication from one clean reference is preferred for generating various higher frequencies.

The energy efficiency of oscillator is the most important factor in the design of clock multiplier, e.g., multiplying DLL (MDLL) or PLL, since the oscillator dominates the power consumption. For a given target frequency, it is desired to have larger resistance and smaller capacitance to minimize the charging current while maintaining the same time constant (Fig. 1). A typical RC product with a device output resistance and the minimum capacitance given by device parasitic only fits into the gigahertz range. Therefore, it is easier to obtain better energy efficiency (W/Hz) in the generation of RF frequency in the gigahertz range. The benefits of small parasitic capacitance with scaled technology also give the overall trend of better energy efficiency in higher frequency generation. However, generation of low frequency (<10 MHz) requires an

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D.-W. Jee is with the Department of Electrical and Computer Engineering, Ajou University, Suwon 443-649, Korea (e-mail: dwjee@ajou.ac.kr).

D. Sylvester and D. Blaauw are with the University of Michigan, Ann Arbor, MI 48109 USA.

J.-Y. Sim is with the Department of Electrical Engineering, POSTECH, Pohang 790-784, Korea (e-mail: jysim@postech.ac.kr).

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additional capacitance with an implementable resistance value, and increased capacitance degrades the energy efficiency.

Digital control scheme of oscillator frequency is another challenge in the design of an energy-efficient clock multiplier. To cover a wide frequency range with a fine resolution in all digital way, a large number of delay stages (Fig. 2(a)) or controllable extra capacitance (Fig. 2(b)) is required. But both techniques eventually degrade the energy efficiency. An alternative approach that uses a conventional current-starved scheme (Fig. 2(c)) dissipates extra DC biasing current. In addition, a large device size in the current mirror that conducts small current causes a huge parasitic capacitance, resulting in an increased dynamic power consumption and a long settling time during intermittent operation of a sensor platform.

This paper presents an all-digital MDLL with a digitally controlled leakage-based oscillator (DCLO) for energy efficient generation of clock frequencies in the megahertz range [11]. By exploiting device leakage current to obtain large effective resistance, the proposed MDLL generates 3.2 MHz with 423 nW power consumption, leading to an energy efficiency of 0.132 μW/MHz. An adaptive relocking scheme to support the intermittent operation is also implemented. Depending on the amount of frequency drift during the sleep period, the MDLL adaptively tracks the target frequency after wake-up and optimizes power consumption with minimized settling time. This paper is organized as follows. Section II describes the proposed DCLO with modeling and analyses. Section III describes circuit details of the proposed MDLL and the fast relocking scheme. Section IV shows the chip implementation and the measurement results, and Section V concludes this work.

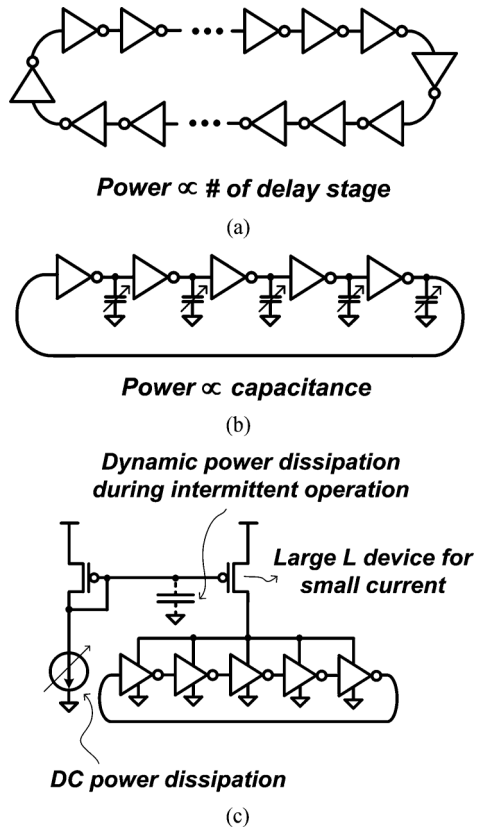

Fig. 2. Conventional oscillator control with (a) the number of delay stages, (b) variable load capacitance, and (c) starved inverter.

II. Digitally Controlled Leakage-Based Oscillator

A. Gate Leakage Based Oscillator vs. Proposed DCLO

The leakage current in deep submicron CMOS technology has been precisely characterized and modeled since it becomes an important player of the power dissipation in large-scale digital systems [12]. Thanks to such high-quality leakage modeling, circuit design technique using gate leakage current as a current source of an oscillator can be considered for the time keeping application in sensor SoC [13]. Although the gate leakage based oscillator has been successfully demonstrated in ultra-low-power design, the difficulty in controlling leakage current digitally limits its application to frequency multipliers which need a fine frequency tuning. As shown in Fig. 3, there can be three possible options to control the gate leakage. The first option is to tie the drain, source and bulk nodes to the ground, but reverse gate leakage current starts to flow as the capacitor-charging node builds up, so power is wasted due to the extra discharging current path. The second option is to make the source, drain and bulk as open nodes, but this option causes the gate capacitance of the device to become negligible and results in difficulty in predictive design of a total RC time constant. The third option is to use an extra voltage bias to avoid these problems, but the extra bias generation dissipates additional power.

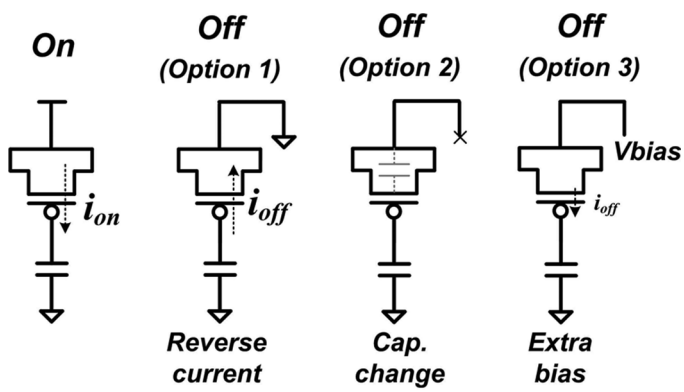

Fig. 3. Control schemes of gate leakage current.

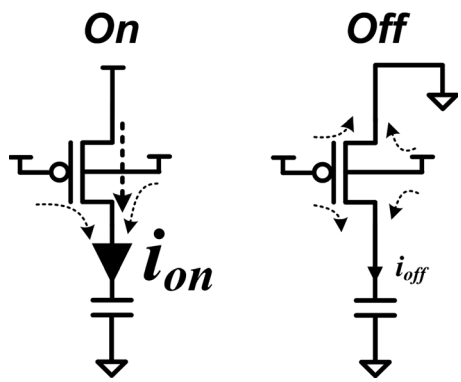

Fig. 4. Proposed leakage current control circuit for digitally controlled oscillator.

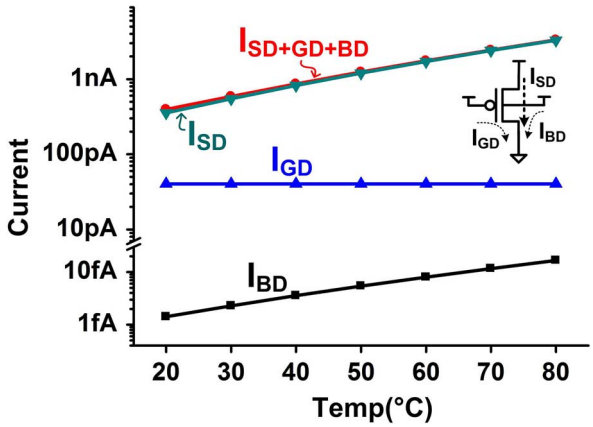

Fig. 5. Simulated leakage current component over temperature change.

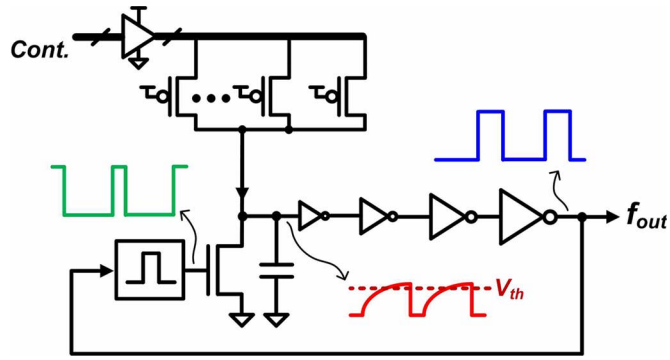

Fig. 6. Proposed digitally controlled leakage based oscillator.

Fig. 4 shows a new circuit technique to control the leakage current in all digital manner. If the source of the PMOS is connected to the supply, all device leakages from channel, gate, and junction flow into the capacitor. In contrast, if the source is connected to the ground, only small portions of the gate and junction leakage flow into the capacitor. Since the gate and bulk nodes are tied up to the supply, both V_{SG} and V_{DG} are negatively biased, so channel leakage current is negligible. Therefore, the leakage current can be controlled digitally by simply connecting the source of the PMOS to the power or the ground.

Fig. 5 shows simulated leakage current of a device in 0.45 V supply with the minimum width and length of 65 nm CMOS technology used in this work. The junction leakage (I_{BD}) is generally orders of magnitude smaller than all the other leakages, so it has no meaningful effect on total leakage current. Channel leakage (I_{SD}) is about 10 times larger than the gate leakage (I_{GD}), even with temperature variations. The temperature dependency is not a problem in clock multipliers since a low frequency drift due to temperature variation would be cleaned up by the loop dynamics of the clock multipliers. Therefore, the proposed scheme provides a large effective resistance for an energy-efficient clock generation with easy controllability.

Fig. 6 shows a simplified schematic of the proposed DCLO. Based on the general architecture of RC oscillator, the resistance is replaced by a PMOS array with source nodes tied to separate drivers for the controllability. A pulse generator connected to the NMOS produces a short pulse to reset the charging node. To maximize the energy efficiency, the charging capacitor is implemented with inherent device and routing parasitic only. This all-digital architecture achieves low power consumption not only with the supply voltage scaling, but also with no static power of bias generation.

B. Noise Modeling of DCLO Oscillator With RC Model

Since the purpose of using leakage current is to implement the function of a large effective resistance, the DCLO needs to be compared with RC oscillator. Fig. 7 compares transient responses of the proposed DCLO and RC oscillator. To get the same oscillation frequency of 2 MHz, with a charging capacitor of 50 fF extracted from the post layout extraction, required R was ~11 MΩ. As shown in the figure, DCLO showed very similar charging slope to that of the RC oscillator. The small difference was caused by the nonlinear effective resistance as the drain-to-source voltage changed.

For noise analysis, a simplified model of DCLO can be derived based on the transient response (Fig. 8). The charging node (B) can be modeled as an RC low-pass filter output with a resistance R_{AB} and a charging capacitance C_B. Since the source of the PMOS is tied to the supply (vdd), a step input is effectively applied to V_A at t_0 and stays at vdd until the next reset pulse at t_3. Since the reset pulse-width generated from the pulse generator is very small, the pulse-width of $V_A(t_3 - t_0)$ can be approximated as the period of oscillation, $1/f_{osc}$. The charging node voltage V_B then follows a typical RC response during $t_0 - t_3$ as

$$V_B = vdd(1 - e^{-t/R_{AB}C_B}) \tag{1}$$

The noise voltage V_{nB} at V_B is

$$V_{nB}^2 = kT/C_B \tag{2}$$

where k is Boltzmann's constant and T is the absolute temperature.

The first inverter stage acts as a comparator and dominates noise performance. To simplify the analysis, following assumptions have been made: 1) PMOS and NMOS of inverter have identical device parameters, and 2) the inverter logic threshold is $vdd/2$. When V_B passes the logic threshold $(vdd/2)$ at t_1, V_c starts to ramp down by discharging the output parasitic capacitance C_c. Considering V_B stays around $vdd/2$ during the period t_1–t_3, the first inverter stage can be modeled with small signal parameters of GmV_b and Ro where Gm is $gm_p + gm_n$, V_b is $V_B - vdd/2$ and Ro is $r_{op}//r_{on}$. At t_2, Vc falls below the threshold of the second inverter stage then further ramps down until the next reset event at t_3. The spectral density of the noise current in discharging C_c is

$$S_{i_{nC}} = 2 \cdot \mathrm{kT} \cdot \mathrm{n} \cdot \mathrm{Gm} \tag{3}$$

Note that both transistors operate in the subthreshold region, and only the thermal noise is considered because the flicker noise is negligible in the frequency band of interest (above a few tens of kilohertz). Since i_{nC}^2 is a white noise and is integrated over t_1–t_2 at capacitance C_C, the variance of the total noise voltage at V_C can be derived as [14]

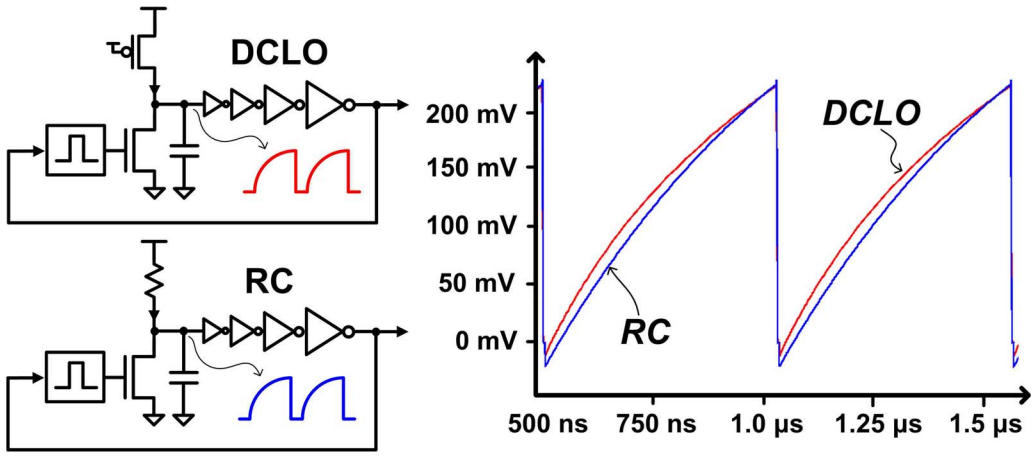

Fig. 7. Comparison of transient response of DCLO and RC oscillator.

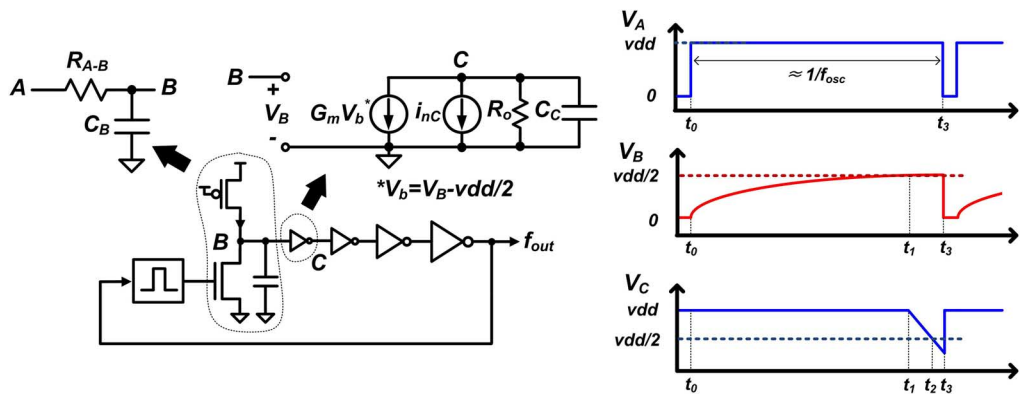

Fig. 8. Analysis model of DCLO as RC oscillator.

$$V_{nC}^2 = \frac{S_{inC}}{2 \cdot C_c^2} \cdot (\text{transition delay}) + kT/C_c = \frac{2 \cdot \mathrm{kT} \cdot \mathrm{n} \cdot \mathrm{Gm}}{2 \cdot C_c^2} \cdot (t_2 - t_1) + kT/C_c \quad (4)$$

The thermal noise term $(kT/\mathrm{C_C})$ is the initial noise stored on $\mathrm{C_C}$ at t_1. The total charge $\mathrm{Q_C}$ discharged from $\mathrm{C_C}$ during t_1–t_2 is

$$Q_c = \int_{t_1}^{t_2} Gm \cdot V_b(t)dt = C_c \cdot vdd/2 \quad (5)$$

Since we have assumed that both transistors have identical parameters ($gm_p = gm_n = gm, \mathrm{r_{op}} = \mathrm{r_{on}} = r_o$), the gain of the first inverter stage is $gm \cdot r_o$. Note that both transistors are biased with the same vdd/2 and mismatch between gm_p and gm_n is negligible, since gm of a subthreshold-biased transistor is $(\text{drain current})/\mathrm{n} \cdot Vt$, where n and Vt represent the subthreshold factor and the thermal voltage, respectively. Then, $\mathrm{V}_b(\mathrm{t}_2)$ can be obtained from

$$vdd/2 = gm \cdot r_o \cdot \mathrm{V}_b(\mathrm{t}_2) \quad (6)$$

Assuming a linear transition of $V_b(t)$ in $t1$–$t2$ and using $V_b(\mathrm{t}_1) = 0$ lead to the equation for $\mathrm{V}_b(\mathrm{t})$

$$\mathrm{V}_b(\mathrm{t}) = \frac{vdd/2gm \cdot r_o}{\mathrm{t}_2 - \mathrm{t}_1} \cdot (\mathrm{t} - \mathrm{t}_1) \quad (7)$$

Applying (7) to (5) derives an expression for $t_2 - t_1 = r_o \cdot C_c$ and (4) can be simplified to be

$$V_{nC}^2 = \frac{\mathrm{kT}}{C_c} \cdot (1 + n \cdot 2gm \cdot r_o) \quad (8)$$

The jitter of an oscillator can be estimated from the voltage noise. It has been well studied through several literatures [14]–[16]. The voltage noise at node B and C create variances σ_{t1}^2 and σ_{t2}^2, respectively in the transition time of the first and second inverter stages.

$$\sigma_{t1}^2 = V_{nB}^2 \times \left(\left| \frac{\partial V_B(t)}{\partial t} \right|_{t=t_1} \right)^{-2} \quad (9)$$

$$\sigma_{t2}^2 = V_{nC}^2 \times \left(\left| \frac{\partial V_C(t)}{\partial t} \right|_{t=t_2} \right)^{-2} \quad (10)$$

The noise contributions from subsequent inverter stages and the pulse generator can be neglected since their contributions to the jitter are scaled by time derivative and charging slopes are high enough. The transition slope of node B can be derived from (1) as

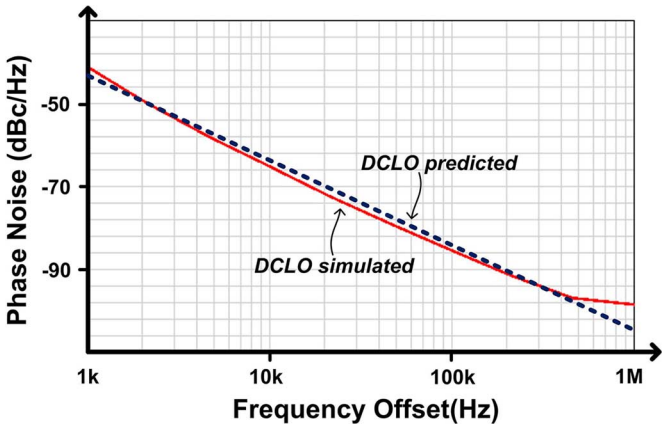

Fig. 9. Comparison of phase noise with calculated and simulated DCLO.

$$\left|\frac{\partial V_B(t)}{\partial t}\right|_{t=t_1} = \frac{vdd}{R_{AB}C_B} e^{-(t_1-t_0)/R_{AB}C_B} \tag{11}$$

For node C,

$$\left|\frac{\partial V_C(t)}{\partial t}\right|_{t=t_2} = \left|\frac{\partial V_B(t)}{\partial t}\right|_{t=t_2} \cdot gm \cdot r_o. \tag{12}$$

Assuming that the noise sources are independent and the differences between t_1, t_2 and t_3 are small enough compared with the oscillator period, the total variance of the period can be approximated as the sum of (9) and (10):

$$\Delta\sigma^2 = \left(\frac{vdd}{R_{AB}C_B} e^{-\frac{1/f_{\rm OSC}}{R_{AB}C_B}}\right)^{-2} \cdot \left(\frac{kT}{C_B} + \frac{\rm kT}{C_c} \cdot (1 + n \cdot 2gm \cdot r_o) \cdot (gm \cdot r_o)^{-2}\right) \tag{13}$$

The conversion from jitter to phase noise at an offset frequency of Δf is presented in [14]

$$L(\Delta f) = \frac{f_{\rm osc}^3 \cdot \Delta\sigma^2}{\Delta f^2} \tag{14}$$

Fig. 9 shows simulated and predicted (by 13 and 14) phase noise of the DCLO ($f_{\rm osc} = 2$ MHz), demonstrating the proposed modeling of leakage current with a large resistance provides a good prediction of the phase noise of the DCLO. The difference in slope at low frequency offset is due to $1/f$ noise which is not modeled in (13). The overall difference is $\leq$2 dB (10 k–100 k offset), because of the assumption of $t_{1-3} - t_0 \to 1/f_{\rm osc}$ in (13). Higher noise level near 1 MHz in simulation than predicted level is due to noise folding from harmonics.

Observation from (13) also reveals the charging capacitance and comparator noise are two critical factors; this is generally-accepted knowledge in the oscillator design. The effect of comparator noise can be reduced by using noise filtering techniques [17] or a high gain stage instead of a simple inverter in this work. Increasing the capacitance by reducing the resistance also improves the phase noise. In any case, there is a tradeoff between phase noise performance and power consumption. The tradeoff can be parameterized with the figure of merit for phase noise [16], [17]

$$\mathrm{FoM}_{PN}(\mathrm{dB}) = 10 \cdot \log\left(L(\Delta f) \cdot \mathrm{Power}_{\rm OSC}(\mathrm{mW}) \cdot \frac{\Delta f^2}{f_{\rm osc}^2}\right) \tag{15}$$

Because the proposed DCLO follows an RC oscillator, the achievable FoM is limited, as in other RC oscillators. This limitation will be analyzed in the next section.

C. DCLO FoM Analysis

The power consumption at RC stage depends on the supplied current from vdd, during the charging period.

$$\begin{aligned}\mathrm{Power}_{\rm RC} &= vdd \cdot \int_{t_0}^{t_3} \frac{vdd}{R_{AB}} e^{-t/R_{AB}C_B} dt \cdot f_{\rm osc} \\ &\approx C_B \cdot vdd^2 \cdot \left(1 - e^{-\frac{1/f_{\rm OSC}}{R_{AB}C_B}}\right) \cdot f_{\rm osc}\end{aligned} \tag{16}$$

For the first inverter stage, dynamic power consumption is

$$\begin{aligned}\mathrm{Power}_{\rm 1st\ inv.\ dynamic} &= vdd \cdot \int_{t_1}^{t_3} C_c \cdot \frac{dV_C}{dt} dt \cdot f_{\rm osc} \\ &= vdd \cdot C_c \cdot \int_{V_c(t_3)}^{vdd} dV_C \cdot f_{\rm osc} \\ &= C_c \cdot vdd \cdot (vdd - V_C(t_3)) \cdot f_{\rm osc},\end{aligned} \tag{17}$$

where $V_C(t_3)$ is

$$\begin{aligned}V_C(t_3) &= vdd - V_b(t_3) \cdot gm \cdot r_o \\ &\approx vdd - vdd(1/2 - e^{-1/f_{\rm osc}/R_{AB}C_B}) \cdot gm \cdot r_o\end{aligned} \tag{18}$$

For (16) and (18), the same assumption of $t_3 - t_0 \to 1/f_{\rm osc}$ is used as in (13).

The DC current of the 1st inverter stage, $\mathrm{I_C}$, increases exponentially with $\mathrm{V_B}$ until $\mathrm{V_B} = vdd/2$ at t_2. After t_2, $\mathrm{V_B}$ decreases since the PMOS transistor starts to limit current supply (Fig. 10). Static current $\mathrm{I_C}$ with the gate-source bias of $\mathrm{V_B} = vdd/2$ can be derived from the well-known ratio of transconductance to current in the subthreshold region, which is

$$\frac{gm}{I_d} = \frac{1}{n \cdot V_T} \tag{19}$$

where V_T is kT/q. Therefore,

$$I_{C\,\rm Max} = gm \cdot n \cdot V_T \tag{20}$$

Assuming a linear transition of I_C during an oscillation period with $\mathrm{I_C(t_0)} = 0$ and $\mathrm{I_C(t_3)} = \alpha \cdot gm \cdot n \cdot V_T$ (Fig. 10, red line), the static power consumption at the 1st inverter stage can be approximated as

$$\mathrm{Power}_{\rm 1st\ inv.\ static} = \frac{1}{2} \cdot \alpha \cdot gm \cdot n \cdot V_T \cdot vdd \tag{21}$$

The fitting coefficient α is used to equalize the total current of linear approximation to that of the real current curve (Fig. 10, shaded area). The expected value of α is $\leq$1 with the small time difference between $t_1 - t_3$. Thus, total power consumption of the first inverter stage is,

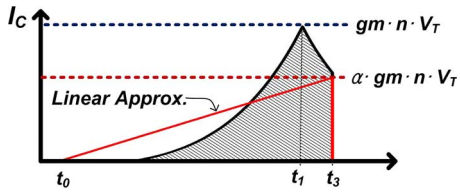

Fig. 10. Approximation of static current consumption from the 1st inverter stage with transient response modeling.

$$\text{Power}_{\text{1st inv.}} = C_c \cdot vdd^2 \cdot \left(\frac{1}{2} - e^{-\frac{\frac{1}{f_{\text{osc}}}}{R_{AB}C_B}}\right) \cdot gm \cdot r_o \cdot f_{\text{osc}} + \frac{1}{2} \cdot \alpha \cdot gm \cdot n \cdot V_T \cdot vdd \quad (22)$$

The power consumption by subsequent inverter stages and the pulse generator can be modeled in a similar way. However, in this analysis, we assume that it is fixed when the oscillation frequency (f_{osc}) is given, because the slew is already limited at the second inverter stage output. Power consumption by other circuits ($\text{Power}_{\text{others}}$) can be obtained from simulation with an oscillation frequency of $f_{osc,}$; the total power consumption is

$$\text{Power}_{\text{osc}} = \text{Power}_{\text{RC}} + \text{Power}_{\text{1st inv.}} + \text{Power}_{\text{others}} \quad (23)$$

Both (16) and (22) indicate that the power consumption mainly depends on charging capacitance and supply voltage. As explained in Section II.A, the benefits of the proposed DCLO architecture are now obvious since it minimizes C_B, C_C and supply voltage to achieve lower power consumption. Fig. 11 shows the calculated FoM_{PN} of DCLO with various values of charging capacitor C_B and C_C in (13), (16), and (22). The supply voltage (=0.45 V) was fixed to keep $\text{Power}_{\text{others}}$ as constant. The fitting factor, α, was set to 1 to represent the most pessimistic case. The designed DCLO achieved -150 dB FoM_{PN}, which is very close to that of practical relaxation oscillator [15], [17]. This result reveals a high potential of DCLO as an oscillator scheme for ultra-low-power consumption. FoM_{PN} is dominated by the first inverter stage; by increasing Cc at the cost of additional power consumption, FoM_{PN} could be improved to -158 dB, which is considered to be the theoretical limit. However, our target was to design the lowest power-consuming DCLO for MDLL ($\text{C}_\text{B} = 100$ f, $\text{C}_\text{C} = 3.75$ f), since it still provides reasonably low noise for a given MDLL application.

III. MDLL With DCLO

A. Circuit Description

Fig. 12 shows the top block diagram of the proposed MDLL which consists of the DCLO, a frequency detector(FD), a lock detector(LD) and an FSM for generating MUX selection signal (SEL) and to update the clock ($f_{\text{ref}}/3$) of the DCLO code. The DCLO is controlled in three steps: a coarse binary 6 b with a successive approximation register(SAR), a fine binary 6 b with another SAR and a finer thermometer 64 b with a

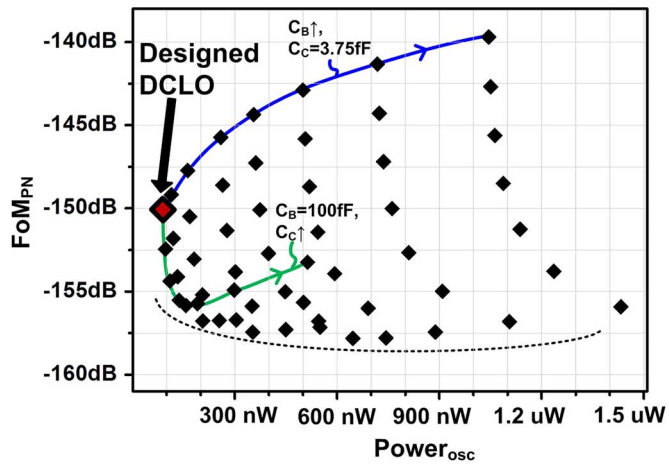

Fig. 11. Phase noise FoM of DCLO.

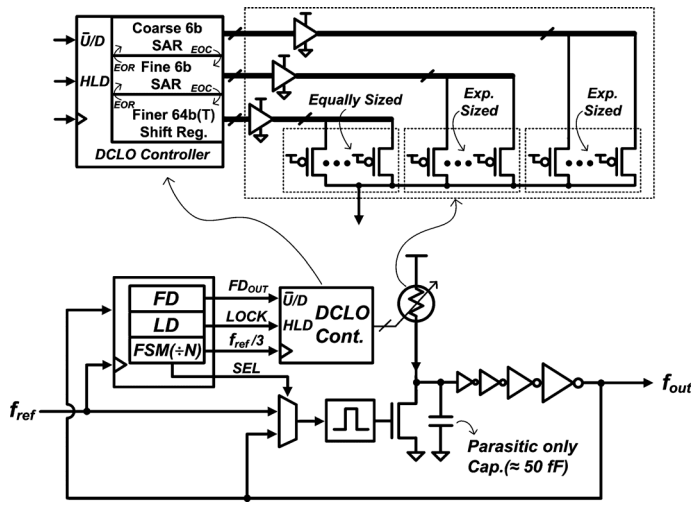

Fig. 12. Top block diagram of MDLL.

shift register (SR). All flip-flops are implemented with thick gate transistors to minimize static leakage current. FD compares f_{out}/N with f_{ref} and drives DCLO controller (DCLO cont.). LD checks whether a pre-defined lock condition is met and triggers LOCK to hold the DCLO control code. In every N cycles of the output clock, FSM sets SEL to inject the reference edge into the pulse generator [18] input instead of the feedback clock. Therefore, the accumulated jitter can be eliminated in every reference cycle. The reference clock (f_{ref}) for the sensor platform is usually tens of kilohertz, which corresponds to the jitter filtering bandwidth. This is the main reason that MDLL architecture is preferred to PLL that has a maximum bandwidth limited to $0.1\times$ f_{ref} for loop stability.

Fig. 13 shows simulated DCLO output frequency versus coarse and fine control codes. The designed DCLO had $>8\times$ frequency range from 400 k to 3.35 MHz at 0.45 V supply voltage, 25°C and TT corner. This wide frequency range is intended to demonstrate megahertz-range generation with the proposed MDLL over PVT variations. Fig. 14 shows the summary of statistics from Monte-Carlo (MC) and corner simulations. MC simulation with 1 k points shows the lowest

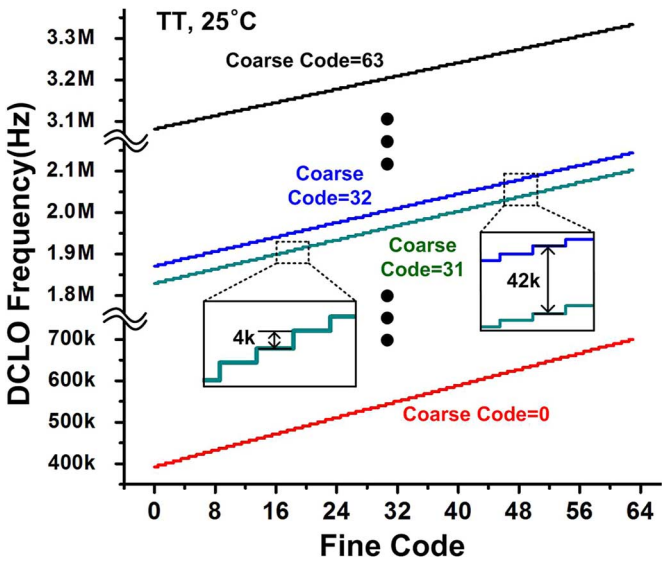

Fig. 13. Simulated DCLO output frequency over coarse/fine codes.

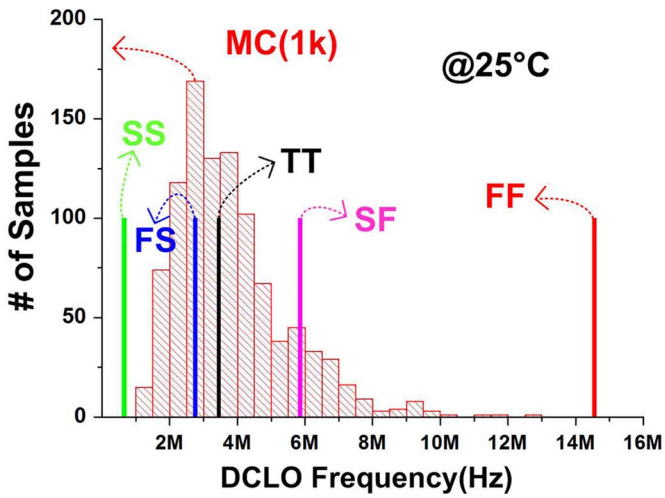

Fig. 14. Statistics from Monte-Carlo(1k) and corner simulations at the highest DCLO output frequency.

output frequency of 1.08 MHz, which satisfies our design target.

Table I summarizes leakage devices used in DCLO. The low VT device is used for coarse stage to obtain a wide frequency range with larger leaking current, whereas the normal VT device is used for fine and finer stages. Except the leaking PMOS device, high VT and thick gate devices were used for the rest of DCLO circuit to minimize the static leakage current. Finer stage has 16 kHz tuning range (250 Hz/b). If the finer control code reaches its boundary, the end-of-range (EOR) signal is triggered to reset the fine stage SAR, and frequency locking is performed again from the fine step. The frequency range of each control stage has about 2 bit overlap with that of the previous control stage to cover a full frequency range even with process variations, and to support the proposed adaptive fast re-locking strategy which will be explained in the next section.

TABLE I
SUMMARY OF DESIGN PARAMETERS USED FOR DCLO LEAKAGE DEVICES

Stage	Coarse	Fine	Finer
Device Type	Low VT PMOS	Normal VT PMOS	Normal VT PMOS
LSB size (W/L)	700n/60n	250n/60n	200n/350n

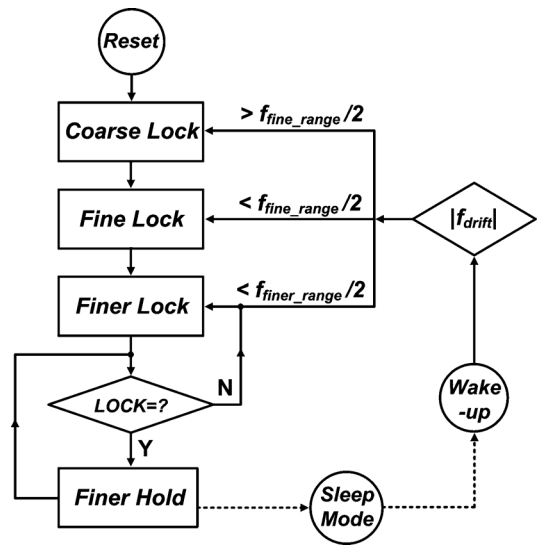

Fig. 15. Lock procedure.

B. Adaptive Fast Relocking Scheme

Fig. 15 shows the detailed lock procedure. After the coarse and fine codes are set, the finer 64 b thermometer code is updated according to FD output until the lock condition is met. LD checks the lock condition in every f_{ref} cycle. If the oscillator output drifts, LD releases the LOCK signal and the finer lock step is performed again. For lock and drift detection, a method similar to that in [19] is adopted.

Considering the application to ultra-low-power sensor platforms, the MDLL is designed to be turned off (sleep mode) when it is not needed. During this sleep time, supply voltage or temperature may change, causing a drift of oscillation frequency. There can be a non-tolerable frequency error after wake-up with the previously held control code. Although the employed binary search algorithm promises relatively fast lock time with the simple control logic [20], further reduction of lock time is preferred in sensor platforms which typically has a strict power budget.

In this work, the coarse and fine codes are stored when the MDLL enters sleep mode. After wake-up, the initial output frequency is set by the previously stored coarse and fine codes with the finer code at the center. Defining f_{drift} as the difference between the target frequency and initial output frequency after wake-up, the first process after wake-up is to compare $|f_{\mathrm{drift}}|$ with $f_{\mathrm{finer\_range}}/2$, where $f_{\mathrm{finer\_range}}$ represents the total frequency range to be covered with the finer code. If f_{drift} is small enough to be tracked only by the finer control ($|f_{\mathrm{drift}}| < f_{\mathrm{finer\_range}}/2$), the locking procedure starts from the finer step;

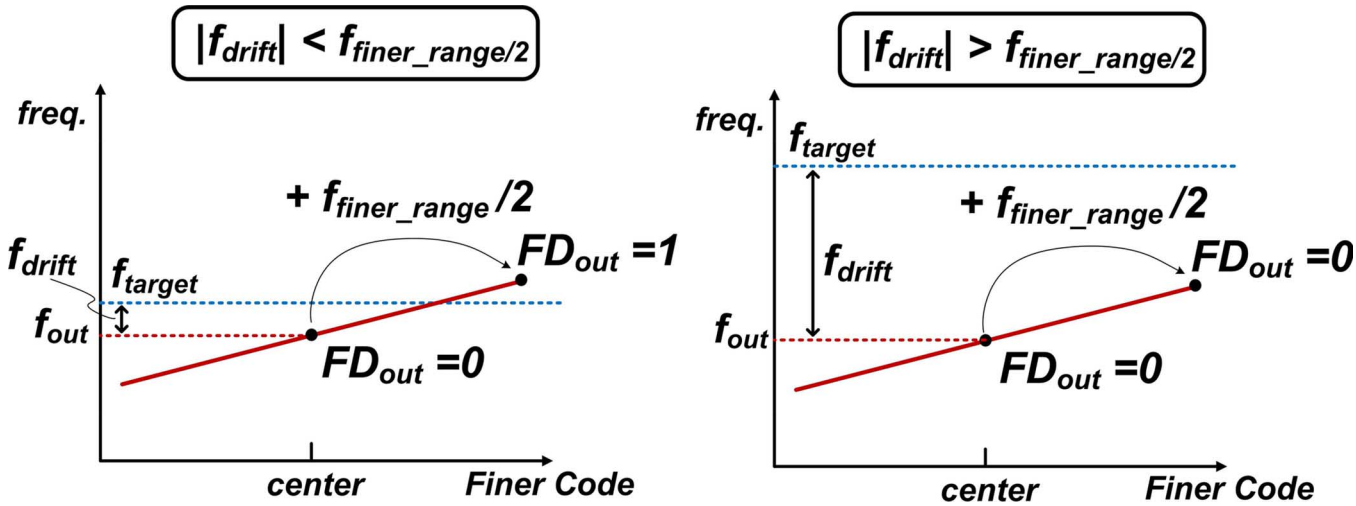

Fig. 16. Example of $|f_{\rm drift}|$ detection procedure.

otherwise, $|f_{\rm drift}|$ is then compared with $f_{\rm fine\_range}/2$, and the locking procedure starts from the coarse step or the fine step depending on the comparison result. This adaptive relocking scheme optimizes power consumption during the lock process, and is especially useful for biomedical applications where temperature does not change much.

Fig. 16 shows an example of $|f_{\rm drift}|$ detection procedure when the initial output frequency ($f_{\rm out}$) is lower than $f_{\rm target}$. $|f_{\rm drift}|$ can be (a) smaller or (b) larger than $f_{\rm finer\_range}/2$. After wake-up, $\rm FD_{out}$ generates '0'. Then, $f_{\rm out}$ is set to move up by the half of the lock range of finer stage ($\rm f_{finer\_range}/2$). If the polarity of $\rm FD_{out}$ changes (`0' $\rightarrow$ `1'), it means the $|f_{\rm drift}|$ can be tracked by the finer stage only and relocking starts from the finer stage. If the polarity is not changed (`0' $\rightarrow$ `0'), it means $|f_{\rm drift}|$ is over the lock range of the finer stage. Then, a similar comparison between $|f_{\rm drift}|$ and the half of fine lock range ($f_{\rm fine\_range}/2$) will be performed for the next decision.

IV. Implementation Results

The MDLL was implemented in a 65 nm CMOS (Fig. 17). The core area is 0.026 $\rm mm^2$. With a 32 kHz reference, which is a typically used frequency for standard watch or a real-time clock, the MDLL generated 3.2 MHz (N = 100) and consumed 423 nW from a 0.45 V supply, showing an energy efficiency FoM of 0.132 μ W/MHz. Fig. 18 shows measured locking transients after wake-up, for the cases of large (upper) and small (lower) frequency drifts. The measurement clearly demonstrates adaptive fast relocking operation depending on the amount of $|f_{\rm drift}|$. 15 cycles of DCLO update clock ($f_{\rm ref}/3$) are needed for large $|f_{\rm drift}|$, while only 4 cycles is needed for small $|f_{\rm drift}|$. The frequency plot also shows the output frequency is stably settled right after the wake-up. Therefore $|f_{\rm drift}|$ detection can succeed immediately.

Fig. 19 shows the measured frequency spectrum at 3.2 MHz output. Fig. 20 shows phase noise measurement with the same condition, revealing rejection of the in-band noise below 32 kHz. The out-of-band noise at 1 MHz offset was -95 dBc/Hz. The phase noise performance is matched well with prediction and simulation presented in Section II.B. There

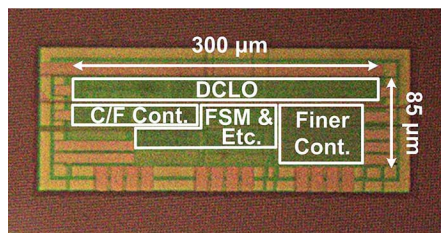

Fig. 17. Chip microphotograph.

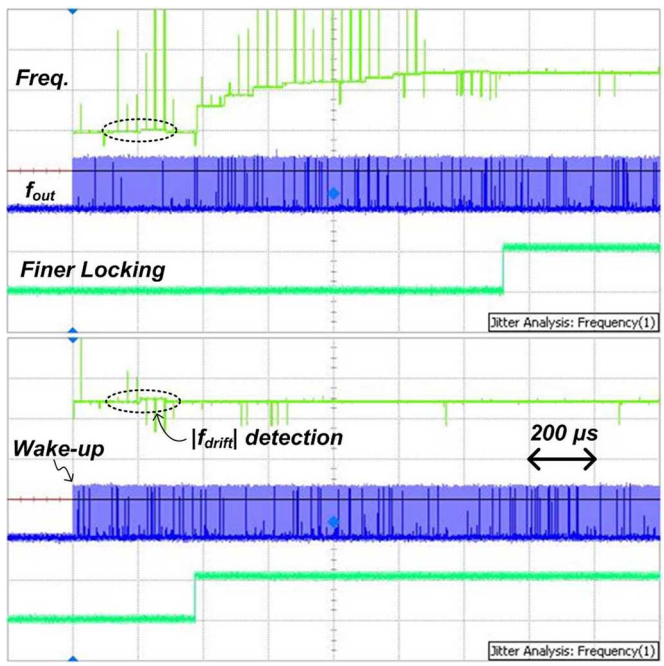

Fig. 18. Measured lock transients after wake-up with (upper) a large frequency drift and (lower) a small frequency drift.

are also harmonic spurs from the reference clock, and they degrade the phase noise near harmonic offset frequencies. However, the spurs contributed little to the total jitter. Integrated $\rm jitter_{rms(10\ k-1\ MHz)}$ was measured as 7.98 ns, while calculated(no spur included) $\rm jitter_{rms(10\ k-1\ MHz)}$ was 7.59 ns

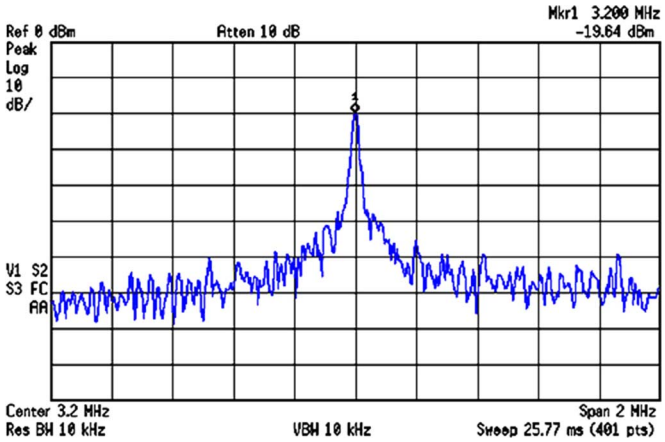

Fig. 19. Measured frequency spectrum.

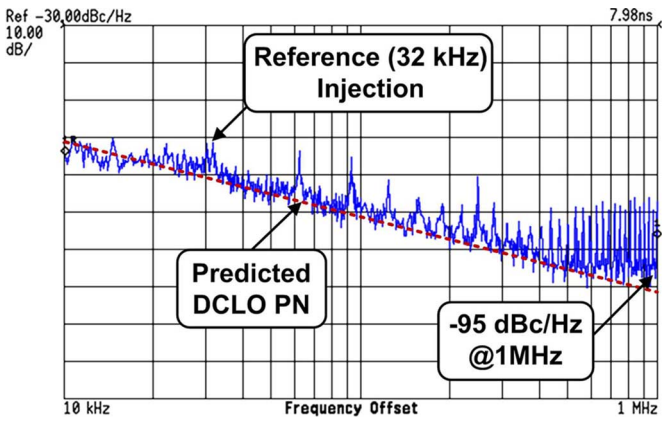

Fig. 20. Measured phase noise (N = 100), dashed line shows predicted phase noise of DCLO.

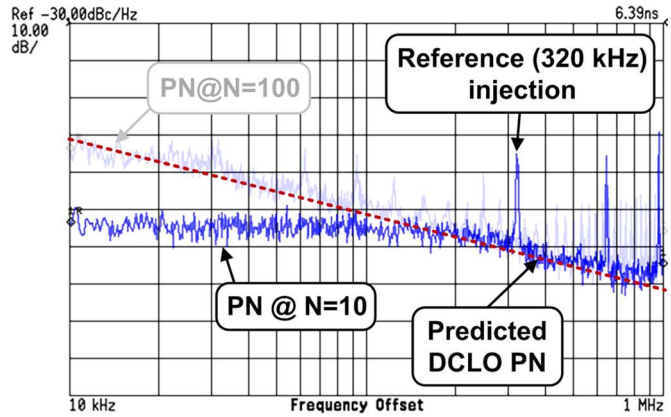

Fig. 21. Measured phase noise (N = 10).

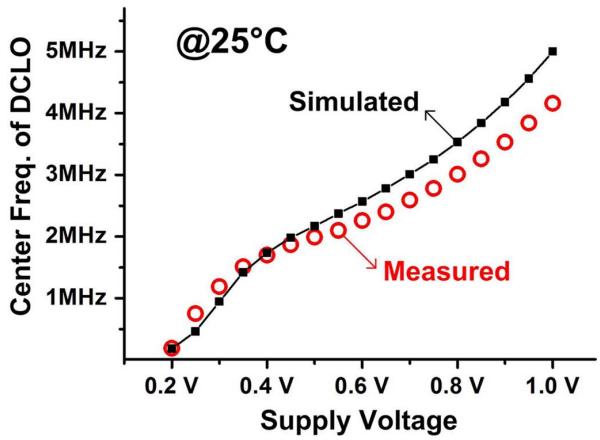

Fig. 22. Comparison of simulated and measured DCLO frequencies over supply voltage variation.

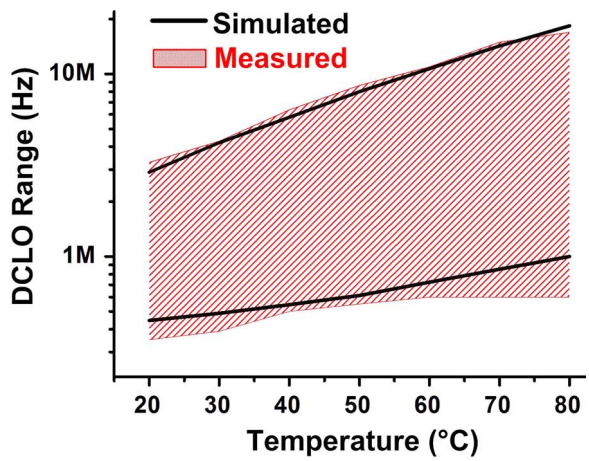

Fig. 23. Comparison of simulated and measured DCLO frequency ranges over temperature variation (supply = 0.45 V).

with the predicted line of DCLO phase noise and the measured noise level of −65 dBc/Hz below 32 kHz offset. The dominant jitter contribution comes from the high in-band noise due to small bandwidth. Note that the total integrated jitter will be much worse with PLL architecture, in which the bandwidth should be smaller than 3.2 kHz.

The phase noise with different multiplication factors of 10 (N = 10) was also measured in Fig. 21. To obtain the same output frequency of 3.2 MHz, a 320 kHz reference clock was used. Measurement with N = 100 is superimposed with shade for the comparison. With this measurement, the in-band noise rejection with MDLL architecture is more clearly observed. Reference and harmonic spurs are more visible, and total integrated $\text{jitter}_{\text{rms}(10\text{ k}-1\text{ MHz})}$ (6.39 ns) is now dominated by spurs. With the predicted line of DCLO phase noise and the measured noise level of −85 dBc/Hz below 200 kHz offset, calculated jitter without spur was 2.06 ns. In this case of the lower multiplication factor with higher reference clock, using additional offset minimization schemes for phase detection [21] could be useful to reduce the spur-induced total jitter. For N = 10, 0.52 V supply voltage was used to operate control circuits with 10× higher reference frequency. The FoM with N = 10 was 0.151 μW/MHz.

Figs. 22–24 verify the simulation validity of the proposed leakage current based design. Measured DCLO characteristics are matched well with simulations under voltage (Fig. 22) and temperature variations (Fig. 23). The results also show that designed DCLO had a sufficiently wide lock range to generate megahertz frequencies in the MDLL even with large temperature variations of leakage current. Fig. 24 shows that the center frequencies of all 10 measured samples fall around the mean value of the Monte-Carlo simulation (1 k) results.

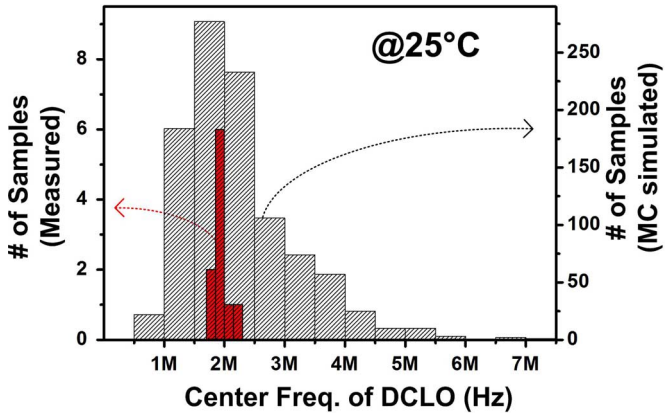

Fig. 24. Comparison of DCLO center frequencies between Monte-Carlo (1 k) simulation and measured 10 samples (supply = 0.45 V).

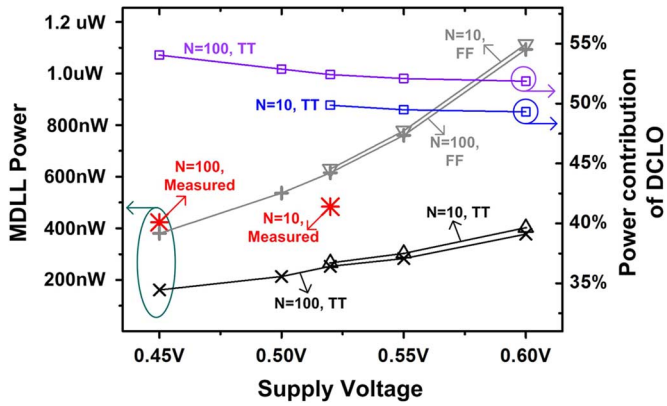

Fig. 25. Comparison of measured and simulated power consumption of MDLL, and power contribution of DCLO(simulated).

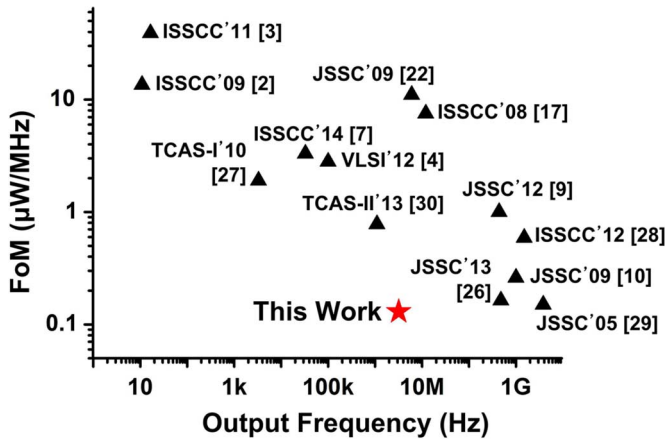

Fig. 26. FoM comparison with state-of-the-art clock generators.

It is worthwhile to mention the supply sensitivity of DCLO around 0.4–0.6 V supply voltage. The DCLO's sensitivity to supply voltage was $0.5\%-f_{\mathrm{VCO}}/1\%-\mathrm{VDD}$, whereas a typical inverter stage has a larger sensitivity of $1\%-\mathrm{delay}/1\%-\mathrm{VDD}$ [22]. It is because the leaking PMOS device can be regarded as a subthreshold biased current source in this low supply voltage range and experiences less dependency on supply change. When drain-source voltage is >0.6 V, the short channel effect exponentially increases leakage current, and the oscillation frequency also follows this trend. An abrupt frequency change below 0.4 V(Fig. 22) is due to the significant portion of a subthreshold circuit delay of the inverters.

Fig. 25 compares simulated power consumption of MDLL versus supply voltage with different process corner conditions at 25°C and measured results. While measured DCLO frequencies were matched well with simulation results at given TT corner (Fig. 22–24), the measured power consumption was about 200 nW higher than TT corner simulation. This excess power consumption is due to the static leakage current from supply-decoupling MOS capacitor, which was taken as the filler for the rest of chip area (0.7 mm^2). Since an appropriate leakage model for the thick-gate transistor used for MOS capacitor was not available during the design process, the large area of the MOS capacitor caused the unexpected leakage portion. The figure also shows the power contribution of DCLO which gradually decreases (54% $\rightarrow$ 52% with N = 100). It is because the static leakage power of control circuits increases exponentially while DCLO power is proportional to the square of the supply voltage. With N = 10 mode, DCLO takes 50% and 49% of the total power consumption at 0.52 V and 0.6 V, respectively. The difference from the N = 100 mode is due to the extra dynamic power consumption of the control circuits with $\times 10$ higher reference frequency.

Table II summarizes the phase noise performance of previously published state-of-the art low power oscillators. The power consumption of the proposed oscillator is speculated from simulated power consumption. This comparison shows that the leakage based oscillator can be also a promising candidate for an accurate clock generation while keeping an ultra-low-power consumption. Table III compares the performance of proposed MDLL with other state of art low-power and high-efficiency clock generators. Even with a high in-band noise floor due to the low reference frequency of 32 kHz, this work has comparable jitter performance to those of [9], [10], which were designed specifically for the sensor node system. Fig. 26 visualizes the energy efficiency FoM of state-of-the-art clock generators versus their output frequencies. The trend reveals that FoM for the lower frequency generation is worse than that for the higher frequency generation, as pointed out in Section I. Nevertheless, this work achieved the best energy efficiency.

V. Conclusion

A digitally controlled oscillator whose frequency is modulated by leakage current is introduced in an all-digital MDLL for ultra-low-power sensor platforms. The proposed leakage control circuit facilitates easy and fully-digital fine frequency tuning and ultra-low-power frequency generation. To investigate the proposed DCLO in detail, it is modeled as an effective RC oscillator. The equation for the phase noise FoM is also derived along with noise and power analyses. The analyses show that the FoM limit of the proposed DCLO is similar to that of RC-based oscillator. A fast relocking scheme suitable for sensor platforms is also used in the proposed MDLL. The MDLL automatically detects frequency drift after wake-up, and adaptively chooses the optimal frequency-locking stage

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED OSCILLATORS

	This Work	JSSC'02 [16]	ISSCC'08 [17]	JSSC'09 [23]	ISSCC'10 [24]	TCAS-I'09 [25]
Type	DCLO	Relaxation	Relaxation	RC	Relaxation	LC
Frequency	3.2 MHz	1.5 MHz	12 MHz	6 MHz	14 MHz	24 MHz
Power	90 nW*	1.8 mW	90 µW	66 µW	25 µW	49.5 mW
FoM_{PN}	-150.6 dB	-150.7 dB	-162.0 dB	-142.0 dB	-146.0 dB	-148.7 dB
Area	0.006 mm^2	1.17 mm^2	0.03 mm^2	0.03 mm^2	0.04 mm^2	2.25 mm^2
Process	65 nm	0.8 µm	65 nm	65 nm	0.18 µm	0.25 µm

*Simulated

TABLE III
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED LOW POWER- HIGH EFFICIENCY CLOCK GENERATORS

	This Work	JSSC'12 [9]	JSSC'09 [10]	JSSC'13[26]	ISSCC'12 [28]
Architecture	Digital MDLL	Fracional-N PLL	Duty-Cycled PLL	Digital PLL	Digital MDLL
Frequency Range	370k~3.8MHz	400~433MHz	300M~1.2GHz	176-480MHz	0.8-1.8GHz
Reference Frequency	32kHz	1.84MHz	20MHz	30MHz	375MHz
RMS Jitter (Integration Range)	0.025UI_{rms} (10k-1 MHz)	0.024UI_{rms} (7k hits)	0.03UI_{rms} (50 hits)	0.0037UI_{rms} (20k hits)	0.0006UI_{rms} (10k-100MHz)
Power	484nW	440uW	260uW	78uW	890uW
Area	0.026mm^2	0.0736mm^2	0.028mm^2	0.057mm^2	0.25mm^2
Process	65nm	130nm	65nm	90nm	130nm

to reduce idling power of the whole system. The MDLL with DCLO was implemented with 65 nm CMOS process and consumes 423 nW for 3.2 MHz generation, showing an energy efficiency FoM of 0.132 μW/MHz.

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Dong-Woo Jee (M'13) received the B.S., M.S., and Ph.D. degrees in electronic and electrical engineering from Pohang University of Science and Technology (POSTECH), Korea, in 2006, 2009, and 2013, respectively.

From 2011 to 2012, he was a Visiting Researcher with the University of Michigan, Ann Arbor, MI, USA. From 2013 to 2015, he worked as an Analog IC Designer at Biomedical Circuit group of IMEC in Leuven, Belgium. In 2015, he joined Ajou University, where he is currently an Assistant Professor. His research interests include circuit technique for scaled CMOS device, analog/digital frequency synthesizer PLL, ultra-low-power clock generation for sensor node system, sensor interfaces and analog circuits for biomedical applications.

Dr. Jee was the recipient of the Gold Prize at the 17th HumanTech Paper Award hosted by Samsung Electronics in 2011.

Dennis Sylvester (S'95–M'00–SM'04–F'11) received the Ph.D. in electrical engineering from the University of California, Berkeley, CA, USA, where his dissertation was recognized with the David J. Sakrison Memorial Prize as the most outstanding research in the UC-Berkeley EECS department.

He is a Professor of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, MI, USA, and Director of the Michigan Integrated Circuits Laboratory (MICL), a group of ten faculty and 70+ graduate students. He has held research staff positions in the Advanced Technology Group of Synopsys, Mountain View, CA, Hewlett-Packard Laboratories, Palo Alto, CA, and visiting professorships at the National University of Singapore and Nanyang Technological University. He has published over 400 articles along with one book and several book chapters. His research interests include the design of millimeter-scale computing systems and energy efficient near-threshold computing. He holds 22 US patents. He also serves as a consultant and technical advisory board member for electronic design automation and semiconductor firms in these areas. He co-founded Ambiq Micro, a fabless semiconductor company developing ultra-low power mixed-signal solutions for compact wireless devices.

Dr. Sylvester received an NSF CAREER award, the Beatrice Winner Award at ISSCC, an IBM Faculty Award, an SRC Inventor Recognition Award, and eight best paper awards and nominations. He is the recipient of the ACM SIGDA Outstanding New Faculty Award and the University of Michigan Henry Russel Award for distinguished scholarship. He serves on the technical program committee of the IEEE International Solid-State Circuits Conference and previously served on the executive committee of the ACM/IEEE Design Automation Conference. He has served as Associate Editor for IEEE TRANSACTIONS ON CAD and IEEE TRANSACTIONS ON VLSI SYSTEMS and Guest Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II.

David Blaauw (M'94–SM'07–F'12) received the B.S. degree in physics and computer science from Duke University in 1986, and the Ph.D. in computer science from the University of Illinois, Urbana, IL, USA, in 1991.

After his studies, he worked for Motorola, Inc. in Austin, TX, USA, where he was the manager of the High Performance Design Technology group. Since August 2001, he has been on the faculty at the University of Michigan, Ann Arbor, MI, USA, where he is a Professor. He has published over 450 papers and holds 40 patents. His work has focussed on VLSI design with particular emphasis on ultra low power and high performance design.

Dr. Blaauw was the Technical Program Chair and General Chair for the International Symposium on Low Power Electronic and Design. He was also the Technical Program Co-Chair of the ACM/IEEE Design Automation Conference and a member of the ISSCC Technical Program Committee.

Jae-Yoon Sim (M'02–SM'13) received the B.S., M.S., and Ph.D. degrees in electronic and electrical engineering from Pohang University of Science and Technology (POSTECH), Korea, in 1993, 1995, and 1999, respectively.

From 1999 to 2005, he worked as a senior engineer at Samsung Electronics, Korea. From 2003, to 2005, he was a post-doctoral researcher with the University of Southern California, Los Angeles, CA, USA. From 2011 to 2012, he was a visiting scholar with the University of Michigan, Ann Arbor, MI, USA. In 2005, he joined POSTECH, where he is currently an Associate Professor. His research interests include high-speed serial/parallel links, PLLs, data converters and power module for plasma generation.

Prof. Sim has served on the Technical Program Committees of the IEEE International Solid-State Circuits Conference (ISSCC), Symposium on VLSI Circuits, and Asian Solid-State Circuits Conference (ASSCC). He received the Author Recognition Award at ISSCC 2013 and was a co-recipient of the Takuo Sugano Award at ISSCC 2001.