A 120nW 8b Sub-ranging SAR ADC with Signal-Dependent Charge Recycling for Biomedical Applications

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Abstract

We present an 8-bit sub-ranging SAR ADC designed for bursty signals having long time periods with small code spread. A modified capacitive-DAC (CDAC) saves previous sample's MSB voltage and reuses it throughout subsequent conversions. This prevents unnecessary switching of large MSB capacitors as well as conversion cycles, reducing energy consumed in the comparator and digital logic and yielding total energy savings of 2.6×. In 0.18µm CMOS, the ADC consumes 120nW at 0.6V and 100kS/s with 46.9dB SNDR.

Introduction

Interest in wireless sensor networks has grown recently for biomedical (ExG) and environmental monitoring (e.g., temperature and pressure) applications [1-2]. In these sensor interfaces, the SAR ADC is a common choice due to low power consumption and high energy efficiency. Many signals in these targeted application areas have the following characteristics: 1) Low activity for the majority of the time, i.e., short-term signal variation is small; 2) Long-term signal variation is wide; and 3) Bursts of activity occasionally occur within a short time period, such as a neuron spike. Several recent works were proposed that take advantage of these signal characteristics. A bypass window technique [3] skips bit cycles when the signal is within a predefined range while an LSB-first approximation [4] starts the conversion from the previous sample. Another approach [5] modulates sampling rate according to signal activity. However, a predefined window cannot track a signal's low activity region while the LSB-first approximation toggles MSBs in the DAC every cycle for an initial guess, consuming energy. In this work, we propose a sub-ranging ADC that uses a moving window and stores the previous MSBs voltage value on a series capacitor. This enables the MSBs of the CDAC to be held fixed in subsequent cycles. Due to the large MSB capacitors size, substantial energy is saved in the CDAC as well as the comparator and logic. Energy savings are signal dependent; the approach was applied to 39 actual ECG recordings and showed 2.6× energy savings while fully preserving arrhythmia detection accuracy.

Proposed Circuit

Fig. 1 describes the conceptual operation of the proposed *N*-bit ADC. After an initial full conversion, an *m*-bit sub-ranging window is set based on the conversion result. Then, the next conversion begins within that window, skipping conversion cycles for *m* MSBs. The architecture is similar to the conventional SAR ADC except for a series capacitor (C_{MSB}) between CDAC and comparator (Fig. 2a). C_{MSB} is used to store the voltage corresponding to the most significant *m*-bits (V_{MSB}) from the previous sample (Fig. 2b). If the next sample falls within the same sub-ranging window, energy to switch the MSB capacitors reduces dramatically (by 16× for 4 MSBs in an 8-bit SAR) while comparator and logic energy reduces linearly with the number of MSBs stored due to reduced conversion cycles. When the signal goes out of the predefined window, the ADC switches back to full-range mode for one cycle to re-acquire the signal.

Fig. 3 shows detailed ADC operation. In MSB phase 1, the selected *m*-bit capacitor array is configured based on the previous MSBs. In phase 2, selected capacitors are connected to V_{ref-} for charge redistribution. As a result, the *m*-bit MSB voltage of the previous sample is stored across C_{MSB}. Unselected capacitors in the CDAC are precharged to (V_{ref+}-V_{CM}) during MSB phase 1 to prevent the bottom plate voltage from going below ground due to capacitive coupling in MSB phase 2. After the C_{MSB} is set, the subsequent sample and conversion phases are the same as in conventional SAR operation except that only LSBs are computed. During LSB conversion V_{COMP} can be expressed as:

$$V_{COMP} = V_{CM} + -V_{in} + (\frac{C_{1,M}}{C_{T,M}} + \frac{C_{1,L}}{C_{T,N}})(V_{ref+} - V_{ref-}),$$

where $C_{T,M}$ is the capacitance of *m*-bit capacitor array, $C_{T,N}$ is the capacitance of the *N*-bit capacitor array, $C_{1,M}$ and $C_{1,L}$ are the sum of all capacitances connected to V_{ref+} during MSB phase 1 and LSB conversion, respectively. This conversion process is identical to the conventional SAR approach. Since total charge at node V_{COMP} remains constant, the voltage across C_{MSB} always returns to V_{MSB} at the end of conversion, enabling reuse of the MSB information.

Due to parasitic capacitances, the stored charge will not be scaled correctly during LSB conversions, which causes non-uniformity between sub-ranging windows. This is solved by introducing a correction capacitor (C_{COR}, Fig. 4a). C_{COR} is connected to V_{ref-} during LSB conversions to cancel out this scaling error and is connected to V_{ref+} in MSB phase 1 for pre-charging. When C_{COR} is correctly set, the conversion process becomes immune to parasitic capacitances. Simulated INL across C_{COR} error shows that linearity is relatively insensitive to the absolute value of C_{COR} (Fig. 4b).

As leakage on C_{MSB} can cause errors as time passes, a refresh rate is set to restore V_{MSB} (0 to 63 cycles in our implementation). This rate can be optimized to maximize energy savings depending on the environment (e.g., temperature). When the conversion result is out of the sub-range, an error flag is set and C_{MSB} is reset in the subsequent full-range conversion. Fig. 5 shows the overall operating algorithm.

Total energy consumed by the proposed ADC depends on the number of MSBs (*m*) that are stored on C_{MSB} for sub-ranging (Fig. 6). As *m* increases, pre-charge energy for the unused capacitors goes down as well as comparator, DAC, and logic energy due to fewer cycles for conversion. However, energy and frequency of storing the MSB voltage increases. Simulation showed a minimum operating energy when *m* is 4 bits. Note that energy is consumed for storing MSB and pre-charging only when the signal is out of the sub-ranging window (3.7% of total cycle during ECG detection). The selection of the unit capacitance in the *m*-bit capacitor array also impacts energy. A lower capacitance is preferred to reduce energy during MSB configuration, but comparator energy increases due to the need to compensate for gain loss arising from the series connection of C_{MSB} and C_{p2}. The ADC uses a StrongARM comparator with 3-sigma offset of ±30mV, calibrated with binary 4-bit capacitors at the comparator outputs. CDAC is composed of 4.5fF MOM unit capacitors.

Measurements

The test chip is fabricated in 0.18µm CMOS with an area of 0.12mm^2. The proposed design is tested at 100kS/s and operates from a single 0.6V supply voltage. Measured DNL and INL are +0.3/-0.3 LSB and +0.6/-0.6 LSB, respectively (Fig 7). Fig. 8 shows the measured power spectrum. Measured SNDR and SFDR are 46.9dB and 63.8dB, respectively. Fig. 9 shows measured data from an ECG simulator. Power reduces by 2.6× compared to an 8-bit conventional SAR ADC with negligible data loss. Effectiveness of the sub-ranging approach is assessed with an atrial fibrillation detection algorithm [7] using 39 actual patient ECG waveforms (Fig. 10). Fig. 10 shows that the classifier output is identical with the conventional and proposed ADCs, indicating the potential of this approach for biomedical applications. Fig. 11 shows the chip micrograph. Table I summarizes this work and compares against state-of-art SAR ADCs with similar application focus.

References

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[5] M. Trakimas *et al.*, TCAS, 2011. [6] M. Yip *et al*., ISSCC, 2011.
[7] H. Oral *et al*., U.S. Patent 201 3019 7380 A1, Aug. 2013.

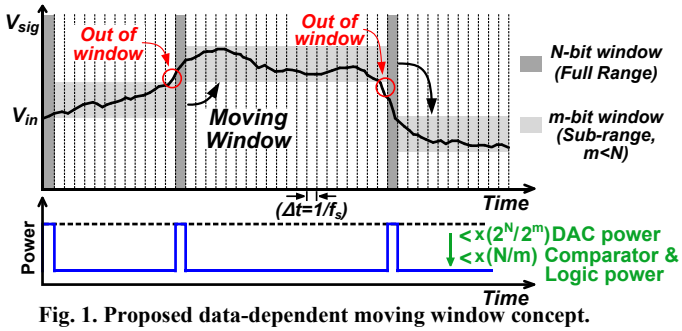

Fig. 1. Proposed data-dependent moving window concept.

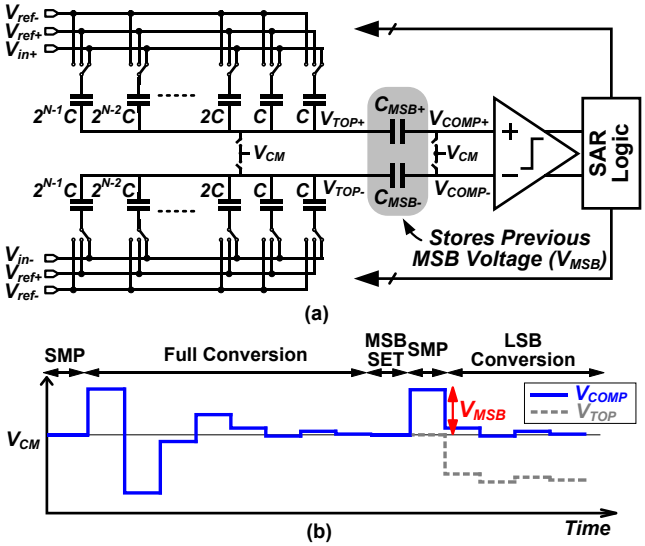

Fig. 2. (a) Proposed architecture of sub-ranging SAR ADC and (b) operation of MSB recycling.

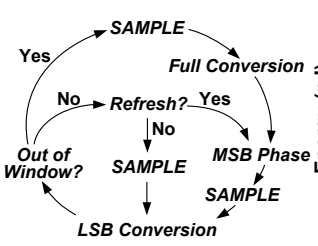

Fig. 5. Conversion Algorithm.

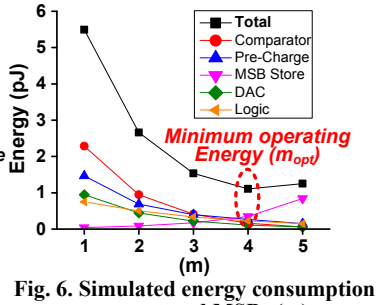

Fig. 6. Simulated energy consumption versus stored MSBs (m).

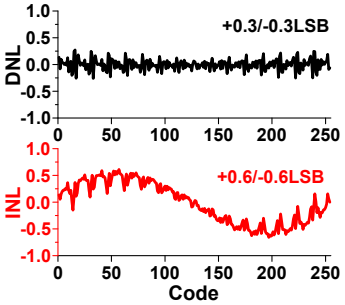

Fig. 7. Measured DNL and INL.

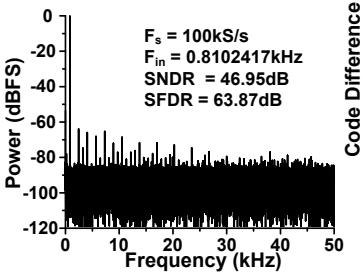

Fig. 8. Meausred FFT of ADC output data.

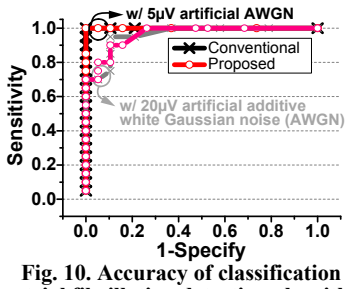

Fig. 10. Accuracy of classification using atrial fibrillation detection algorithm [7].

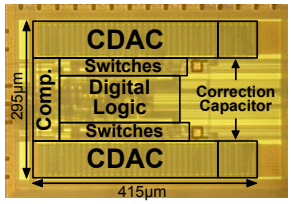

Fig. 11. Die micrograph.

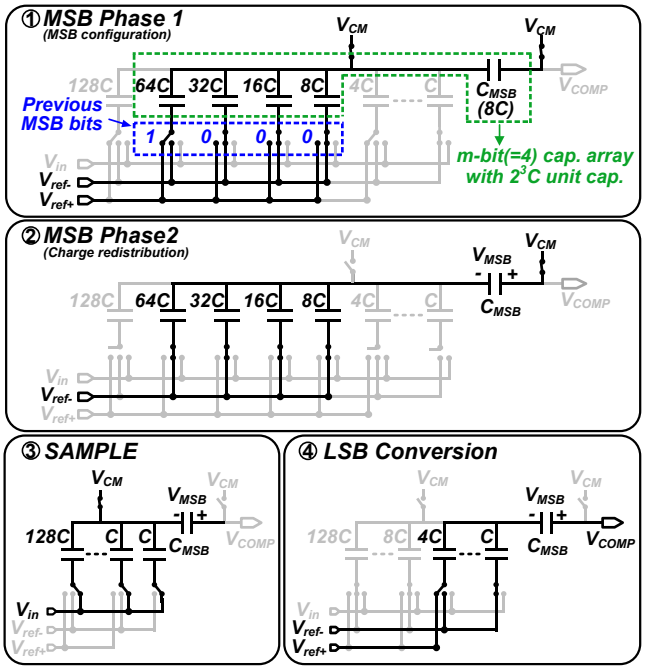

Fig. 3. Sub-ranging procedure using capacitive DAC.

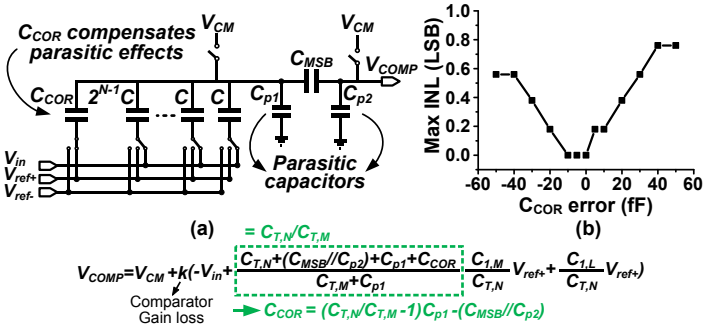

Fig. 4. (a) Correction capacitor (C_{COR}) for parasitic compensation and (b) effect of correction error on linearity in simulation.

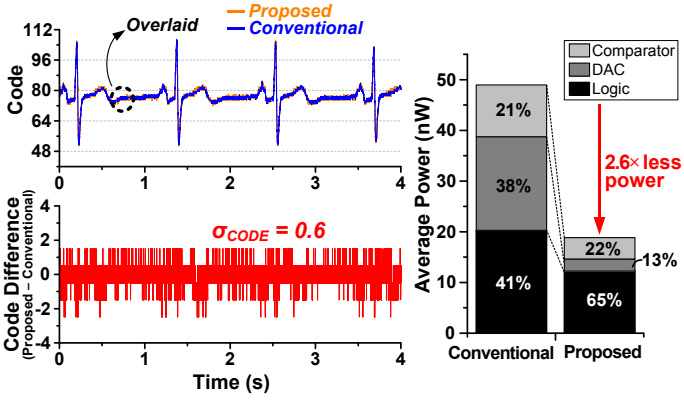

Fig. 9. Measurement result with ECG simulator sampled at 8kHz.

Table I. Performance summary and comparison.

	This Work	[3]	[4]	[5]	[6]
Technology	**0.18μm**	0.18μm	0.18μm	0.18μm	65nm
Area [mm^2]	**0.12**	0.08	0.12	0.96	0.21
Supply Voltage [V]	**0.6**	0.6	0.6	0.7	0.55
Sampling Rate [kS/s]	**100**	200	16	50	20
Resolution [bit]	**8**	10	10	8	8
Power [nW]	**120**	1040	47-170*	25000	146
ENOB [bit]	**7.5**	9.3	9.7	6.9	7.5
FOM [fJ/conv-step]	**6.6**	8.03	3.5-20*	4186	40

*For best (DC) and worst case (Full Nyquist sinusoid) inputs