Noise Analysis Methodology for Partially Depleted SOI Circuits

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Abstract

In PD SOI technology, signal switching history and intial state of the circuit nodes can affect the device body voltage and also cause parasitic BJT leakage currents, which can lead to significant increase in noise propagation and noise failures. In this paper we explore the effects of input switching history, initial circuit conditions and the parasitic BJT device on all steps in a traditional noise analysis methodology: noise injection, noise propagation and noise failure criterion. We present a new noise analysis methodology to account for the floating body and the BJT effects in PD SOI technology. We demonstrate the new technique on an industrial microprocessor design in PD SOI and show that the current noise analysis methods do not account for 56% of noise fails.

Introduction

With the emergence of partially-depleted silicon-on-insulator (PD-SOI) technology, new design concerns such as the floating body (FB) and device threshold voltage (Vt) variations and parasitic bipolar junction (BJT) devices have surfaced (1)(3). Fully depleted (FD) SOI technology does not suffer from body voltage variations but it has so far had limited commercial applications due to sensitivity to process and gate-oxide thickness variations and large source/drain resistance degrading the device performance (2).

Although PD-SOI technology has yielded significant gains in circuit performance, these gains have come at the cost of increased noise sensitivity due to the issues listed below:

1. Reduced source/drain capacitance i.e. smaller ground to coupling capacitance ratio, thereby increasing noise susceptibility.
2. Device body voltage variations with input switching activity. Higher body voltages yield lower device threshold voltages and increased noise propagation and noise failure.
3. Parasitic BJT in parallel with a device which can turn on when the device is in an off-state, resulting in drain-to-source current and injection of noise at the device output.

Furthermore, the increase in gate-oxide leakage current has increased the dependence of the body voltage on the gate voltage. This has exacerbated body voltage variations and its impact on noise in PD-SOI circuits. These effects necessitate changes in current methods of noise analysis.

Fig. 1 shows the typical noise analysis steps with proposed SOI modifications.The net under consideration for noise is called the *victim* net and the nets capacitively coupled to it are called the *aggressor* nets. Aggressors switching from low to high would cause a *low overshoot* type of noise on a victim held at logic low. Similarly, an aggressors switching from high to low would cause *high undershoot* type of noise

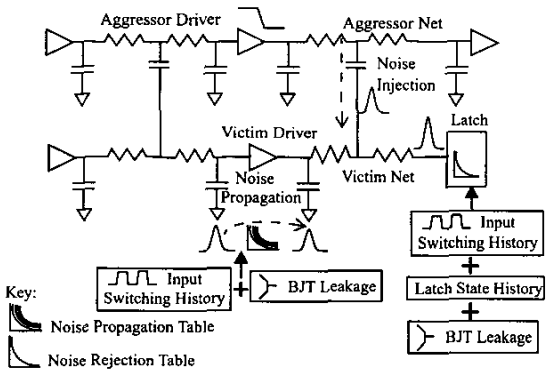

Figure 1. Traditional Noise Methodology with SOI Modifications

on a victim held at logic high.Traditional noise analysis tools (5) typically compute noise in three phases, as discussed below:

1. *Noise injection*: noise on a victim is computed due to the switching of aggressors.
2. *Noise propagation*: noise at the output of a circuit is computed given a noise pulse at its input.
3. *Noise failure:* injected noise and propagated noise is computed along a logic path till a latch is encountered and failure is determined if the latch state is altered.

In PD-SOI, the threshold voltage variation and BJT leakage would cause significant variation in the amount of propagated noise and injected noise. It would also affect the latch immunity. While extensive work has focussed on the impact of the switching history on circuit delay (3)(4), relatively little work is focussed on its impact on noise. Previous work in PD-SOI noise analysis (6) deals with the calculation of specific body voltages during noise analysis but requires apriori knowledge of the input states and switching histories of the nets. For most nets, however, the switching history is unknown and a worst-case analysis is needed to ensure a robust design.

In this paper, we propose a practical methodology that allows direct assignment of the worst-case switching history scenario to a circuit. The proposed approach is critical in detection and elimination of all possible noise failures in PD-SOI circuits. We present the results from our proposed method for 2,466 nets for an industrial microprocessor design in 65nm gate, 20A oxide thickness partially-depleted SOI technology (7) and show that current noise methodology only reports 65% of the nets above a noise threshold of 50mV and accounts for 44% of all possible noise failures when used for SOI based designs thus, demonstrating the need for SOI based noise analysis methodology.

Steps for SOI Noise Analysis

For SOI based noise analysis as shown in Fig. 1, we

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develop an analysis approach for determining the combination of switching history for inputs to a circuit such that it results in maximum noise propagation through the circuit. This approach was used to build noise propagation tables

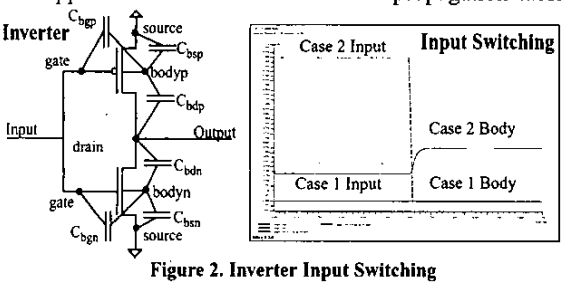


Figure 2. Inverter Input Switching

and the noise rejection tables for circuits in an industrial microprocessor design. For maximum impact of switching on the noise propagation, we assume input switching in the cycle before the noise event on the input to a circuit In a circuit, the input from which the noise pulse is propagated to the circuit output is called the *primary input.*

We divide the circuits on the basis of their topology into two categories; series/parallel structures, such as nand, nor, aoi circuits and pass transistor structures, such as multiplexers.

1. Noise Propagation

The steps for determining the input switching history for maximum noise propagation for low overshoot type of noise are outlined as follows,

1. Add switching history to the primary input.
2. Determine the circuit inputs controlling the gate terminals of nfets in series stack with the primary input controlled device, make them logic high.
3. Determine the circuit inputs controlling the gate terminals of nfets in parallel stack with the primary input controlled device, make them logic low with switching history.
4. If inputs controlling the nfets in parallel stacks with the primary input controlled nfet can have a switching history resulting in the parasitic BJT leakage, calculate the BJT noise and superimpose on the worst case propagated noise.

1.1 Series/Parallel Stacks

In the simple case of an inverter, the input switching, case2 in Fig. 2 (methodology step1), should yield the maximum low overshoot noise propagation. Noise propagation curves are shown in Fig. 3. The plot has input noise pulse

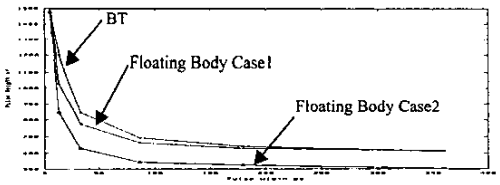


Figure 3. Inverter Noise Propagation Curves

height on y-axis and input noise width on x-axis that cause a fixed noise voltage (50 mV) at the inverter output. The plot also has a noise propagation curve for a body tied inverter. As expected, low overshoot noise propagation curve for floating body circuit with switching history for the input, case2 is the worst. The body tied (BT) circuit has the best noise immunity, i.e. SOI is more noise prone.

Similarly for nand3 gate, to propagate the low overshoot type noise from the primary input A0 to the output, case2 in Fig. 4 has switching history for A0 (SOI methodology step1), A1 and A2 are held high (SOI methodology step2). Low overshoot noise propagation curves for nand3 are shown in Fig. 4. Case2 has the worst low overshoot noise propagation curve. Body tied nand3 has the smallest noise propagation.

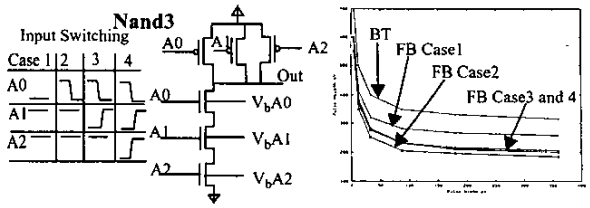


Figure 4. Series Stack Nand3

For a parallel nfet stack, e.g nor3 gate, to propagate low overshoot noise from the primary input A0 to the output, case4 in Fig. 5, has all inputs A0, A1 and A2 switching (SOI methodology step3). Low overshoot noise propagation curves for nor3 are shown in Fig. 5 and case4 has the worst low overshoot noise propagation.

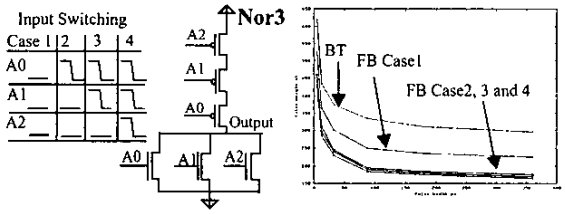


Figure 5. Parallel Stack Nor3

AOI circuits have parallel stacks of more than one device in series, as shown in Fig. 6. Here with case3 input switching there could be BJT leakage across the nfet gate controlled by input B0. This BJT noise is calculated separately and superimposed on the worst case propagated noise to get the total propagated noise as demonstrated by the spice simulation in Fig. 7. The noise propagation curves for the AOI stack are shown in Fig. 6. The BJT leakage with propagated noise combination (case3) is the worst low overshoot noise propagation curve (methodology step4).

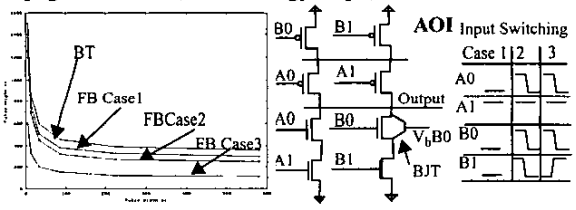


Figure 6. Parallel and Series Stack AOI

Circuits more complex than considered here would require more complex analysis as illustrated by the multiplexer and latch circuits in the following sections.

1.2. Multiplexers

For a multiplexer Fig. 8, propagated noise due to noise on data inputs is similar to noise propagation through a buffer and as discussed for series/parallel stacks, the worst case low overshoot noise propagation is when all datain have switching history. Noise propagation curves are shown in Fig. 9, case3 has the worst low overshoot noise propagation curve.

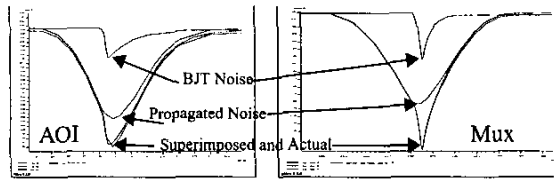


Figure 7. AOI and Mux BJT N

For noise propagation due to noise on a select signal, sel1, one other select signal(sel0) would require switching history such that the output of the mux is always driven by a datain inputs, D0 or D1. Also D2 can have a switching history resulting in BJT leakage through pass gate PG2 which is calculated separately and added to select propagated noise. Fig. 7 demonstrates the additive property of the BJT noise with select propagated noise. Fig. 9 illustrates select noise propagation curves for the mux. Maximum noise is propagated with switching history on primary select input, at least one other select input and datain inputs resulting in BJT leakage.

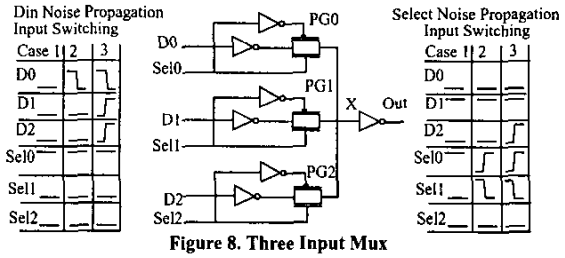


Figure 8. Three Input Mux

2. Noise injection

For calculating the injected noise, the victim driver is modeled as a linear resistance to ground (for an nfet, rail voltage for pfet). A net (victim) driven by a driver is held to logic low through this resistance, called holding resistance (holdR). All nets with significant coupling capacitances to the victim nets are considered aggressors. Noise contributions are individually calculated for each aggressor and all such contributions superimposed to get the worst case noise injected on the victim.

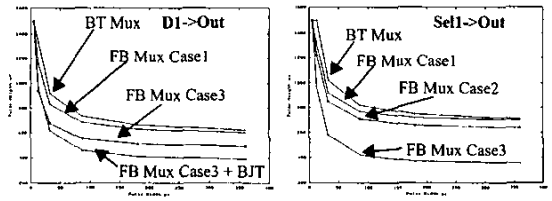
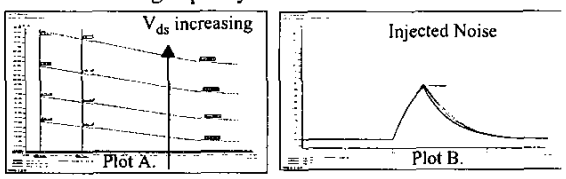


Figure 9. Mux Propagated Noise Curves

The holding resistance is calculated based on the worst case input state of the driver circuit. In SOI, in addition to the input states, their switching history is also relevant. The body voltage of the device varies with the switching history and the state of the input. The variation in the body voltage translates to threshold voltage variations which would affect its current sinking capacity.



cted Noise and

Fig. 10, plotA shows device body voltage for an nfet on x-axis and holdR on y-axis. HoldR vs. body voltage curves are plotted for different drain to source (Vds) voltage values. For an nfet with an injected noise, i.e. Vds of 400mV, body voltage variation from 100mV to 200mV would change the device holdR by 10Ohm. These small variations in holding resistance do not affect the injected noise significantly as illustrated by Fig. 10, plot B. It shows injected noise on a victim net from spice simulations held by an SOI driver with switching history at its inputs and without input switching history. As expected the injected noise is not affected by holdR variations due to input switching activity.

3. Noise Failure Criterion

The injected noise is propagated through the gates in a logic path to a latch and if this noise pulse causes the latch to change its state it is considered a *noise functional fail.*

Consider a latch shown in Fig. 11, latch state can alter from noise on data input, din or clock signal, clk. The amount of noise on latch inputs altering the latch state is dependent on latch input switching history and an additional variable, latch *state switching history.* Latch state switching history is defined as latch storage node switching activity before the noise event on its inputs. Fig. 11 illustrates the input and latchnode switching cases considered for din and clk noise rejection calculations.

For din low overshoot noise rejection, with clock at logic high the latch is transparent and din to latchnode path is equivalent to an inverter, Fig. 11. Based on the noise propagation methodology in Sec. 1, maximum noise propagation would occur if din has switching history. Adding switching history to clock signal can either not effect the latch state, case2 or it could cause state switching history, case3. Comparing the body terminal of nfet ndin in Fig. 11 for case2 and case3, it is at a higher potential in case3 than in case2. Fig. 12 illustrates din to latchnode noise rejection curves. It

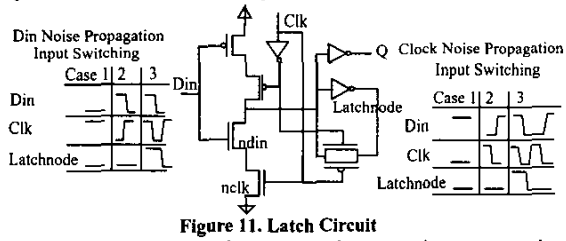


Figure 11. Latch Circuit

can be seen that case3 results in worst case low overshoot noise rejection curve.

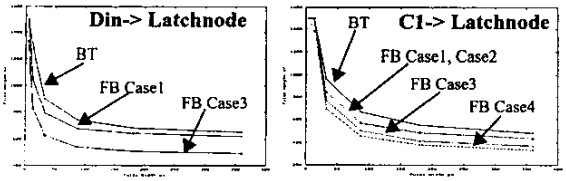


Figure 12. Latch Propagated Noise Curves

Similarly, for clock low overshoot noise rejection, clock to latchnode path is similar to select to dout path in a mux, Sec. 1.2, and maximum noise propagation would occur if clock has switching history. Adding din switching history would cause the latch state switching history, case3. Fig. 12 illustrates the clock noise rejection curves, case3 results in worst case noise rejection curve. High undershoot noise cases are analogous and can be similarly analyzed.

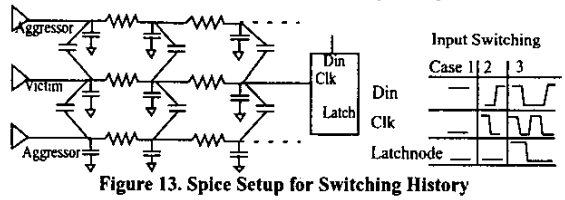


Figure 13. Spice Setup for Switching History

Results

The proposed SOI methodology was implemented in an industrial noise analysis tool(5). To test the accuracy of the proposed approach, we compared the noise analysis using the pre characterized noise propagation tables (NPT) with SPICE simulation, as shown in Table 1. In all cases the error was below 10%, and was largely due to run time data interpolation of data values in propagation tables, which can be further reduced by increasing the number of table entries.

Table 1. SOI and Spice Results for Select Nets

Net	SOI Noise Analysis	Spice	Error (%)
1	228mV	234mV	3%
2	252mV	230mV	9%
3	232mV	220mV	5%

We also studied the impact of different switching histories for a net using SPICE simulation. As shown in Fig. 13 the circuit used has aggressor nets injecting noise on a victim latch clock input which can have switching history as shown. Simulations were done with bulk and SOI circuits. The simulation results are shown in Fig. 14. Injected noise is the same in all cases as expected since the holding resistance does not change significantly. The propagated noise from clock input to latchnode increases from bulk technology to SOI technology. For SOI technology, including the input switching history and the latch state switching history increases the propagated noise sufficiently to change the state of the latch causing a failure.

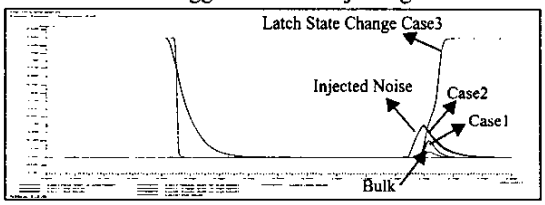


Figure 14. Latch Failure Spice Simulations

Finally, the SOI noise analysis tool was tested on an industrial microprocessor. The noise analysis was performed for a comparable bulk technology, SOI technology with traditional noise analysis and SOI technology with the proposed noise methodology. We show the number of noise failures in the three cases in Table 2, the traditional methodology reports only 44% of the total fails predicted by the new methodology. In addition only 65% of the nets above a certain noise threshold are reported by the traditional methodology. Also note that the comparable bulk technology has 90% less fails compared to SOI.

Table 2. Noise Analysis Results

Total Nets=2466	Bulk	SOI with no Switching	SOI with Switching
# Nets exceeding 50mV noise height	130	391	602
# Latch nets Failing	28	128	290

Conclusions

In this paper we demonstrated the importance of considering input switching history for noise analysis in SOI technology based designs. We show that SOI is more susceptible to noise due to smaller junction capacitance, floating body voltage and parasitic BJT leakage. We show that these effects have significant effects on propagated noise, and latching of noise which can lead to a failure otherwise not accounted for with current noise analysis tools. We propose an efficient methodology for performing a PD-SOI aware noise analysis and demonstrate results on industrial circuit.

References

(1) M. M. Pelella, et. al., "Hysteresis in floating-body PD/SOI CMOS circuits", *VLSI-TSA*, pp 278-281, 1999.

(2) A. Marshall, S. Natarajan, "PD-SOI and FD-SOI: A comparison of Circuit Performance", *ICECS*,Vol. 1, pp 25-28, 2002.

(3) C. Chuang, P. Lu, C. J. Anderson, "SOI for Digital CMOS VLSI: Design Considerations and Advances", *Proc. of IEEE*, pp 689-720, Vol 86, No. 4, April 1998.

(4) P. Lu, C. Chuang, J. Ji, et al, "Floating-Body Effects in Partially Depleted SOI CMOS Circuits", *IEEE JSSC*, pp 1241-1253, August 1997.

(5) R.Levy et.al., "ClariNet: A noise analysis tool for deep submicron design", *DAC*, pp233-238, 2000.

(6) S. C. Chan, K. L. Shepard, D. Kim, "Static Noise Analysis for Digital Integrated Circuits in Partially Depleted Silicon-On-Insulator Technology", pp. 916-927, *IEEE TCAD*, Vol. 21, No. 8, Aug. 2002.

(7) D. Bearden, "SOI design experiences with motorola's high-performance processors", *IEEE Int. SOI Conf.*, pp 6-9, Oct. 7-10, 2002.