CROSSTALK NOISE ESTIMATION USING EFFECTIVE COUPLING CAPACITANCE

Li Ding, Pinaki Mazumder, and David Blaauw

Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, MI 48109, USA

ABSTRACT

This paper describes an accurate and efficient method to estimate the crosstalk noise caused by multiple aggressor nets. Traditionally, the noise injected by each individual aggressor net is computed while the coupling capacitances from the victim net to non-switching aggressor nets are grounded. This approach, however, can significantly underestimate the maximum noise voltage. We therefore propose a more accurate approach where the noise generated by an aggressor is calculated while each quiet aggressors is replaced with an *effective* load capacitor, the value of which is obtained by multiplying the coupling capacitance with a *load factor*. A formula is derived to calculate the load factor based on parameters of the aggressor, the coupling capacitance and the effective slew rate of the victim net. Using HSPICE simulation, we demonstrate that the proposed approach results in an average error of 1% and 3σ error of 9%, while the traditional approach that used grounded coupling capacitors consistently underestimates the actual noise voltage and has an average error of 9% and 3σ error of 42%. Based on the new reduction method, a crosstalk noise estimation flow is proposed and is shown to produce promising results.

1. INTRODUCTION

Crosstalk noise between signal wires has become a prominent source of failures in high-speed VLSI systems [1]-[3]. This is especially the case in deep submicron circuit designs due to the aggressive interconnect scaling in the lateral dimensions with relatively unchanged vertical dimensions. Therefore, accurate crosstalk noise estimation in early stages of circuit design is pivotal to ensure the reliable operation of deep submicron VLSI circuits.

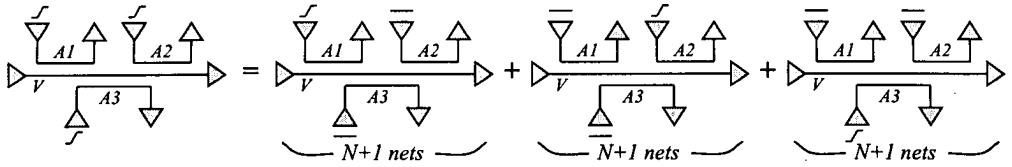
Crosstalk affects circuit behavior in two ways. First, when aggressor nets switch simultaneously with the victim net, the gate delay of the victim net is affected. Second, if the victim net is quiet, the switching of aggressors may results in voltage glitches on the victim net, possibly causing a functional signal integrity failure. In this paper, we focus on the latter problem.

The coupling capacitance from neighboring wires has become comparable to, if not more prominent than, the ground capacitance of a net. This has made it necessary that a victim net is analyzed together with all its coupled aggressor nets. However, it is not uncommon to have tens of thousands of long wires in a large design, where each net has hundreds of aggressor nets. Proper alignment of the switching time for all aggressors in order to generate the maximum crosstalk noise is very time consuming. A common approach uses the superposition law to estimate the maximum crosstalk noise [2], [4], [5]. In this approach, the complete, coupled network is simulated once for each aggressor driver, while all other aggressor drivers are held quiet. To compute the worst-case crosstalk noise of an N-aggressor system, it is therefore necessary to calculate the crosstalk noise of an N+1-net system for N times, as shown in Figure 1(a). This becomes very inefficient when the number of aggressors is large.

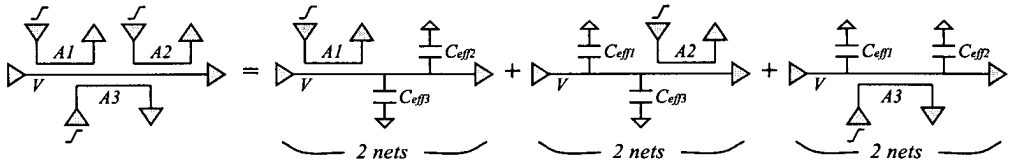
To improve efficiency, previous works [4]-[7] assume either explicitly or implicitly that coupling capacitances from the victim net to non-switching aggressor nets are grounded. This reduces the network from N+1 nets to only two nets. Therefore, the maximum crosstalk noise can be calculated in linear time with respect to the number of aggressors N. However, since during superposition the quiet aggressor nets follow the victim net waveform to a certain extent, their effective load capacitance is always less than the coupling capacitance value. Note that crosstalk noise decreases as the total effective load capacitance at the victim net increases. By using grounded coupling capacitance C_X, these methods have therefore improved the efficiency of the analysis at the cost of significantly *underestimating* the crosstalk noise.

In this paper, we propose a new approach which maintains the efficiency of the analysis, but improves the accuracy. Instead of grounding the coupling capacitors, we replace them with an *effective* load capacitor, as shown in Figure 1(b). The value of the effective capacitance is obtained by multiplying the coupling capacitance with a *load factor*. A formula is derived to calculate the load factor using pa-

This work was supported in part by the Office of Naval Research and by Semiconductor Research Corporation under contract 959.001.



(a) Basic superposition



(b) Proposed reduction method

Figure 1: Comparison of basic superposition and proposed reduction method. (Drivers and receivers are modeled as resistors and capacitors, respectively. $N = 3$ in the illustration.)

rameters of the aggressor net, the coupling capacitance and the effective slew rate of the victim net. We present results that demonstrate the accuracy of the proposed method and compare its effectiveness with the traditional approach.

The remainder of this paper is organized as follows. In Section 2, we derive the equation for the load factor. In Section 3, we present the overall noise estimation methodology and present results. In Section 4, we draw our conclusions.

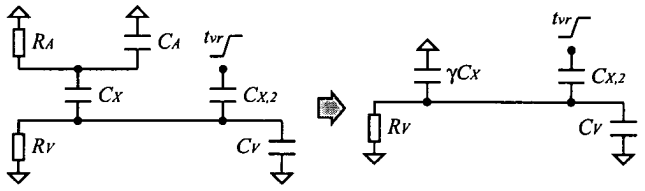


Figure 2: Crosstalk circuit for load factor analysis.

2. EFFECTIVE COUPLING CAPACITANCE OF QUIET AGGRESSORS

In this section, we will derive the formula to estimate the load factor γ of an aggressor net, based on the circuit shown in Figure 2. For simplicity of presentation, interconnect resistances are neglected. In Section 3, we will extend the formula to include interconnect resistances and incorporate it into a simple crosstalk noise model.

We first study the upper and lower bounds of γ. When the effective resistance of a quiet aggressor R_A approaches zero, we can consider the aggressor node as ground. Therefore, the effective load capacitance is the coupling capacitance $C_{MAX} = C_X$ and $\gamma = 1$. On the other hand, as R_A approaches infinity, the aggressor node floats and the coupling point (on the victim net) is connected to the ground through two series capacitors C_X and C_A. Therefore, the effective load capacitance approaches $C_{MIN} = C_A C_X/(C_A + C_X)$ and $\gamma = C_A/(C_A + C_X)$. For a realistic R_A value, the effective load capacitance is somewhere between these two bounds.

The current drawn from the victim node to an aggressor node is

$$C_X\left(\frac{dV_V(t)}{dt} - \frac{dV_A(t)}{dt}\right).$$

Therefore, our task is to find a constant γ such that

$$\gamma C_X \frac{dV_V(t)}{dt} \simeq C_X\left(\frac{dV_V(t)}{dt} - \frac{dV_A(t)}{dt}\right). \quad (1)$$

Kirchoff's current equation at the quiet aggressor node is

$$(C_A + C_X)\frac{dV_A(t)}{dt} + \frac{V_A(t)}{R_A} = C_X \frac{dV_V(t)}{dt}. \quad (2)$$

For a normalized ramp input at the victim node $V_V(t) = t/t_r$, $0 \le t \le t_r$, the above equation simplifies to

$$(C_A + C_X)\frac{dV_A(t)}{dt} + \frac{V_A(t)}{R_A} = \frac{C_X}{t_r}, \quad (3)$$

Solving the differential equation with the initial condition that $V_A(0) = 0$, we obtain the following formula

$$V_A(t) = \frac{R_A C_X}{t_r}\left(1 - e^{-\frac{t}{R_A(C_A+C_X)}}\right). \quad (4)$$

The averaged γ value during the input rising period can be calculated by integrating (1) from 0 to t_r. Use initial and final conditions, we obtain the following equation after simplification

$$\gamma \simeq 1 - V_A(t_r). \quad (5)$$

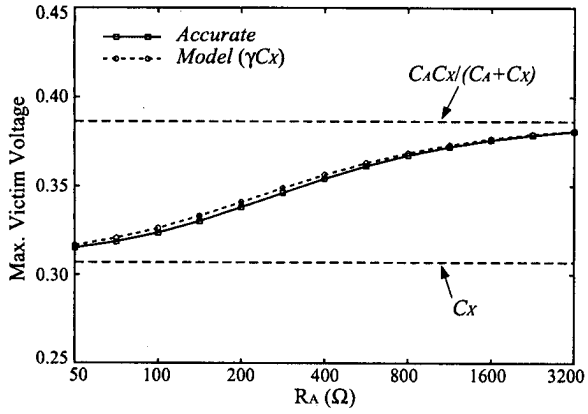


Figure 3: Comparison of the reduced circuit with original circuit. C_A=100 fF, C_X=200 fF, $C_{X,2}$=200 fF, R_V=1000 Ω, C_V=200 fF, and t_r=100 ps.

The load factor γ is obtained by combining (4) and (5)

$$\gamma = 1 - \frac{t_X}{t_r}\left(1 - e^{-\frac{t_r}{t_A}}\right), \qquad (6)$$

where

$$t_X = R_A C_X, \quad t_A = R_A(C_A + C_X).$$

It can be shown that the effective coupling capacitance C_{eff} calculated by multiplying C_X with the γ value obtained in (6) approaches C_X when $R_A \rightarrow 0$ and that $C_{eff} \rightarrow C_A C_X/(C_A + C_X)$ as $R_A \rightarrow \infty$.

Figure 3 compares the reduced circuit with the original one using typical parameters. The maximum crosstalk noise rises when R_A increases. The reduced model has a maximum error of only 1% in the entire R_A range shown in the figure. As a comparison, the maximum possible error using either C_X or $C_A C_X/(C_A + C_X)$ as the effective capacitance is over 25%.

The proposed effective coupling capacitance method was tested on 5000 random test circuits using the following parameter ranges. The capacitances range from 20 fF to 400 fF, the effective resistances range from 50 Ω to 2000 Ω, and the rise time of the aggressor ranges from 30 ps to 500 ps. Figure 4 illustrates the relative errors for the test circuits using the three different effective coupling capacitances. It is quite clear that using C_X or $C_A C_X/(C_A + C_X)$ as capacitive load will overestimate or underestimate the crosstalk noise, respectively. More quantitatively, the average errors are 9.0% and 6.0% and the 3σ errors are 42% and 43%, respectively. In contrast, using the proposed formula, we have an average error of only 1.0% and a 3σ error of 9%. Furthermore, the formula slightly overestimate the crosstalk noise, which is usually more desirable.

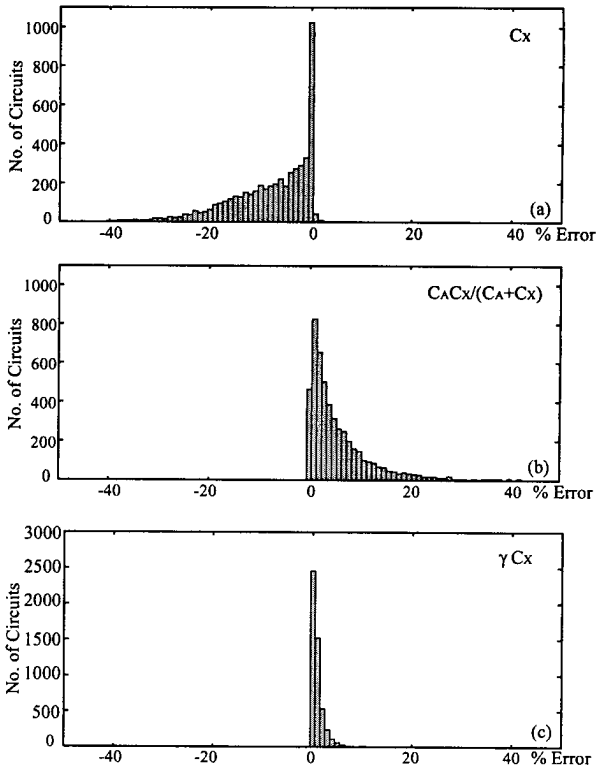


Figure 4: Simulation results of 5000 random circuits.

3. CROSSTALK NOISE ESTIMATION METHODOLOGY

Our crosstalk noise model for the single aggressor problem, as shown in Figure 5, is an extension to the 2-π model proposed in [7]. Here both the victim net and aggressor nets are modeled as two π-type circuits so that the location of the capacitive coupling can be correctly modeled.

It is quite straightforward to calculate the circuit parameters of the proposed model. Taking the victim net as an example, node 2 is the center of the coupling region, which divides the entire victim wire into two segments. R_{VL} and R_{VR} are the lumped resistances of the left and the right segments, respectively. C_{VL} is half the wire capacitance of the left segment C_{left} plus the driver output diffusion capacitance. C_{VR} is the sum of the load capacitance and half the value of the wire capacitance of the right segment C_{right}. Finally, C_{VM} is $(C_{left} + C_{right})/2$, which is half the total wire capacitance. The aggressor net can be treated the same way.

The load factor formula derived in Section 2 does not consider interconnect resistance. However, it can be easily extended to calculate the load factor of a quiet aggressor net modeled by the shown 2-π model. By matching the lower order moments of the aggressor at node *1*, we obtain

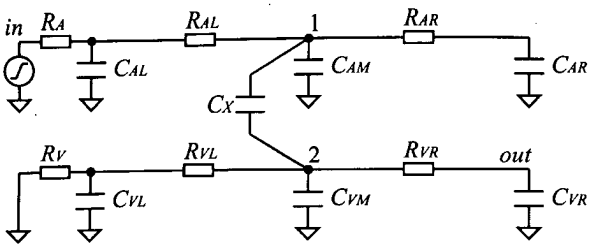


Figure 5: Single aggressor crosstalk noise model.

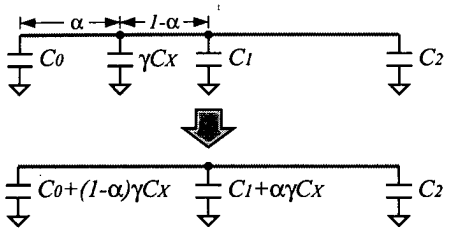


Figure 6: Incorporating effective coupling capacitance into 2-π model.

an equivalent aggressor circuit without interconnect resistance with the following parameters

$$R_A^* = R_A + R_{AL}, \quad (7)$$

$$C_A^* = (\frac{R_A}{R_A + R_{AL}})^2 C_{AL} + C_{AM} + C_{AR}. \quad (8)$$

To incorporate the effective coupling capacitances into the equivalent circuit shown in Figure 5, we distribute those capacitances among the two nearest model capacitors. Figure 6 illustrates one such transformation.

We applied the proposed crosstalk estimation methodology to two simple circuits shown in Figure 7. The interconnect parameters are based on a 0.18 μm process: the ground capacitance is 80 fF/mm, the coupling capacitance is 150 fF/mm, and the sheet resistance is 160 Ω/mm. Simulation results are shown in Table 1, where the last three columns are normalized crosstalk voltages of the original circuit, the reduced circuit using C_X, and the reduced circuit using γC_X, respectively. Relative errors are listed in parenthesis. The proposed method yields a very small error in all cases.

4. CONCLUSION

A novel method to speedup crosstalk noise estimation by reducing quiet aggressor nets to effective coupling capacitors is proposed in this paper. A formula to calculate the effective capacitances is derived and verified using HSPICE simulation. The reduction method is incorporated into the

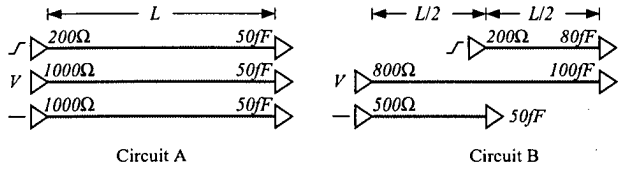


Figure 7: Example circuits.

Table 1: Simulated results of example circuits

Ckt	L (mm)	V_0	V_{C_X} (Err%)	$V_{\gamma C_X}$ (Err%)
A	0.5	0.229	0.214 (-6.6)	0.232 (1.3)
	1.0	0.272	0.247 (-9.2)	0.278 (2.2)
	2.0	0.292	0.260 (-11.0)	0.300 (2.7)
B	1.0	0.168	0.164 (-2.4)	0.170 (1.2)
	2.0	0.221	0.210 (-5.0)	0.223 (0.9)
	4.0	0.271	0.254 (-6.3)	0.270 (-0.4)

2-π model based crosstalk estimation analysis flow. Experiments have show that the proposed reduction method consistently yields superior results.

5. REFERENCES

[1] K. L. Shepard and V. Narayanan, "Noise in Deep Submicron Digital Design," *IEEE International Conference on Computer-Aided Design*, pp. 524-531, Nov. 1996.

[2] A. Devgan, "Efficient Coupled Noise Estimation for On-Chip Interconnects," *IEEE International Conference on Computer-Aided Design*, pp. 147-151, Nov. 1997.

[3] M. Kuhlmann, S. S. Sapatnekar, and K. K. Parhi, "Efficient Crosstalk Estimation," *IEEE International Conference on Computer Design*, pp. 266-272, 1999.

[4] A. Vittal and M. Marek-Sadowska, "Crosstalk Reduction for VLSI," *IEEE Transactions on Computer-Aided Design og Integrated Circuits and Systems*, vol. 16, no. 3, pp. 290-297, Mar. 1997.

[5] R. Levy, D. Blaauw, G. Braca, *et al.*, "ClariNet: A Noise Analysis Tool for Deep Submicron Design," *Design Automation Conference*, pp. 233-238, June 2000.

[6] P. Chen and K. Keutzer, "Towards True Crosstalk Noise Analysis," *IEEE International Conference on Computer-Aided Design*, pp. 132-137, Nov. 1999.

[7] J. Cong, D. Z. Pan, and P. V. Srinivas, "Improved Crosstalk Modeling for Noise Contrained Interconnect Optimization," *Asia and South Pacific Design Automation Conference*, pp. 373-378, 2001.

[8] A. Vittal, L. H. Chen, M. Marek-Sadowska, *et al.*, "Crosstalk in VLSI Interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, no. 12, pp. 1817-1824, Dec. 1999.