A Low Ripple Switched-Capacitor Voltage Regulator Using Flying Capacitance Dithering

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Abstract—In this work, a switched-capacitor voltage regulator (SCVR) that dithers flying capacitance to reduce output voltage ripple is presented, and the benefits of such ripple reduction are investigated. In the proposed technique, SC converters are designed to run at the maximum available frequency, and the flying capacitance for different phases is adjusted according to load current change through comparators and a digital controller. The proposed technique is demonstrated in a 65 nm test chip consisting of a 40-phase SCVR with 4b capacitance modulation (CM) and a 2:1 conversion ratio. On-chip circuits for ripple measurement and load performance monitoring were included to accurately assess the magnitude and impact of ripple reduction. Measurement results show that at a 2.3 V input, an on-chip ripple magnitude of 6–16 mV at 1 V output is achieved for 11–142 mA load. Peak efficiency is 70.8% at a power density of 0.187 W/mm².

Index Terms—Dithered-capacitance modulation (DCM), flying capacitance dithering, multi-phase interleaving, on-chip ripple measurement, On-chip voltage regulator, ripple reduction, switched-capacitor (SC) DC–DC converter.

I. INTRODUCTION

7 OLTAGE regulation using on-chip step-down DC-DC converters provide several important benefits, including the reduction of package input current to mitigate IR drops and Ldi/dt droop, faster load response, and per-block dynamic voltage scaling (DVS) [1], [2] for energy-efficient power management. Traditionally, linear regulators or buck converters have been proposed for on-chip step-down voltage regulation. However, linear regulators exhibit low-conversion efficiency for practical step-down ratios, as they are limited by the ratio of the output to input voltages. On the other hand, buck converters can exhibit improved efficiency, but depend strongly upon the development of very high-Q on-chip inductors, which generally require new magnetic layers. Switched-capacitor (SC) DC-DC converters, which utilize capacitors for voltage conversion, can be fully integrated on-chip while achieving high-conversion efficiency and have thus recently gained in popularity for on-chip regulation [3]–[13]. In an SC converter with a 2:1

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conversion ratio, the flying capacitance is switched periodically between input/output and output/ground during the two phases of operation. Upon transitions between phases, charge from the flying capacitor is injected into the voltage output, which results in output voltage ripple. To prevent V_{\min} failures in the load due to this voltage ripple, additional voltage margin is required, which leads to tradeoffs in performance and power efficiency. A conventional approach to reduce ripple in SC converter is multiphase interleaving, an example of which is shown in Fig. 1 for two-phase interleaving. The open-loop ripple magnitude with N_{PH} -phase interleaving can be expressed as

$$V_r = \frac{I_L \times T_{\rm SC}}{N_{\rm PH} \times C_{\rm tot}} = \frac{I_L}{F_{\rm SC} \times N_{\rm PH} \times C_{\rm tot}} \tag{1}$$

where I_L is the load current, T_{SC} is the switching period ($F_{SC} = 1/T_{SC}$), N_{PH} is the number of interleaved phases, and C_{tot} is the flying capacitance plus any additional ac-equivalent decoupling capacitance seen at the output.

However, (1) is valid only when the SC converter operates in open loop, where the output voltage is not regulated to a target voltage in response to load current or input voltage changes. In prior SC converter designs, many closed-loop output voltage-regulation techniques with phase interleaving have been introduced, including single-boundary multiphase control (SB-MC), multiphase pulse frequency modulation (PFM), digital capacitance modulation (CM), and conversion ratio adjustment [3]–[10]. However, most of these efforts do not address the output voltage ripple issue in SC converters, particularly as the output ripple magnitude in SB-MC and PFM schemes can unfortunately be even larger than that in open-loop operation.

Fig. 2(a) shows an example of an SC converter with PFM and 10-phase interleaving. In a PFM design, a phase generator creates clocks of $N_{\rm PH}$ phases with frequency of up to $F_{\rm CMP}/N_{\rm PH}$, where $F_{\rm CMP}$ is the comparator frequency and $N_{\rm PH}$ is the number of interleaved phases [e.g., a 1 GHz can generate 10-phase clocks with frequency up to 100 MHz as shown in Fig. 2(a)]. PFM toggles the clocks in a round-robin fashion on-demand when the output voltage ($V_{\rm out}$) falls below the target voltage ($V_{\rm target}$); thus, frequency of the 10-phase clocks vary depending on load current. This results in ripple due to both excessive charge transfer and the inherent voltage drop below $V_{\rm target}$ as illustrated in Fig. 3(a).

There has been work on output ripple reduction in SC converters [12], [13], but with control techniques external to the primary regulation loop. In [9], the flying capacitance is modulated for ripple mitigation with the single-bound hysteretic

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 $C_{fly} \xrightarrow{V_{in}} B \xrightarrow{V_{out}} A \xrightarrow{V_{in}} C_{fly} \xrightarrow{V_{out,AV}} V_{out,AV} \xrightarrow{V_{Nu}(No-load output voltage level) = V_{in}/2} V_{out,AV} \xrightarrow{V_{r}(ripple) = (I,X T_{sc})/(N_{PIX} X_{Cort})} \xrightarrow{V_{r}(ripple) = (I,X T_{sc})/(N_{PIX} X_{Cort})}$

Fig. 1. Schematic of a 2:1 SC converter with two-phase interleaving (left), and waveform of output voltage (right).

controller proposed in [3]. However, in addition to inheriting limitations from SB-MC, this work adjusts the number of phases for CM, where the number of phases must be reduced to achieve a small flying capacitance, which can actually degrade output ripple. As an alternative approach, a hybrid converter was proposed in [18], where SC converter and linear regulator were connected in series. However, this approach results in area increase due to separate load capacitors required at output of linear regulator, and efficiency degradation due to linear regulator dropout voltage. Furthermore, in case of an SC converter with phase-interleaving and high load current, ripple with very high frequency > 1GHz can occur, and good PSRR of linear regulator at such a high frequency is required, resulting in design complication and power consumption overhead.

To minimize ripple in closed-loop SC converters, this work proposes dithered-CM (DCM), in which the flying capacitance is adjusted on-demand with a fixed frequency used for the SC converter. Clocks with a large number of phases are generated using a delay-locked loop (DLL), so significant phaseinterleaving can be used to maximize temporal distribution of the flying capacitance charge transfer [17].

II. PROPOSED TECHNIQUE: DCM

A. On-Demand CM

The operation and output voltage waveforms for the proposed on-demand CM scheme are illustrated in Figs. 2–4 as compared with traditional PFM schemes. On-demand CM triggers SC converters at every clock edge, but changing the size of flying capacitor on a cycle-by-cycle basis allows modulation of the amount of the transferred charge. By splitting the SC into parallel structures with binary-sized flying capacitors, a sufficient range of CM can be achieved.

As shown in Fig. 2(b), in the proposed on-demand CM scheme, a digital controller finds the required flying capacitance (C_{REQ}) to be switched at a given load current. With the flying capacitance quantized to a unit capacitance of C_{LSB} , there must exist an integer M such that $M \times C_{\text{LSB}} < C_{\text{REQ}} \leq (M+1) \times C_{\text{LSB}}$, where $0 \leq M \leq C_{\text{MAX}}/C_{\text{LSB}}$ and C_{MAX} is the maximum flying capacitance assigned to a phase. Thus, the open-loop voltage level at flying capacitance $C_{\text{FLY}} = (M+1) \times C_{\text{LSB}}$ and $C_{\text{FLY}} = M \times C_{\text{LSB}}$ are above and below V_{target} , respectively, as illustrated in Fig. 3. For both cases, open-loop ripple is in accordance with (1) and not affected by the control scheme. Fig. 3 shows that PFM with a fixed flying capacitance degrades ripple characteristics as compared with the open-loop ripple when the load current is less than its maximum value, due to excessive charge transfer. However, with on-demand CM, by switching $(M + 1) \times C_{\text{LSB}}$ when $V_{\text{out}} < V_{\text{target}}$ and $M \times C_{\text{LSB}}$ when $V_{\text{out}} > V_{\text{target}}$, V_{out} , regulation can be achieved with low ripple.

Fig. 4 shows a comparison of the proposed scheme with PFM for 1/3 of the maximum load current. In PFM, clock pulses are generated on-demand and the full C_{FLY} is switched each time a clock pulse is generated. To source 1/3 the maximum load current, PFM will generate a clock pulse every third cycle (in Fig. 4, at T1 and T4 across six clock cycles). However, the full C_{FLY} switching followed by zero C_{FLY} switching results in high ripple. By contrast, on-demand CM sets $5 \times C_{LSB}$ at time T0, which results in 5/16 of maximum charge transfer in that cycle under assumption that the maximum flying capacitor available in an SC converter is $16 \times C_{\text{LSB}}$. Since 5/16 < 1/3, the output voltage drops slightly and falls below the target voltage, adjusting on-demand CM to $6 \times C_{\text{LSB}}$. At T1, the transferred charge increases to 6/16 of maximum, increasing the output voltage. Since the output voltage now exceeds the threshold, on-demand CM then switches back to $5 \times C_{\text{LSB}}$ for T2 and T3, creating a repeating pattern every three cycles with an average charge transfer of $1/3 \times 6/16 + 2/3 \times 5/16 = 1/3$ the maximum charge, which corresponds to flying capacitance of $5.33 \times C_{\text{LSB}}$. Since the difference between actual and ideal flying capacitance is always less than $1 \times C_{\text{LSB}}$, the charge transfer is kept largely proportional to the load current, resulting in low output ripple.

B. Dithered-CM

In on-demand CM, the ripple is induced by the C_{LSB} quantization of C_{FLY} . To further minimize the ripple beyond that, a dithering-like feature is proposed to obtain the effective $C_{\rm FLY}$ with finer granularity than C_{LSB} . Fig. 5 shows an example where C_{FLY} of $5.2 \times C_{\text{LSB}}$ and $5.4 \times C_{\text{LSB}}$ are used for switching instead of $5 \times C_{\text{LSB}}$ and $6 \times C_{\text{LSB}}$. Resolution smaller than discrete C_{LSB} values can be conceptually obtained by averaging $5 \times C_{\rm LSB}$ and $6 \times C_{\rm LSB}$ in time. This can be realized by allowing phase resolution of the SC converter switching periods $(T_{\rm SC}/N_{\rm PH})$ smaller than clock period of the comparator $(T_{\rm CLK})$ and considering the average $C_{\rm FLY}$ during this time window as an effective $C_{\rm FLY}$. In Fig. 5, where phase resolution $(T_{\rm SC}/N_{\rm PH})$ is set as $T_{\text{CLK}}/5$, $5.2 \times C_{\text{LSB}}$ is obtained by consecutively switching $[5, 5, 6, 5, 5] \times C_{\text{LSB}}$ in T_{CLK} , and $5.4 \times C_{\text{LSB}}$ is obtained by consecutively switching $[5, 6, 5, 6, 5] \times C_{\text{LSB}}$ in T_{CLK} . This is similar to the dithering concept in an oversampled analog-todigital converter (ADC) where toggling between neighboring quantized values can be used to obtain fine resolution and good linearity [16]. We thus achieve DCM by combining this dithering feature with on-demand CM.

C. Implication of Ripple Reduction: Power Conversion Efficiency (PCE), Load Power Utilization Factor (PUF), and Effective PCE (PCE_{eff})

With the load circuit modeled as a resistor, Fig. 6 illustrates a simplified operation of an SC converter with N_{PH} -phase interleaving, where the SC converter clock period (T_{SC}) is set so that the minimum output voltage V_{\min} equals V_{ref} . Output voltage





Fig. 2. (a) Baseline scheme: pulse-frequency modulation (PFM), and (b) proposed scheme: on-demand CM.



Fig. 3. (a) Waveform of SC converter with PFM overlaid with open-loop ripple, and (b) waveform of SC converter with on-demand CM, output of which is lying between two open-loop voltage levels of $C_{FLY} = (M + 1) \times C_{LSB}$ and $M \times C_{LSB}$.



Fig. 4. Baseline scheme: PFM (top). Proposed scheme: on-demand CM. (bottom).

Fig. 5. DCM is the combination of on-demand CM and dithering-like feature.



 $C_{tot} = N_{PH} \times C_{unit}$, where $C_{tot} = total capacitance & N_{PH} = number of interleaved phases <math>C_{rem}$ (remaining capacitors that do not switch at a transition state) = $C_{tot} - 2 \times C_{unit}$

Fig. 6. Simplified operation of SC converter with $N_{\rm PH}$ -phase interleaving, resistor load (R_L) and clock period of $N_{\rm PH} \times T_{\rm trigger}$, which sets minimum peak of $V_{\rm out}$ equal to $V_{\rm ref}$, and corresponding output waveform.

ripple (V_r) can be derived using a procedure as outlined next. Output voltage (V_{out}) changes from V_{ref} to $V_{ref} + V_r$ during the phase-transition state. If C_{rem} is the remaining capacitance that does not switch during the transition state, half of the C_{rem} is connected between V_{out} and the input voltage (V_{in}) while the other half is connected between V_{out} and ground. Then, the instantaneous charge influx to the latter $C_{rem}/2$, $Q_{dc2,tr}$ is $(C_{rem}/2) \times V_r$. As shown in Fig. 6, when the state changes from phase M to phase M + 1 (transition state), the voltage across the left C_{unit} changes from $V_{in} - V_{ref}$ to $V_{ref} + V_r$, and the left C_{unit} loses charge of $Q_{f1,tr} = C_{unit} \times \{(V_{in} - V_{ref} - (V_{ref} + V_r)\} = C_{unit} \times (V_{in} - 2V_{ref} - V_r)$ in this process. After solving $Q_{dc2,tr} = Q_{f1,tr}$, we can represent the output voltage ripple as

$$V_r = \frac{2 \times (V_{\rm in} - 2V_{\rm ref})}{N_{\rm PH}} \tag{2}$$

where $N_{\rm PH}$ is the number of phases, $V_{\rm in}$ is the input voltage, and $V_{\rm ref}$ is the desired $V_{\rm min}$.

Trigger period ($T_{\text{trigger}} = T_{\text{SC}}/N_{\text{PH}}$) can be written as below because the RC time constant is $R_L C_{\text{tot}}$, and T_{trigger} is the time it takes to discharge the output node from $V_{\text{ref}} + V_r$ to V_{ref}

$$T_{\text{trigger}} = C_{\text{tot}} R_L \ln \left\{ \frac{(V_{\text{ref}} + V_r)}{V_{\text{ref}}} \right\}.$$
 (3)

Based on (2) and (3), we can quantify the power delivered to load (P_L), input power (P_{in}), and power conversion efficiency (PCE = P_L/P_{in}) by the following equations:

$$P_L = \frac{V_{\rm rms}^2}{R_L}$$
, where $V_{\rm rms}^2 = \frac{(V_{\rm ref} + V_r)^2 + (V_{\rm ref} + V_r)V_{\rm ref} + V_{\rm ref}^2}{3}$ (4)

$$P_{\rm in} = \frac{V_{\rm in}Q_{\rm in}}{T_{\rm trigger}} = \frac{V_{\rm in}}{T_{\rm trigger}} \frac{C_{\rm tot}V_r}{2}$$
(5)

Power conversion efficiency (PCE) =
$$\frac{P_L}{P_{\text{in}}} = \frac{V_{\text{rms}}^2}{R_L P_{\text{in}}}$$
. (6)

From the perspective of the digital circuit load, since the minimum output voltage (V_{\min}) level determines the maximum operating frequency, we can define a load PUF as



Fig. 7. Impact of ripple reduction in SC converter ($C_{\text{tot}} = 3.7 \text{ nF}$, $V_{\text{in}} = 2.3 \text{ V}$, $V_{\text{ref}} = 1 \text{ V}$): (a) PCE, effective PCE, load PUF versus ripple, (b) power overhead ($P_{\text{in}} - P_{\min}$) due to ripple and SC converter versus ripple.

Load power utilization factor (PUF) =
$$\frac{P_{\min}}{P_L} = \frac{V_{\min}^2}{R_L P_L}$$

= $\frac{V_{\text{ref}}^2}{R_L P_L}$. (7)

Effective PCE (PCE_{eff}) = PCE × PUF =
$$\frac{V_{\min}^2}{R_L P_{in}} = \frac{V_{ref}^2}{R_L P_{in}}$$
(8)

where P_{\min} is defined as the load power consumption when the load circuit (modeled with R_L) operates at V_{\min} . Similar concepts to PUF and P_{\min} are also discussed in [15].

Intuitively, (3)–(6) imply that PCE degrades with the reduction in V_r because a decrease in V_r results in more decrease in P_L than in P_{in} . However, as implied by (7) and (8), with the reduction in V_r , PUF is improved and P_{in} is reduced, resulting in the improvement of PCE_{eff}. Therefore, PCE_{eff} can be used as an indicator of both voltage regulation capability and PCE, while PCE cannot represent voltage regulation capability. Moreover, it is noted in (5) that the reduction in V_r attains power consumption saving.

Based on (2)-(8), the effect of ripple on PCE, PUF, and PCE_{eff} can be obtained. In Fig. 7, by setting $C_{tot} = 3.7 \text{ nF}$, $V_{\rm in} = 2.3$ V, and $V_{\rm ref} = 1$ V and assuming that $T_{\rm trigger}$ is set according to (3), PCE, PUF, and PCE_{eff} are plotted against ripple magnitude, which is governed by the number of phases $(N_{\rm PH})$. Due to a decrease in $V_{\rm rms}$, it is shown that PCE degrades with ripple reduction, but PUF is improved with smaller ripple: when ripple is reduced from 150 to 3.7 mV, PCE decreases from 93.8% to 87.1%, and PUF increases from 86.4% to 99.6%. Therefore, it is noted that PCE_{eff} is improved with ripple reduction: when ripple is reduced from 150 to 3.7 mV, PCE_{eff} is improved from 81.0% to 86.8%. In other words, input power consumption decreases with ripple reduction. For instance, as shown in Fig. 7(b), when $R_L = 7.1 \ \Omega$ (load current is approximately 141 mA), improving ripple from 150 to 3.7 mV reduces input power consumption by 11.5 mW. These results imply that the theoretically attainable PCE of SC converter can degrade with ripple reduction, but ripple reduction decreases load power consumption, thereby improving PUF and PCE_{eff}.

Phase M



Fig. 8. Normalized available flying capacitance as a function of number of interleaved phases with and without 4b CM under area constraint of $880 \times 830 \ \mu m^2$.

III. IMPLEMENTATION OF DCM

A. Selection of the Number of Interleaved Phases

The proposed DCM approach is implemented in a 40-phase SC voltage regulator (SCVR) with 4b DCM. The number of phases and the modulation resolution presents a tradeoff between voltage ripple and area utilization of capacitance. As the number of phases and modulation resolution increases, the achievable ripple reduces; however, the total capacitance is divided among a larger number of individual units, resulting in area overhead due to capacitor spacing requirements in layout and peripheral circuits. Fig. 8 shows that the available capacitance decreases as the number of interleaved phases increases under a fixed area constraint (in this case, $880 \times 830 \ \mu m^2$). To keep the area overhead below 10%, 40 phases with 4b CM was chosen, which has the same area utilization as 160-phase interleaving without CM. However, 160-phase interleaving would increase the power consumption and implementation complexity due to the required clock generation by up to $4\times$. Moreover, clocks with excessive number of phases are susceptible to variation, where the ripple reduction benefits could be diminished.

B. 40-Phase SCVR with 4b DCM

The 40-phase SCVR with 4b DCM is composed of four SC-banks as shown in Fig. 9. Each SC-bank comprises five twophase SC converter blocks with 4b DCM, and each two-phase SC converter block consists of SC converters with 4 + 1 binaryweighted flying capacitors where $C_{\text{LSB}} = 5.8$ pF to provide a discrete flying capacitance value for each SC phase as shown in Fig. 10. No explicit output capacitance is used. To ensure a fixed SCVR frequency and minimum ripple, one additional flying capacitor with C_{LSB} is always switching. The local clock generation waveform in the two-phase SC converter is illustrated in Fig. 10. Using a toggle flip-flop (TFF), a nonoverlapping clock generator, and level converters, local 95 MHz clocks are generated from the 190 MHz input clock when the input signal to



Fig. 9. Top-level diagram of 40-phase SCVR with 4b DCM.



Fig. 10. Two-phase SC converter block for 4b DCM.



Fig. 11. Operation of 40-phase SCVR with 4b DCM in steady state.

the TFF is asserted. Note that the SC converter recovers output voltage droop by dumping charge to the output node during the transition of the local clocks. A DCM controller adjusts inputs to TFFs, which is represented by CM[3:0], for CM.

As shown in Fig. 9, the 760 MHz master clock is first divided down to 190 MHz. A DLL then generates twenty 190 MHz clocks with 263 ps resolution between phases, and each of the 190 MHz clocks drives a two-phase SC converter block. Each two-phase SC converter locally generates two nonoverlapping, half-frequency clocks (95 MHz) and allows 5.2 ns between charge transfers. In total, 20 charge transfers occur in a 190 MHz clock cycle, resulting in an effective operation at 3.8 GHz.

Three comparators (C0–C2) operate off the 760 MHz master clock, generating a comparison output every five clock phases. References $V_{\text{th},p}$ and $V_{\text{th},m}$ are used to adjust CM upon load current changes, and V_{target} is used to regulate V_{out} in steady

Time



СМРР 0 СМРМ 0 СNT _M 0	0 0 0	0 1 1	0 1 2	0 1 3	0	0	1	1	1	1 0	1 0	0	0	0	0	0	0	0	0	(
CMPM 0 CNT _M 0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	(
CNT _M 0	0	1	2	3	4	5	0	•	_											
				Ľ	7	3	U	0	0	0	0	0	0	0	0	0	0	0	0	
CM 3	3	4	6	9	13	15	15	15	15	15	14	14	14	14	14	14	14	14	14	1
N _{d,reg} 1	1	1	1	1	1	5	4	3	2	1	5	5	5	5	5	5	5	5	5	
N _d 0	0	1	1	1	1	5	3	2	1	0	4	4	5	5	4	4	4	5	5	4

Fig. 12. Flowchart of DCM controller (top). Stabilization example under transient load current change (bottom).

state. The steady-state example in Fig. 11 shows CM dithering between CM[3:0] = 3.6, when CMP = 1 (cycles 1–2) and CM[3:0] = 3.4, when CMP = 0 (cycles 3–5), resulting in an average CM value of 3.48.

C. DCM Controller

Fig. 12 shows a flowchart of the DCM controller, and a table of DCM output generation and a stabilization example under transient change in load current. The DCM controller adjusts the CM level for a given load current, and CM increases with a load current increase. Five modulation signals CM0-CM4 are generated as a function of base discrete CM and output dithering value N_d , as shown in the top right part of Fig. 12. N_d is obtained from $N_{d,reg}$, base dithering level stored in registers. N_d is set $N_{d,reg} - 1$ for $V_{out} > V_{target}$, and $N_{d,reg}$ for $V_{out} < V_{target}$. In transient condition, the controller adjusts the base discrete CM and $N_{d,reg}$, and after entering steady-state, only N_d is adjusted between $N_{d, \text{reg}} - 1$ and $N_{d, \text{reg}}$ depending on V_{out} . For instance, to generate CM[3:0] = 3.6and 3.4 in Fig. 11, the controller sets the base discrete CM = 3, and $N_{d,reg} = 3$ in transient condition. In steady-state, for $V_{\text{out}} < V_{\text{target}}$, the controller sets $N_d = 3$, and it sets CM0 = 4, CM1 = 3, CM2 = 4, CM3 = 3, and CM4 = 4. For $V_{\text{out}} > V_{\text{target}}$, the controller sets $N_d = 2$, and it sets CM0 = 3, CM1 = 4, CM2 = 3, CM3 = 4, and CM4 = 3. The maximum value of N_d and $N_{d,reg}$ were set at 5. This is because (comparator clock period)/(phase resolution in switching clocks for SCVR) = $T_{\rm CMP}/(T_{\rm SC}/N_{\rm PH}) = 5$ and one SC bank has five SC converter blocks. As CM[3:0] changes between two neighboring values to regulate V_{out} close to V_{target} , limitcycle oscillation and output ripple ensue in steady-state. This locked-state of the closed loop of DCM behaves similar to



Fig. 13. Die photo and area summary.

bang bang PLL (BBPLL), in that it has inevitable limit cycles, and it cannot be analyzed in the traditional Laplace domain because of nonlinearity introduced by a 1 bit quantizer or a comparator in the loop. DCM, which is digitally controlled with a comparator, regulates V_{out} by asymptotically settling around V_{target} [19].



Fig. 14. Contour plot of measured output voltage in open-loop as a function of current density and normalized enabled capacitance when CM[3:0] = 8 - 15 (left). Normalized enabled capacitance in closed-loop versus power density when $V_{target} = 1$ V (right).



Fig. 15. On-chip ripple measuring circuit (left) and on-chip ripple measurement at load current of 11 mA (right).

Operation sequence of the controller in transient condition is as follows: upon a large load current change, if $V_{\text{out}} < V_{\text{th},m}$, then counter CNT_M is incremented and added to the base discrete CM (e.g., $CM = CM + CNT_M$). This increases the base discrete CM geometrically for each subsequent cycle with $V_{\text{out}} < V_{\text{th},m}$, and it can lead to an overshoot in the output voltage. When $V_{\text{out}} > V_{\text{th},p}$, the controller decrements the stored dithering level $N_{d,reg}$ by one in each cycle until $N_{d,reg}$ reaches zero, at which point the base discrete CM is decreased by one and $N_{d,reg}$ is reset to 5. The much stronger adjustment of C_{FLY} when $V_{\text{out}} < V_{\text{th},m}$ than when $V_{\text{out}} > V_{\text{th},p}$ minimizes the likelihood of an undershoot in favor of an overshoot. In steady state, where V_{out} lies between $V_{th,p}$ and $V_{th,m}$, only the dithering level (N_d) is adjusted. One example for transient stabilization of DCM controller is illustrated in the bottom part of Fig. 12. Finally, a shunt push-pull regulator proposed in [15] is used to mitigate undershoot and overshoot against transient load current change.

IV. MEASUREMENT RESULTS

A test chip was fabricated in a 65 nm CMOS process to compare the DCM and PFM schemes. A die photo and area summary are shown in Fig. 13. MIM and MOS capacitors are used for flying capacitors in this SCVR to achieve a total capacitance of 3.7 nF (MIM capacitors = 0.93 nF, and MOS capacitors = 2.77 nF). Due to *pn*-junction diodes formed by *p*-substrate and *n*-well, MOS capacitors have larger bottomplate parasitic capacitance compared to MIM capacitors, but they have good capacitance density. MOS and MIM capacitors have $k_{bot} = 5\%$ and $k_{bot} = 1\%$, respectively, where $k_{bot} = ratio$



Fig. 16. Periodic load current change between 11 and 48 mA with period of 2 μ s (left), and corresponding overshoot and undershoot measurement results (right).

of bottom-plate parasitic capacitance to nonparasitic capacitance, and MOS capacitors have $> 2 \times$ capacitance density in comparison to MIM capacitors. With the utilization of MOS capacitors in addition to MIM capacitors, die space can be more efficiently utilized, as MOS capacitors can be placed beneath MIM capacitors, and higher power density can be achieved.

Parameters V_{in} , V_{target} , $V_{th,m}$, and $V_{th,p}$ are set to 2.3, 1, 0.985, and 1.015 V, respectively. Fig. 14 shows the measurement results for open-loop operation and closed-loop operation of the DCM scheme. While the total capacitance is kept constant, a load current increase leads to an increase in the modulated flying capacitance for voltage regulation as expected. Open-loop measurements confirm that the adjustment of V_{target} , $V_{th,m}$, and $V_{th,p}$ enables the regulation of the output voltage to different voltage levels.

For accurate ripple measurement, we implemented an onchip monitoring circuit [14] that consists of a comparator,



Fig. 17. (a) Measured ripple magnitude versus power density for DCM and PFM, overlaid with calculated open-loop ripple, and (b) measured average output voltage (V_{out}) of DCM and PFM.

which is asynchronously clocked, and 15b counters, which record the fraction of cycles with $V_{\text{out}} < V_{\text{RMC}}$, as shown in Fig. 15. The measurement sequence is as follows:

- 1) sweep V_{RMC} (voltage at plus-terminal of comparator) for the voltage range of interest;
- 2) at each V_{RMC} , start over after resetting two counters (CNT and $\text{CNT}_{\text{REF}} = 0$);
- 3) when DONE = 1, calculate probability= $CNT/(2^{15}-1)$;
- 4) find V_{prob99} and V_{prob1} (with V_{probN} defined as voltage with probability equal to N%);
- 5) calculate ripple from the difference between V_{prob99} and V_{prob1} .

Fig. 15 shows an example plot for this on-chip ripple measurement. The probability calculated using outputs of the ripple monitor is plotted against V_{RMC} for DCM and PFM at a constant load current. DCM achieves a 6 mV ripple, compared to 140 mV for PFM at $I_L = 11$ mA. It should be noted that the PFM mode can be obtained by reconfiguring the existing DCM controller. In PFM mode, only comparator C0 is used to trigger the controller and CM0–CM4 are all set to 15 or 0, depending on the output voltage level. DCM and PFM were both measured with the same on-chip ripple monitor for comparison.

Fig. 16 shows the output voltage response in DCM to a periodic load current change between 11 and 48 mA (period = $2 \mu s$). Undershoot and overshoot voltages under these conditions were also measured with the on-chip ripple monitor. It was observed that the periodic load current change results in 65 mV undershoot and 105 mV overshoot, which are obtained by finding $V_{\rm RMC}$ with probability = 0% and 100%, respectively. The fact that the overshoot is larger than the undershoot is a direct result of the more aggressive controller response to $V_{\rm out} < V_{\rm h,m}$.

Fig. 17(a) shows the measured DCM and PFM ripple versus power density and Fig. 17(b) shows the average output voltage versus power density, both for the load current range from 11 to 142 mA. DCM ripple ranges from 6 to 16 mV and scales with load current, as expected. DCM ripple closely tracks the open-loop ripple expression $I_L/(F_{\rm SC} \times N_{\rm PH} \times C_{\rm TOT})$, and the output voltage of DCM is tightly regulated to $V_{\rm target} = 1$ V.



Fig. 18. On-chip digital load circuit performance monitor.



Fig. 19. Measured minimum peak output voltage (V_{MIN}) versus power density (left). Impact of V_{MIN} on frequency of on-chip digital load circuit performance (right).

The load performance monitor proposed in [15] was implemented in the test chip to investigate the impact of output ripple on digital load circuit performance. As shown in Fig. 18, the monitor circuit measures propagation time of a path with a voltage-controlled oscillator, the frequency of which can be observed externally. By sweeping control voltage (V_{CTRL}) and changing clock frequency until the monitor flags an error signal, the maximum frequency, or the propagation time of the path, is found. The supply voltage of the load performance monitor is connected to output voltage of the SC converter in the test chip, such that the impact of the minimum output voltage $(V_{\rm MIN})$ on the digital-load performance can be compared for DCM and PFM modes. In Fig. 19, V_{MIN} is plotted against power density for both DCM and PFM. Using the on-chip digital load performance monitor, it is found that the PFM-driven circuit exhibits 16% slower performance than DCM at large load current. Fig. 20 shows that DCM achieves a peak efficiency of 70.8% at a power density of 0.187 W/mm², which corresponds to $I_L = 142$ mA. DLL, controller, and comparators



Fig. 20. Measured efficiency versus power density.

TABLE I Power Loss Breakdown of DCM SC Converter (at $I_L = 142$ mA)

Component	Subcomponent	Power loss (mW)	Percentage(%)
Conduction loss		18.5	33.2
Switching loss		33.8	60.8
	P _{bot} of MIM-capacitors (sim.)	0.88	1.6
	P _{bot} of MOS-capacitors (sim.)	13.2	23.7
Controller, comparator, and DLL		3.3	5.9
Total		55.6	100

consume 3.3 mW. Excluding power consumption of the DLL, controller, and comparators, the SC converter itself achieves peak efficiency of 72.6%.

Table I summarizes the power loss breakdown of the implemented DCM SC converter at $I_L = 142$ mA. Main power loss is attributed to switching loss, because 1) the number of clockdriving circuits such as TFFs, level shifters, and nonoverlapping clock generators increase in proportion to the number of phase and CM and 2) switching loss due to bottom-plate parasitic capacitors of MOS capacitors is significant. To improve efficiency, the number of phases and CM could be reduced with a relaxed constraint on ripple, and switching frequency could be reduced while trading off power density. Fabrication in advanced CMOS process can also help resolve switching loss of clock driving circuits and parasitic switching loss of flying capacitors. The bottom-plate parasitic switching loss (P_{bot}) can be written as (9). If MIM capacitors of 3.7 nF had been used instead of the combination of MIM and MOS capacitors, P_{bot} can be significantly reduced with power density degradation, and peak efficiency could be improved by approximately 4%.

$$P_{\rm bot} = k_{\rm bot} C_{\rm FLY} V_{\rm sw}^2 F_{\rm sw} \tag{9}$$

where C_{FLY} = flying capacitance, and V_{sw} = swing voltage of bottom-plate parasitic capacitor.

A comparison to prior work is summarized in Fig. 21 and Table II. Fig. 21 plots peak efficiency and power density of prior works and the proposed work in a similar fashion to [13]. The dotted line in Fig. 21 indicates that peak efficiency and power density have tradeoff relation. Prior works fabricated in 65 nm process were grouped. Compared to the other 65 nm prior work, this work shows slightly lower peak efficiency because of split flying capacitors and reduced capacitance utilization per area. Moreover, if flying capacitors had not been split in this work,



Fig. 21. Comparison of peak efficiency versus power density: prior works are indicated with black square symbols, and this work is indicated with red square symbol.

TABLE II Comparison Table

Metric	[5]	[6]	[8]	This work
Technology	22 nm tri-gate	32 nm SOI	45 nm Bulk	65 nm bulk
Capacitor type	MIM	Deep Trench	MOS	MIM + MOS
Conversion ratio (M)	2:1, 3:2, 5:4, 1:1	2:1, 3:2	3:2, 2:1	2:1
Closed-loop modulation	Frequency	Frequency	Frequency (PFM), capacitance	Capacitance dithering
Comparator frequency	2 GHz	4 GHz	30 MHz	760 MHz
SC converter frequency (MHz)	≤ 250	≤ 125	≤ 30	95
Number of phases	8	16	2	40
C_{FLY}/C_{OUT}	¹ N/R/0.1 nF	16 nF/0	0.534 nF/0.7 nF	3.7 nF/0
V _{in} /V _{out}	1.23 V/0.45 ~ 1 V	1.8 V/0.7 ~ 1.1 V	1.8 V/0.8 ~ 1 V	2.3 V/1 V
Ripple measurement	Off-chip	Off-chip	Off-chip	On-chip
V _{ripple,pp}	60 mV at ≤ 88 mA	30 mV at 365 mA	50 mV at ≤ 10 mA	6 ~ 16 mV at 11 ~ 142 mA
V _{droop}	< 25 mV at 15→30 mA	94 mV at 30→365 mA	155 mV at 2→10 mA	65 mV at 11→48 mA
² Power density (ρ) (W/mm ²)	0.064	2.71	0.050	0.187
Efficiency at p (%)	68	86.4	66	70.8

¹N/R, not reported.

²Power density, reported at M = 2:1.

higher power density could have been obtained at the same peak efficiency. On-chip capacitance density directly affects power density, and parasitic capacitance affects achievable peak efficiency. As on-chip capacitance density and parasitic capacitance are determined by fabrication technology, the proposed work achieved higher power density than prior works in process with inferior technology than 65 nm, but less power density or less peak efficiency than in process with advanced technology such as deep trench capacitor, ferroelectric capacitor, and SOI technology.

V. CONCLUSION

In this work, DCM is proposed to minimize closed-loop ripple in SCVRs with multiphase interleaving. It is shown that ripple reduction improves load power utilization and effective input power conversion efficiency (PCE_{eff}), thereby reducing power consumption at a constant minimum peak output voltage (V_{\min}). An SC converter with 40-phase interleaving and 4b DCM level was implemented in 65 nm CMOS technology to achieve a ripple magnitude of 6–16 mV for load currents ranging from 11 to 142 mA as was measured with an on-chip ripple measurement circuit.

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