A Successive-Approximation Switched-Capacitor DC–DC Converter With Resolution of $V_{\rm IN}/2^N$ for a Wide Range of Input and Output Voltages

Suyoung Bang, *Student Member, IEEE*, David Blaauw, *Fellow, IEEE*, and Dennis Sylvester, *Fellow, IEEE*

***Abstract*—A fully integrated successive-approximation (SAR) switched-capacitor (SC) DC–DC converter is presented that overcomes the coarse output voltage resolution limitation of traditional SC converters. An SAR SC converter cascades multiple stages of 2:1 SC converters, and achieves a fine-grained conversion ratio resolution of $V_{\rm IN}/2^N$, where $V_{\rm IN}$ is the input voltage and N is the number of stages. As the SAR SC converter generates the output voltage through SAR, each stage of 2:1 SC converter provides a fixed voltage level, requiring minimal configuration change for regulation. Analysis shows that the SAR SC converter has a slow-switching-limit output impedance increasing proportionally to $\log_2$ (number of resolution), and switching loss of bottom-plate parasitic capacitor decreasing with the number of stages. As a test chip, an SAR SC converter with 7 b resolution is fabricated in 180 nm CMOS process and implemented by cascading 4:1 and five 2:1 two-phase interleaving SC stages. It achieves 31.25 mV voltage resolution with output voltages over 0.4 V at $V_{\rm IN} = 4$ V. Using this fine grain voltage regulation approach, line and load regulations are implemented with a feedback/feedforward controller with peak efficiency of 72% for load currents from 0 to 300 μA. The test chip occupies 1.69 mm^2 and utilizes on-chip capacitors of 2.24 nF in total.**

***Index Terms*—Fine-grained voltage generation, fully integrated power converter, on-chip voltage regulator, power management unit, successive-approximation (SAR) switched-capacitor (SC) converter, SC DC–DC converter.**

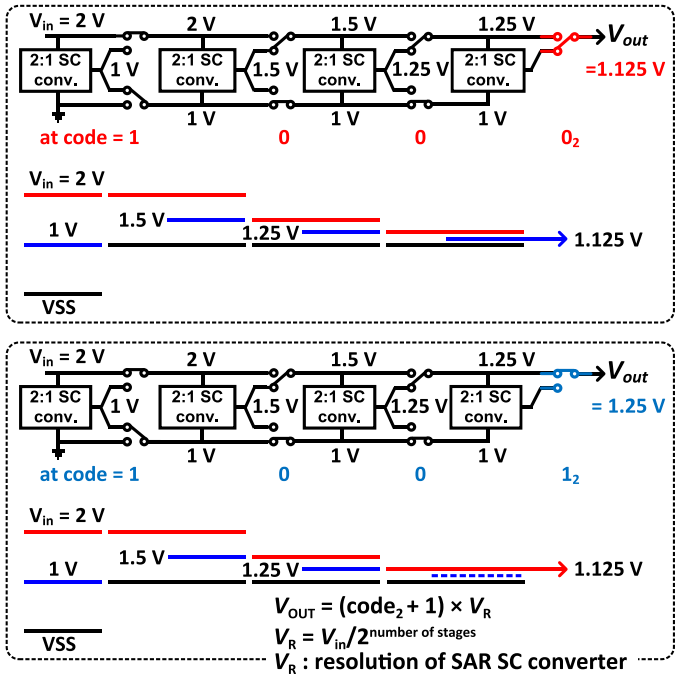

Fig. 1. Conceptual example of 4 b SAR SC DC–DC converter operation for code $= 1000_2$ (top) and 1001_2 (bottom).

I. Introduction

FULLY integrated power converters are gaining interest from designers of small-volume electronic systems by offering several benefits: reduced package overhead, reduced IR drops and Ldi/dt droops in package and PCB, and per-block dynamic voltage scaling (DVS). On-chip power converters can be employed in modern system-on-chips (SoC) and today's Internet-of-Things (IoT) devices to extend battery lifetime via energy-efficient power management while realizing a small form factor.

Switched-capacitor (SC) DC–DC converters have recently emerged as favorable candidates for on-chip power converters, thanks to CMOS process compatibility, good efficiency, and scalability of load power and frequency [1]. On the other hand, on-chip inductive power converters require high-Q inductor for good efficiency, necessitating special masks and increased manufacturing costs. A packaged bondwire-based inductive converter can offer improved quality factor, but this approach uses dedicated bondwires that require postfabrication effort [2]. Also, load power scaling in inductive converters is challenging and hence complex control and operation are required to supply low power loads [3], hurting efficiency. Moreover, linear regulators have efficiency that is directly limited by the ratio of output voltage to input voltage, making them nonideal despite their process compatibility and good power densities.

However, efficient power conversion of SC converters is performed only around discrete conversion ratios. In other words, only one pair of frequency and output voltage level offer peak efficiency at a given conversion ratio and load current. Operating points that deviate from these optimal ones result in efficiency degradation. Adding more conversion ratios in conventional SC converters can help provide greater design flexibility, but this increases implementation complexity,

Manuscript received May 14, 2015; revised September 25, 2015; accepted November 06, 2015. Date of publication January 14, 2016; date of current version January 29, 2016. This paper was approved by Associate Editor Gyu-Hyeong Cho.

The authors are with the University of Michigan, Ann Arbor, MI, 48105 USA (e-mail: suyoungb@umich.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2015.2501985

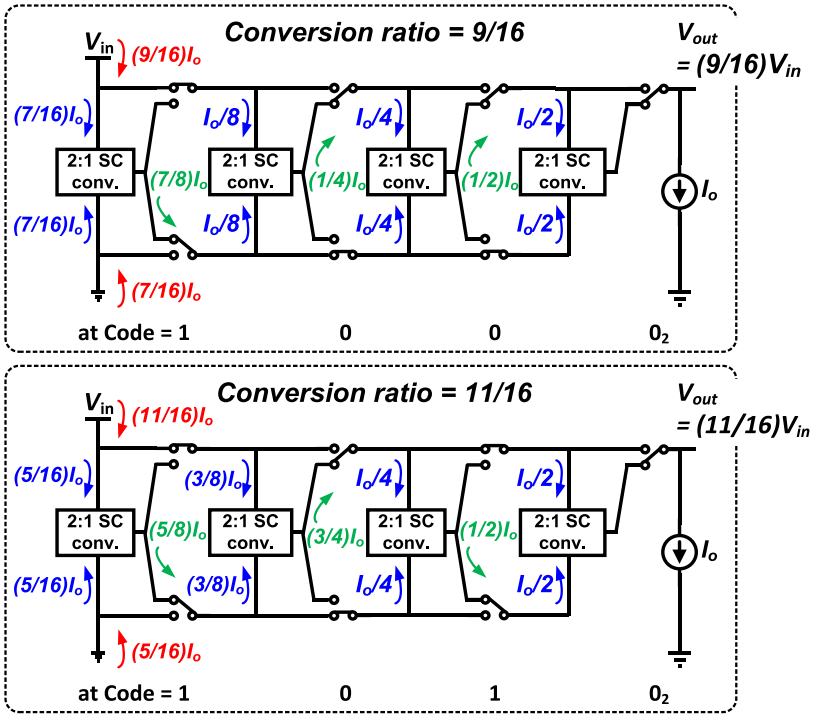

Fig. 2. Current flow of 4 b SAR SC converter for code $= 1000_2$ (top) and 1010_2 (bottom).

often leading to increased losses and degraded efficiency. For instance, series-parallel SC converters that are reconfigurable with several conversion ratios have irregular structures with additional switches, which limit their reconfigurability while also harming efficiency [4]–[11].

This paper presents a successive-approximation SC (SAR SC) DC–DC converter that provides a conversion ratio resolution of $V_{\rm IN}/2^{\rm number\ of\ stages}$ [12]. An SAR SC converter cascades multiple stages of 2:1 SC converters. The proposed SAR SC converter offers a large number of conversion ratios, and has smaller slow-switching limit impedance, or charge-sharing loss [13], and smaller switching loss due to bottom-plate parasitic capacitor than other conventional SC converters with the same number of conversion ratios. In the SAR SC converter, the 2:1 SC converter cell in each stage generates the voltage resolution set by the number of stages between the first stage and the corresponding stage regardless of conversion ratio, and a conversion ratio is successively obtained between neighboring stages. Thus, minimal change in configuration is required in case of conversion ratio adjustment.

This paper is organized as follows. In Section II, architecture of the SAR SC converter is introduced, power loss due to slow-switching limit impedance and bottom-plate parasitic switching loss are analyzed for efficiency optimization with switching frequency, and comparison against other topologies is made. In Section III, a test chip architecture and detailed implementation are presented that allows for fine output voltage control with dynamic fine-grained conversion ratio adjustment, and enable effective closed-loop load and line regulation for low power applications. In Section IV, measurement results are presented.

II. SAR SC Converter

A. Concept of SAR SC Converter

Fig. 1 describes the operating principle of the SAR SC DC–DC converter. The main idea is to cascade multiple 2:1 SC-stages using configuration switches to obtain a fine grain output voltage ($V_{\rm OUT}$). Each SC-stage takes two inputs ($V_{\rm high}$, $V_{\rm low}$) and produces an output $V_{\rm mid} = (V_{\rm high} + V_{\rm low})/2$. The high voltage of the next stage is connected to either the high or mid voltage of the previous stage. The low voltage of the next stage is connected to either the mid or low voltage of the previous stage. In the four-stage example of Fig. 1, $V_{\rm in} = 2\,{\rm V}$ is converted to $V_{\rm OUT} = 1.125\,{\rm V}$ with configuration code $= 1000_2$ and to $V_{\rm OUT} = 1.250$ with code $= 1001_2$, providing a 125 mV step under no-load condition.

With configuration code $= 1000_2$, the first-stage converter output is 1 V, representing the average of 2 and 0 V. Thus, the second stage takes 2 and 1 V as high and low voltage. The MSB is one and controls the switch configuration between the first and second stages. Hence, the mid-voltage of the second stage becomes 1.5 V. The high voltage of the third stage is connected to the mid-voltage of the second stage, and the low voltage of the third stage is connected to the low voltage of the second stage. In other words, the third stage takes 1.5 and 1 V as its high and low voltages, since the second bit is 0. As a result, the mid-voltage of the third stage becomes 1.25 V. Since the third bit is also 0, the mid-voltage of the final stage becomes 1.125 V. To generate an output of 1.125 V, the mid-voltage of the final stage is connected to the final output, and the LSB is set to 0. On the other hand, in order to make the output 1.25 V, the high

voltage of the final stage is connected to the final output, and the LSB is set high, resulting in $\text{code} = 1001_2$. Note that SAR converter can generate an output voltage level that is successively approximated, so each stage of 2:1 converter is designed to generate a fixed level of voltage. When $V_{\rm IN}$, target voltage, or load current changes, only a successive (i.e., minimal) change of configuration is required for regulation.

In summary, output voltage is given as follows:

$$V_{\rm out} = (\text{Code}_2 + 1) \times V_R \tag{1}$$

where V_R, SAR SC converter resolution, is given as follows:

$$V_R = \frac{V_{\rm in}}{2^{\text{number of stages}}}. \tag{2}$$

For a 4 b design with 2 V input, resolution becomes 125 mV. Hence, the key benefit of the proposed converter is the possibility of very fine output voltage resolution over a wide output voltage range.

B. Current Flow and Sizing of SAR SC Converter

Depending on conversion ratio and the corresponding code, the SAR SC converter is reconfigured and the current flow through the SC converter is changed. We explain the current flow with an example using a 4 b SAR SC converter, as illustrated in Fig. 2. With code 1000_2, a conversion ratio of 9/16 is achieved, and each 2:1 SC converter should output current of $7/8 \times I_o$, $1/4 \times I_o$, $1/2 \times I_o$, and $1 \times I_o$ on average, where I_o is the output load current. On the other hand, with code 1010_2, a conversion ratio of 11/16 is achieved, and each 2:1 SC converter outputs currents of $5/8 \times I_o$, $3/4 \times I_o$, $1/2 \times I_o$, and $1 \times I_o$ on average. In addition, the current output of the LSB 2:1 SC converter stage is either zero or $\rm I_o$ according to the LSB code. As such, current flow in the SAR SC converter can be generalized as follows:

$$I_{H(0)} = \frac{1}{2}\overline{C_0} I_o \tag{3}$$

$$I_{L(0)} = \frac{1}{2}\overline{C_0} I_o \tag{4}$$

$$I_{o(1)} = \overline{C_1} C_0 I_o + \left(\overline{C_1} I_{H(0)} + C_1 I_{L(0)}\right) \tag{5}$$

$$I_{H(1)} = I_{L(1)} = \frac{1}{2} I_{o(1)}. \tag{6}$$

Similarly,

$$\begin{aligned} I_{o(k)} = {} & \overline{C_k} \cdot \sum_{i=0}^{k-2} \left(\prod_{j=i+1}^{k-1} C_j\right) I_{H(i)} \\ & + C_k \cdot \sum_{i=0}^{k-2} \left(\prod_{j=i+1}^{k-1} \overline{C_J}\right) I_{L(i)} \\ & + \left(\overline{C_k} I_{H(k-1)} + C_k I_{L(k-1)}\right) \end{aligned} \tag{7}$$

$$I_{H(k)} = I_{L(k)} = \frac{1}{2} I_{o(k)} \tag{8}$$

where code is given as $\overline{C_{n-1} C_{n-2} \cdots C_1 C_{0(2)}}$ and $I_{o(k)}$, $I_{H(k)}$, and $I_{L(k)}$ are the average output current, the current flow from $V_{\rm high}$, and the average current flow from $V_{\rm low}$ of the $(k+1)$th stage, respectively. Due to varying levels of current flow in each stage of 2:1 SC converter depending on configuration, 2:1 SC converters in all stages are sized identically in our implementation.

C. Loss Analysis and Comparison Against SC Converters

1) Analysis of Slow-Switching Limit Impedance for Nonconstant Output Voltage: Slow-switching limit impedance ($R_{\rm SSL}$) is the low-frequency output impedance (R_o) of SC converter under the assumption that switches and all other interconnects are ideal [13]. $R_{\rm SSL}$ arises from charge-sharing mechanism of SC converters. R_o determines the maximum available output of a power converter, and smaller R_o and $R_{\rm SSL}$ indicate higher driving capability of output power. In prior work [13], [16], $R_{\rm SSL}$ is derived for various topologies of SC converters under the assumption that output voltage is constant. However, in practice, only finite decoupling output capacitance is available, and hence the output voltage cannot be a constant level and instead varies periodically with input clocking, and current flow during nontransition phases in addition to instantaneous charge flow during clock transition states must be considered for $R_{\rm SSL}$ as opposed to the analysis in [13] and [16]. Thus, a different approach is required to derive $R_{\rm SSL}$ with nonconstant output voltage. This section covers such an $R_{\rm SSL}$ derivation and compares $R_{\rm SSL}$ with nonconstant output voltage level across various SC converter topologies.

$R_{\rm SSL}$ is inversely proportional to switching frequency and capacitance, so $R_{\rm SSL}$ can be generalized as $\frac{K_{SSL}}{F_s C_{\rm tot}}$, where F_S is switching frequency, $C_{\rm tot}$ is total flying capacitance, and $K_{\rm SSL}$ is the $R_{\rm SSL}$ coefficient, determined by the topology of the given SC converter and stated as a function of flying capacitance ($C_{\rm fly}$) and decoupling output capacitance ($C_{\rm dc}$). $K_{\rm SSL}$ determines performance of the SC converter. For instance, SC topologies with small $K_{\rm SSL}$ values have small output voltage drop due to $R_{\rm SSL}$, and they can supply larger output currents for a given switching frequency and flying capacitance than ones with large $K_{\rm SSL}$. In general, output voltage of an SC converter can be written as

$$V_{\rm OUT,AV} = V_{\rm NL} - R_{\rm SSL} I_o = V_{\rm NL} - \left(\frac{K_{\rm SSL}}{F_s C_{\rm tot}}\right) I_o \tag{9}$$

where $V_{\rm NL}$ is no-load output voltage, and I_o is output current.

Given the SC converter topology, the expression for $K_{\rm SSL}$ can be derived mathematically. A 2:1 SC converter with two-phase interleaving can be taken as an example, as illustrated in Fig. 3. The $V_{\rm OUT}$ waveform along with two clocks ($\rm CLK_A$ and $\rm CLK_B$) driving the converter switches is shown. The flying capacitor ($C_{\rm fly}$) connection is periodically switched; it is connected between $V_{\rm IN}$ and $V_{\rm OUT}$ for one phase, and then connected between $V_{\rm OUT}$ and VSS for the next phase. To avoid short-circuit current that results in charge loss, an intermediate state between the two phases exists, where both $\rm CLK_A$ and $\rm CLK_B$ are zero and $C_{\rm fly}$ is floating. In practice, the SC converter stays in the intermediate state for a short period of time, but it is important to consider it for understanding charge

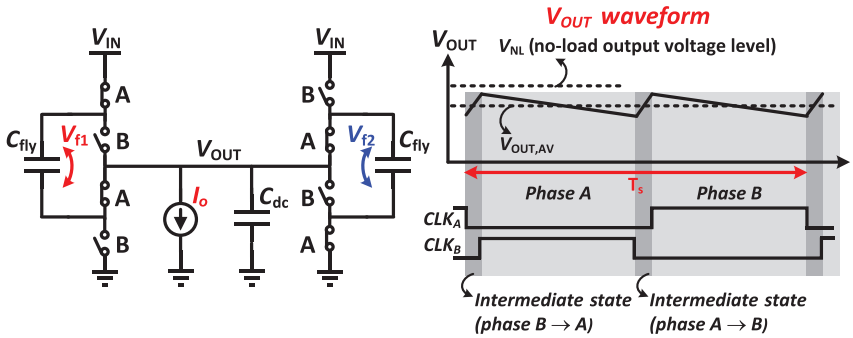

Fig. 3. 2:1 SC converter with two-phase interleaving (left), and $V_{\rm OUT}$ and clock waveforms (right).

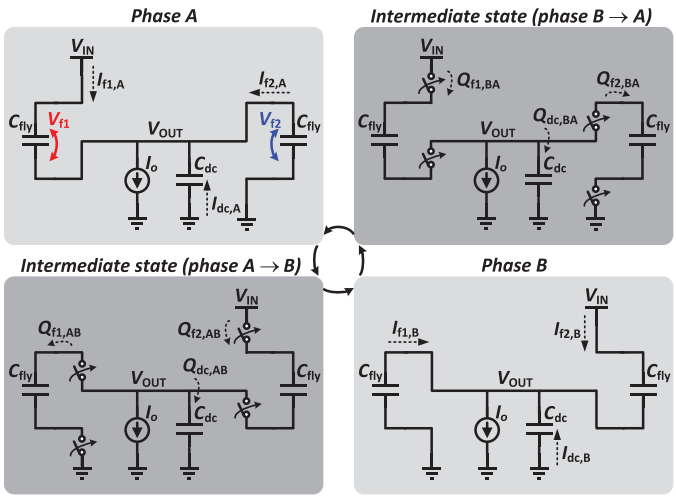

Fig. 4. Current and instantaneous charge flow of a 2:1 SC converter with two-phase interleaving at each phase and intermediate state.

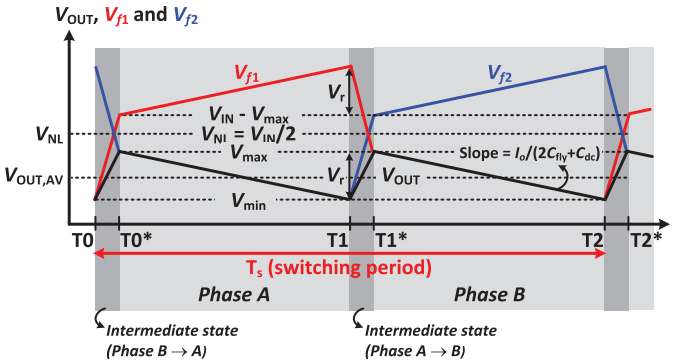

Fig. 5. Waveforms of output voltage ($V_{\rm OUT}$) and voltages across flying capacitors (V_{f1} and V_{f2}) of 2:1 SC converter with two-phase interleaving.

flow during SC converter operation. Fig. 4 illustrates the current (denoted as I) and instantaneous charge flow (denoted as Q) of the 2:1 SC converter with two-phase interleaving, and Fig. 5 provides detailed waveforms of $V_{\rm OUT}$ and voltages across $C_{\rm fly}$'s (V_{f1} and V_{f2}).

In deriving the $K_{\rm SSL}$ expression, the following naming conventions are used. The first subscript indicates what element the current or charge relates to, namely "$f1$" indicates left $C_{\rm fly}$, "$f2$" indicates right $C_{\rm fly}$, and "dc" indicates $C_{\rm dc}$. The second subscript denotes the relevant phase or intermediate state. "A" is phase A, "B" is phase B, "AB" is the intermediate state when transitioning from phase A to B, and "BA" represents the intermediate state when moving from phase B to A.

As the number of interleaved phases is two, the following equations are valid:

$$I_{f1,\rm A} = I_{f2,\rm B} \tag{10}$$
$$I_{f1,\rm B} = I_{f2,\rm A} \tag{11}$$
$$I_{\rm dc,A} = I_{\rm dc,B} \tag{12}$$
$$Q_{f1,\rm AB} = Q_{f2,\rm BA} \tag{13}$$
$$Q_{f1,\rm BA} = Q_{f2,\rm AB} \tag{14}$$
$$Q_{\rm dc,AB} = Q_{\rm dc,BA}. \tag{15}$$

In addition, the following current equations can be derived:

$$I_{f1,A} = \frac{C_{\rm fly}}{2C_{\rm fly}+C_{\rm dc}} I_o \tag{16}$$
$$I_{f2,A} = \frac{C_{\rm fly}}{2C_{\rm fly}+C_{\rm dc}} I_o \tag{17}$$
$$I_{dc,A} = \frac{C_{\rm dc}}{2C_{\rm fly}+C_{\rm dc}} I_o \tag{18}$$
$$\text{Output voltage ripple}: V_r = \frac{T_s I_o}{2\,(2C_{\rm fly}+C_{\rm dc})}. \tag{19}$$

Let us assume that the duration of the intermediate state is negligibly small ($T0 \cong T0*$, $T1 \cong T1*$, $T2 \cong T2*$), and derive expressions for $Q_{f2,\rm AB}$, $Q_{\rm dc,AB}$, and $Q_{f1,\rm AB}$. Since average input current $(I_{\rm in})_{\rm AV} = I_o/2$, charge influx from $V_{\rm IN}$ during half period of T_s is $\frac{I_o}{2}\frac{T_s}{2} = Q_{f2,\rm AB} + I_{f1,\rm A}\frac{T_s}{2}$, and thus $Q_{f2,\rm AB}$ can be written as follows:

$$Q_{f2,\rm AB} = \left(\frac{I_o}{2} - I_{f1,\rm A}\right)\frac{T_s}{2} = \frac{C_{\rm dc}}{2C_{\rm fly}+C_{\rm dc}}\frac{T_s I_o}{4} = \frac{V_r C_{\rm dc}}{2}. \tag{20}$$

In steady state, the charge lost from $C_{\rm dc}$ during phase A or B is replenished during intermediate states, hence $Q_{\rm dc,AB}$ and $Q_{f1,\rm AB}$ are written as follows:

$$Q_{\rm dc,AB} = V_r C_{\rm dc}. \tag{21}$$

Thus,

$$Q_{f1,\mathrm{AB}} = Q_{f2,\mathrm{AB}} - Q_{\mathrm{dc,AB}} = -\frac{V_r C_{\mathrm{dc}}}{2}. \tag{22}$$

Now, let us define the minimum and maximum output voltage as $V_{\min}$ and $V_{\max}$. Then,

$$V_{\mathrm{OUT}}(T0) = V_{\mathrm{OUT}}(T1) = V_{\min} \tag{23}$$

$$V_{\mathrm{OUT}}(T0^*) = V_{\mathrm{OUT}}(T1^*) = V_{\max} \tag{24}$$

$$V_{f1}(T0^*) = V_{\mathrm{IN}} - V_{\max} \tag{25}$$

$$V_{\min} = V_{\max} - V_r. \tag{26}$$

To derive $V_{\max}$ as a function of V_{IN}, C_{fly}, C_{dc}, T_s, and I_o,

$$V_{f1}(T1) = V_{f1}(T0^*) + V_r = V_{\mathrm{IN}} - V_{\max} + V_r \tag{27}$$

$$V_{f1}(T1^*) = V_{f1}(T1) + \frac{Q_{f1,\mathrm{AB}}}{C_{\mathrm{fly}}} = V_{\mathrm{IN}} - V_{\max} + V_r - \frac{V_r C_{\mathrm{dc}}}{2C_{fly}}. \tag{28}$$

Since $V_{f1}(T1^*) = V_{\max}$,

$$V_{\max} = \frac{1}{2} \times \left\{ V_{\mathrm{IN}} - \frac{V_r(-2C_{\mathrm{fly}} + C_{\mathrm{dc}})}{2C_{\mathrm{fly}}} \right\} = \frac{V_{\mathrm{IN}}}{2} - \frac{T_s I_o (-2C_{\mathrm{fly}} + C_{\mathrm{dc}})}{8C_{\mathrm{fly}}(2C_{\mathrm{fly}} + C_{\mathrm{dc}})} \tag{29}$$

$$V_{\mathrm{OUT,AV}} = V_{\max} - \frac{V_r}{2} = \frac{V_{\mathrm{IN}}}{2} - \frac{T_s I_o(-2C_{\mathrm{fly}} + C_{\mathrm{dc}})}{8C_{\mathrm{fly}}(2C_{\mathrm{fly}} + C_{\mathrm{dc}})} - \frac{T_s I_o}{4\,(2C_{\mathrm{fly}} + C_{\mathrm{dc}})} = \frac{V_{\mathrm{IN}}}{2} - \frac{T_s I_o C_{\mathrm{dc}}}{8C_{\mathrm{fly}}(2C_{\mathrm{fly}} + C_{\mathrm{dc}})}. \tag{30}$$

As $2C_{\mathrm{fly}} = C_{\mathrm{tot}}$ (total flying capacitance) and $T_s = 1/F_s$, a 2:1 SC converter with two-phase interleaving has K_{SSL} given by (31). is dependent on flying capacitance and decoupling output capacitance

$$K_{\mathrm{SSL}} = \frac{C_{\mathrm{dc}}}{4\,(2C_{\mathrm{fly}} + C_{\mathrm{dc}})}. \tag{31}$$

Generalized K_{SSL} expressions for an SAR SC converter, a recursive SC (RSC) converter [16], series-parallel SC converter, and ladder SC converter with two-phase interleaving and no output capacitance can be derived similarly; the derived expressions are summarized in Table I. K_{SSL} of SAR SC and RSC converters is not closed-form expression and is instead found using recursive MATLAB code. The K_{SSL} expressions were verified by comparisons against HSPICE simulation results. Difference between HSPICE simulation results with ideal switches and expected results of MATLAB modeling is less than 1%, regardless of load current, total flying capacitance, and conversion ratio.

Fig. 6 plots K_{SSL} for SAR SC converters, RSC converters, series-parallel SC converters, and ladder SC converters with various conversion ratios for the given number of stages bits, when $C_{\mathrm{dc}} = 0$. The number of bits indicated with series-parallel SC and ladder SC converters in Fig. 6 represents the denominator of the conversion ratio. For instance, 4 bit series–parallel SC and ladder SC converters generate $k/2^4 (k = \text{odd integers greater than 0 and smaller than } 2^4)$. It is shown that series-parallel SC and ladder SC converters have K_{SSL} increased by $O(N)$ and $O(N^4)$, respectively, where $N = 2^{\text{number of bits}}$. Although series-parallel SC converters perform better than ladder SC converters with the same number of bits in terms of K_{SSL}, the irregular structure of series-parallel SC converters results in challenges when reconfiguring between multiple conversion ratios. In contrast, SAR SC converters have K_{SSL} that increases with $\log_2 N$, or the number of stages, and offer many conversion ratios with easy reconfiguration and less R_{SSL} overhead.

As $\mathrm{R_o}$ is an indicator of output power deliverable in power converter, power density of an SC converter can be predicted with K_{SSL}. Equation (32) implies that power density is proportional to $C_{\mathrm{tot}}/(\mathrm{Area} \times K_{\mathrm{SSL}})$, where $C_{\mathrm{tot}}/\mathrm{Area}$ is defined as capacitance density determined by CMOS process technology, so $1/K_{\mathrm{SSL}}$ can be used as a metric for comparison of power density in given CMOS process technology. In an SAR SC converter, power density degrades in proportion to $1/\log_2 N$, or 1/(number of stages)

$$\text{Power density} = \frac{P_L}{\mathrm{Area}} = \frac{V_{\mathrm{OUT}} I_L}{\mathrm{Area}} \propto \frac{1}{R_o \times \mathrm{Area}} \propto \frac{F_s C_{\mathrm{tot}}}{K_{\mathrm{SSL}}} \times \frac{1}{\mathrm{Area}}. \tag{32}$$

2) Analysis of Switching Loss Due to Bottom-Plate Parasitic Capacitors: Fully integrated SC converters employ MIM or MOS capacitors for flying capacitors, and bottom-plate parasitic capacitors of these flying capacitors cannot be ignored in moderate load power condition where gate-driving loss and switch conductance loss are relatively small [18]. This is because switching frequency scales with load power, resulting in small gate-driving loss in low load power, as discussed in [18]. Switching loss due to bottom-plate parasitic capacitors (P_{BOT}) can be generalized as follows:

$$P_{\mathrm{BOT}} = \sum_{\mathrm{i}} C_{\mathrm{bot(i)}} \{ s_{\mathrm{ph1(i)}} V_{\mathrm{bot(i),ph1}} \left(V_{\mathrm{bot(i),ph1}} - V_{\mathrm{bot(i),ph2}} \right) + s_{\mathrm{ph2(i)}} V_{\mathrm{bot(i),ph2}} \left(V_{\mathrm{bot(i),ph2}} - V_{\mathrm{bot(i),ph1}} \right) \} \times F_s \tag{33}$$

where $C_{\mathrm{bot(i)}}$ is a bottom-plate parasitic capacitance at node (i), $V_{\mathrm{bot(i),ph1}}$ and $V_{\mathrm{bot(i),ph2}}$ are potentials, $s_{\mathrm{ph1(i)}}$ and $s_{\mathrm{ph2(i)}}$ are scaling factors of $C_{\mathrm{bot(i)}}$ at node (i) in phase 1 and 2, and F_s is switching frequency.

In (33), scaling factors $s_{\mathrm{ph1(i)}}$ and $s_{\mathrm{ph2(i)}}$ are necessary because switching loss due to bottom-plate parasitic arises at internal node (i), where only a fraction of the loss comes from input voltage and the rest comes from ground. Equation (33) can be simplified to (34) by using bottom-plate loss coefficient K_{BOT}. K_{BOT} can be regarded as the normalized bottom-plate loss with ratio of bottom-plate parasitic to a flying capacitor, total flying capacitance, squared input voltage, and switching frequency. Thus, K_{BOT} is determined by the topology of the given SC converter, and K_{BOT} limits power conversion efficiency of the SC converter

$$P_{\mathrm{BOT}} = K_{\mathrm{BOT}}(a_{\mathrm{bot}} C_{\mathrm{tot}}) V_{\mathrm{IN}}^2 F_s \tag{34}$$

TABLE I
GENERALIZED K_{SSL} EXPRESSIONS FOR VARIOUS TOPOLOGIES WHEN OUTPUT CAPACITANCE (C_{dc}) IS ZERO. K/N IS CONVERSION RATIO, $V_{\mathrm{OUT}}/V_{\mathrm{IN}}$

Topology	K_{SSL} ($C_{\mathrm{dc}} = 0$)
SAR	$\propto \log_2 N$
Series–parallel	$\frac{k^2(N-k)^2(N-2k)^2}{2N^2(k^2+(N-k)^2)}$
Conv. ladder	$\frac{(N-1)\times(4N^3k^2-8N^2k^3+8N^2k^2-N^2k-3N^2+4Nk^4-16Nk^3+Nk^2+4Nk-3N+8k^4-4k^2)}{12N(N+2)}$

It is assumed that flying capacitances in an SC converter are sized equal, and two-phase is interleaved

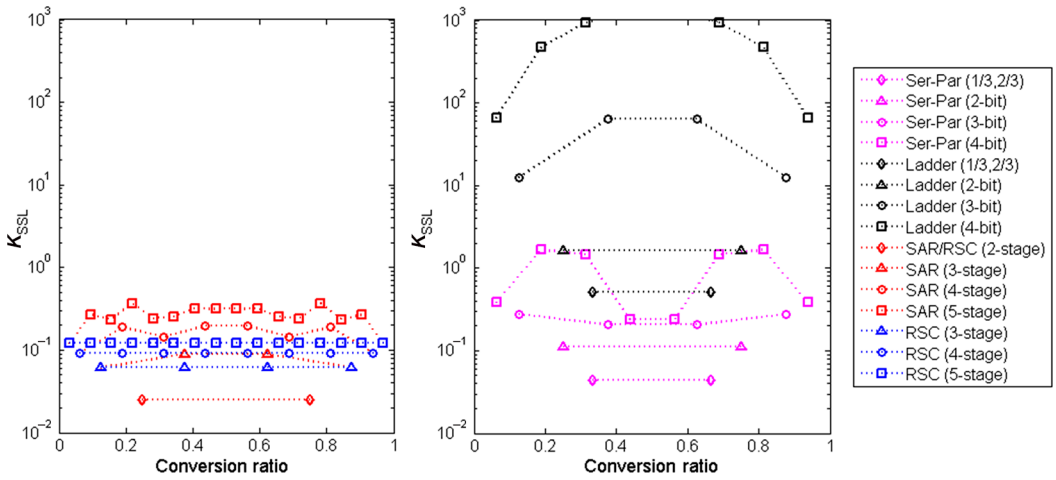

Fig. 6. R_{SSL} coefficient (K_{SSL}) versus conversion ratio for SAR SC and RSC converters (left); for series–parallel SC and ladder SC converters (right).

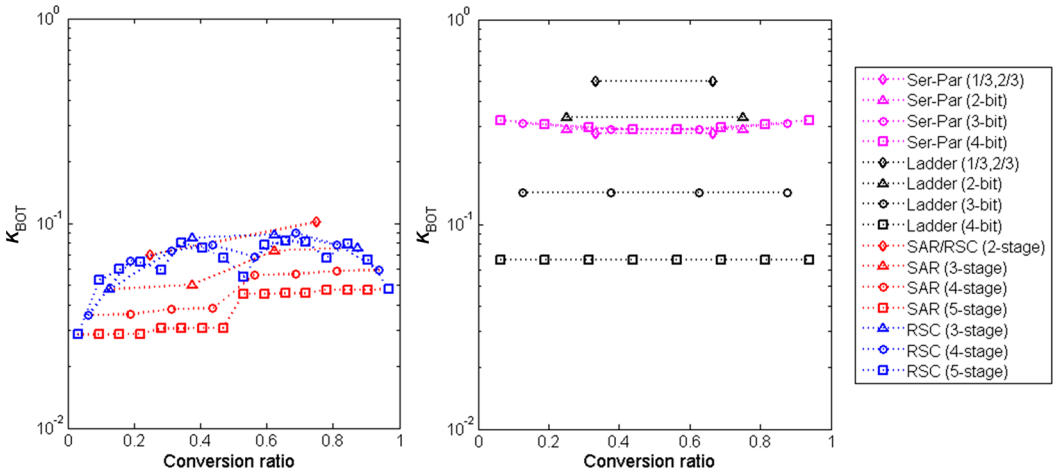

Fig. 7. P_{BOT} loss coefficient (K_{BOT}) versus conversion ratio for SAR SC and recursive RSC converters (left); for series-parallel SC and ladder SC converters (right).

where a_{bot} is the ratio of bottom-plate parasitic to flying capacitors ($C_{\mathrm{bot}}/C_{\mathrm{fly}}$), C_{tot} is total flying capacitance, V_{IN} is input voltage, and F_s is switching frequency.

Based on (34) and the R_{SSL} analysis, P_{BOT} can be obtained mathematically as plotted in Fig. 7. Fig. 7 shows K_{BOT} for SAR SC converters, RSC converters, series-parallel SC converters, and ladder SC converters with various conversion ratios for the given number of stages bits. It is noted that SAR SC and ladder SC converters have K_{BOT} scaling with the number of stages, or the number of bits, but RSC and series-parallel SC converters have K_{BOT} that is almost constant regardless of the number of stages, or the number of bits. This is because SAR SC converters decrease voltage swings, which is defined as $|V_{\mathrm{bot(i),ph1}} - V_{\mathrm{bot(i),ph2}}|$ of bottom-plate parasitic capacitors

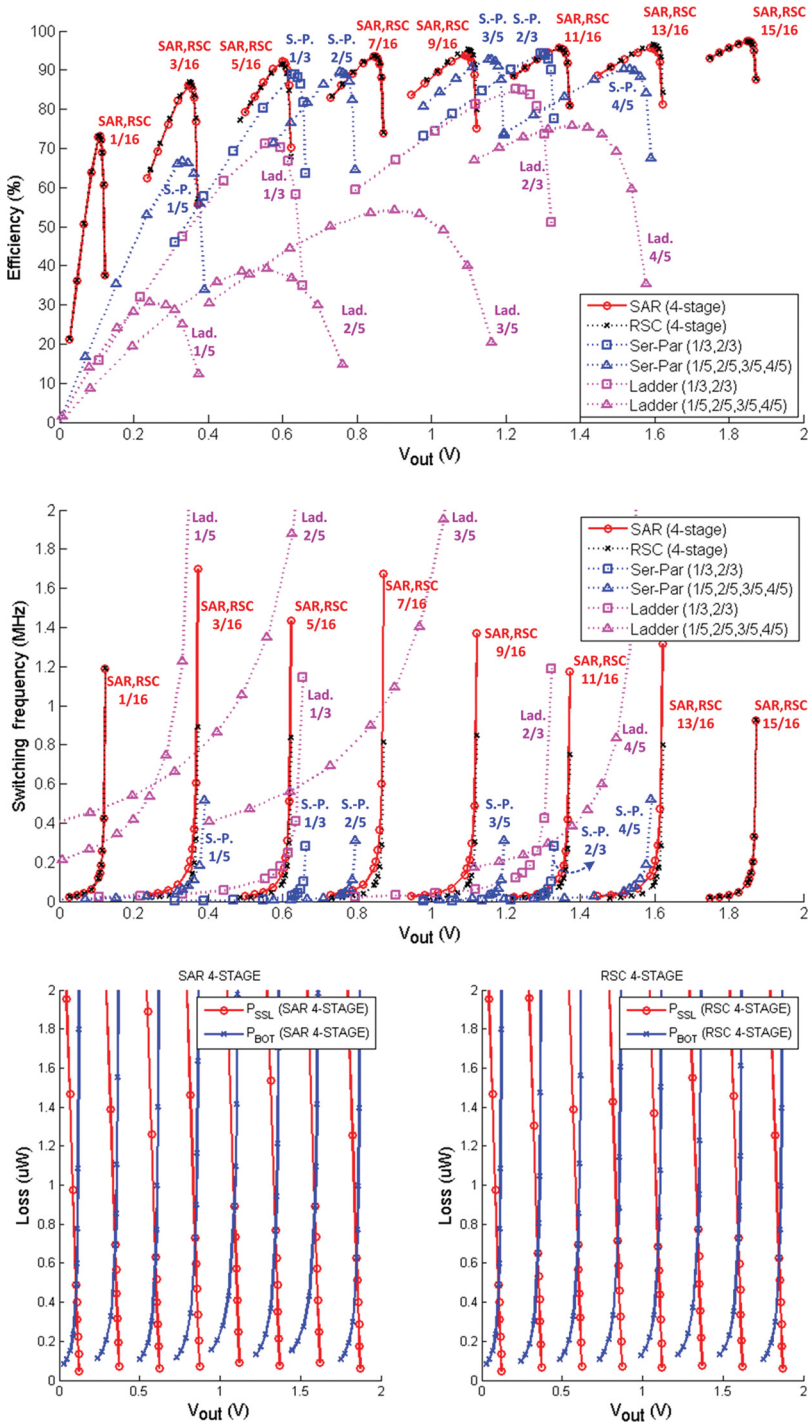

Fig. 8. Efficiency versus output voltage with frequency modulation (top), corresponding frequency versus output voltage (middle), and corresponding changes of $P_{\rm SSL}$ loss and $P_{\rm BOT}$ loss in four-stage SAR SC and RSC SC converters (bottom) when $V_{\rm IN} = 1\,{\rm V}$, total capacitance $= 1\,{\rm nF}$, $C_{\rm bot}/C_{\rm fly} = 3\%$, and $I_o = 25\,\mu{\rm A}$.

at the later stages, as the number of stages increases. Similarly, ladder SC converters reduce voltage swings of bottom-plate capacitors with increasing number of bits, and decrease $K_{\rm BOT}$.

3) Loss Optimization and Comparison of SC Converters: In moderate and low load power regime, total loss ($P_{\rm loss}$) can be expressed as a sum of loss due to $R_{\rm SSL}$ ($P_{\rm SSL}$), and loss due to bottom-plate switching ($P_{\rm BOT}$): $P_{\rm loss} = P_{\rm SSL} + P_{\rm BOT}$. $P_{\rm SSL}$ can be written with $K_{\rm SSL}$ as the following equation:

$$P_{\rm SSL} = R_{\rm SSL} I_L^2 = \frac{K_{\rm SSL}}{F_s C_{\rm tot}} I_L^2 \tag{35}$$

where F_s is switching frequency, $C_{\rm tot}$ is total flying capacitance, and I_L is load current.

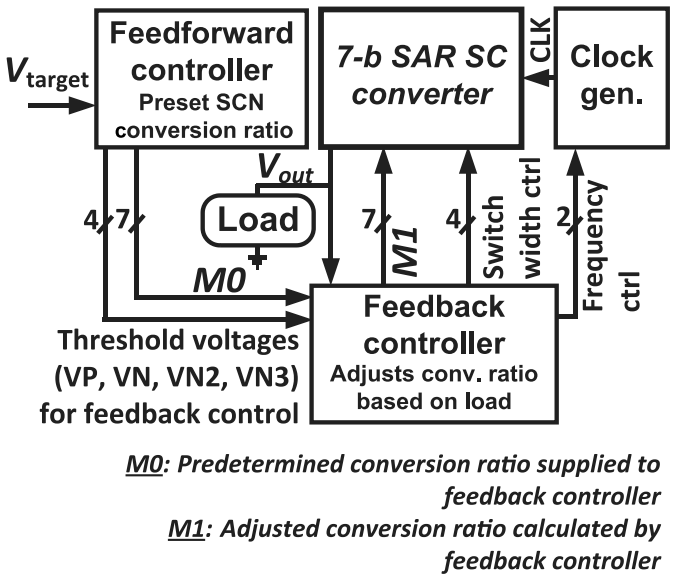

Fig. 9. Top-level block diagram of proposed 7 b SAR SC converter.

Based on (34) and (35), optimal switching frequency ($F_{s,\mathrm{opt}}$), optimal loss ($P_{\mathrm{loss,opt}}$), and corresponding optimal efficiency (η_{opt}) can be obtained as the following equations:

$$F_{s,\mathrm{opt}} = \sqrt{\frac{K_{\mathrm{SSL}}}{a_{\mathrm{bot}} K_{\mathrm{BOT}}}} \frac{I_L}{V_{\mathrm{IN}} C_{\mathrm{tot}}} \tag{36}$$

$$P_{\mathrm{loss,opt}} = 2\sqrt{P_{\mathrm{SSL}} P_{\mathrm{BOT}}} = 2\sqrt{a_{\mathrm{bot}} K_{\mathrm{SSL}} K_{\mathrm{BOT}}} V_{\mathrm{IN}} I_L \tag{37}$$

$$\eta_{\mathrm{opt}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss,opt}}} = \frac{1}{1 + 2\sqrt{a_{\mathrm{bot}} K_{\mathrm{SSL}} K_{\mathrm{BOT}}} \times \left(\frac{V_{\mathrm{IN}}}{V_o}\right)}. \tag{38}$$

Equations (36)–(38) imply that frequency scaling with load current can track optimal efficiency, under the moderate and low load power regime, and regulation capabilities with frequency modulation for load regulation. Fig. 8 shows simulation results based on mathematical models mentioned in Sections II-C1 and II-C2. Under simulation conditions of $V_{\mathrm{IN}} = 2\,\mathrm{V}$, $C_{\mathrm{tot}} = 1\,\mathrm{nF}$, $a_{\mathrm{bot}} = 3\%$, and fixed $I_L = 25\,\mu\mathrm{A}$, efficiency is plotted against output voltage as a result of switching frequency change for different topologies: four-stage SAR SC, four-stage RSC, series-parallel SC, and ladder SC converters with conversion ratios of 1/3, 2/3, 1/5, 2/5, 3/5, and 4/5, at the top of Fig. 8. The corresponding frequencies are shown across output voltage in the middle of Fig. 8. Also, the corresponding changes in P_{SSL} and P_{BOT} as a result of frequency control in SAR SC, and RSC converters are plotted against output voltage in the bottom of Fig. 8. It is noted that optimized SAR SC converters offer a large number of conversion ratios with comparable efficiency to series-parallel SC converters, and SAR SC converters achieve good efficiency over wide range of output voltages, as opposed to conventional series-parallel SC and ladder SC converters with comparable efficiency for a limited range of output voltage. It is also noted that smaller $\mathrm{P_{BOT}}$ of SAR SC converters compensates for P_{SSL} which is slightly larger than RSC converters, resulting in similar optimal efficiencies.

III. Design of Prototype SAR SC Converter

A. Architecture of 7 b SAR SC Converter

A 7 b SAR SC converter is fabricated in a test chip, with additional features such as closed-loop output regulation under load variation and line variation, as shown in Fig. 9. The implemented 7 b SAR SC converter is designed as a cascaded structure of one 4:1 converter and five 2:1 converters (Fig. 10). Each converter is two-phase interleaved. To enable efficient low swing clocks, the first stage is constructed using a 4:1 converter, and the clock generation uses V_{BAT} and $\mathrm{VDD3Q} = 3/4 \times V_{\mathrm{BAT}}$ as its supply and ground. By using V_{BAT} and VDD3Q, clock swing and frequency automatically increase under heavy loading conditions as VDD3Q droops. This creates inherent negative feedback to automatically mitigate P_{SSL}. A conventional approach using VDD1Q and VSS would instead experience voltage droop on VDD1Q, yielding a clock frequency/swing reduction with positive feedback, limiting converter-operating load range.

Capacitive level shifters are used in each converter to drive the switches. For example, the gate voltage G_1 of switch S_1 is referenced to its source (VH [3]) by the cross-coupled PFET structure R_1 and R_2. The gate voltage G_1 then swings low from this reference point through capacitive coupling driven by inverter I_1. Conversely, the gate voltage G_2 of S_2 is referenced to its source VM [3] and is coupled high by I_2. Since the cross-coupled PFET level shifter inherently generates two opposite polarities, a two-phase interleaving can be constructed with effectively no overhead. Four switch structures are connected in parallel, sized $1\times$, $1\times$, $2\times$, and $4\times$ to implement binary-weighting using the thermometer control code SEN[3:0] for switch width modulation. The configuration switches toggle only when the configuration vector changes, and hence can be made large to limit resistive loss with minimal switching energy cost.

B. Feedforward and Feedback Control

Feedforward and feedback controllers provide fine grain control and react to load and line variations. As shown in Fig. 11, the feedforward controller predetermines a conversion ratio M0 by comparing V_{target} with a ramp voltage (V_{RAMP}) that increases by $V_{\mathrm{BAT}}/2^7$ for each cycle of CLKd, which is $32\times$ slower than the converter switching clock (CLK). V_{RAMP} is generated from 2^7 diode-connected PFETs in series, and V_{RAMP} is not generated from the SC converter. M0 is obtained by counting the clock cycle at which V_{RAMP} exceeds V_{target}, and it is updated every 2^7 cycles of CLKd, so M0 is kept the same unless input voltage V_{BAT} changes. Note that V_{target} can be generated with ultra-low power reference voltages [14], [15].

The M0 configuration code results in an SC output voltage (V_{OUT}) that matches V_{target} within one resolution of SAR SC converter, $V_s = V_{\mathrm{BAT}}/2^7$ under no-load conditions (where

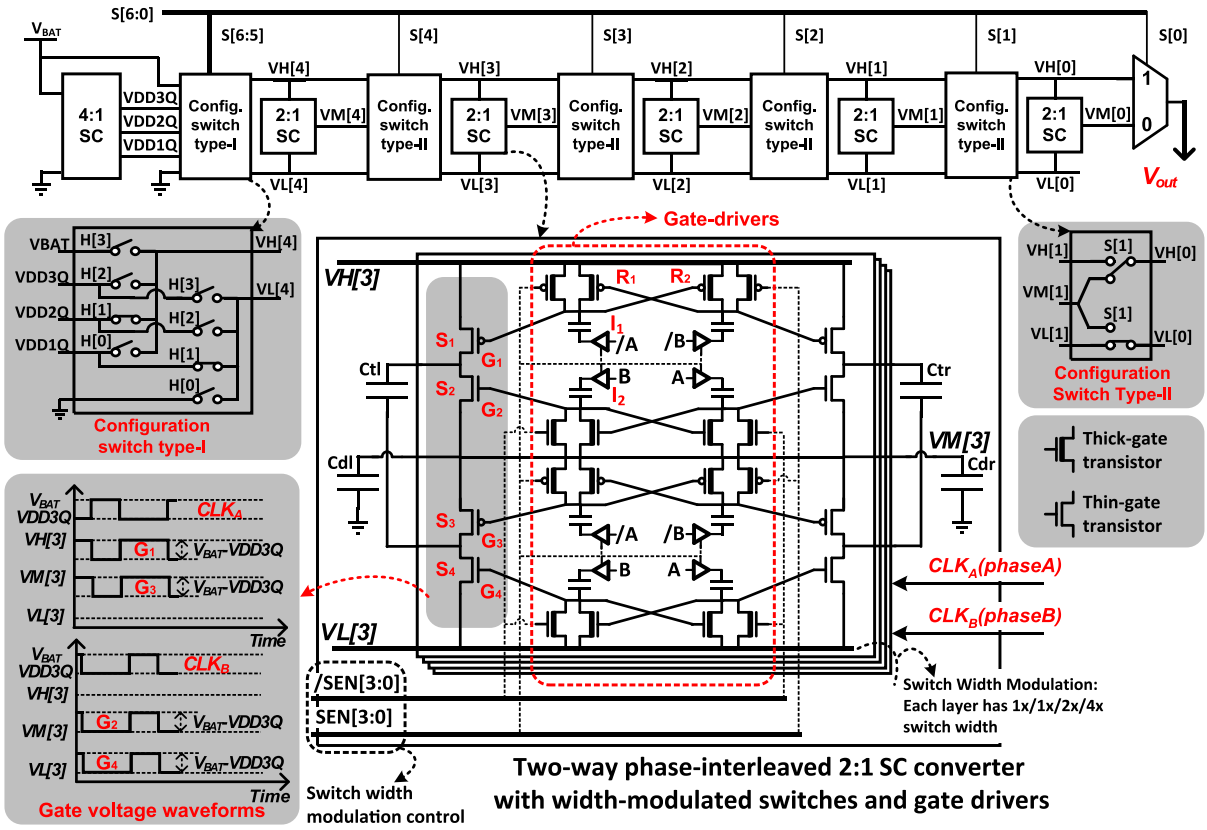

Fig. 10. Proposed 7 b SAR SC DC–DC converter (top). Detailed schematics of configuration switch type-I, II, and 2:1 SC converter (middle). Gate voltage waveforms of a 2:1 SC converter (bottom).

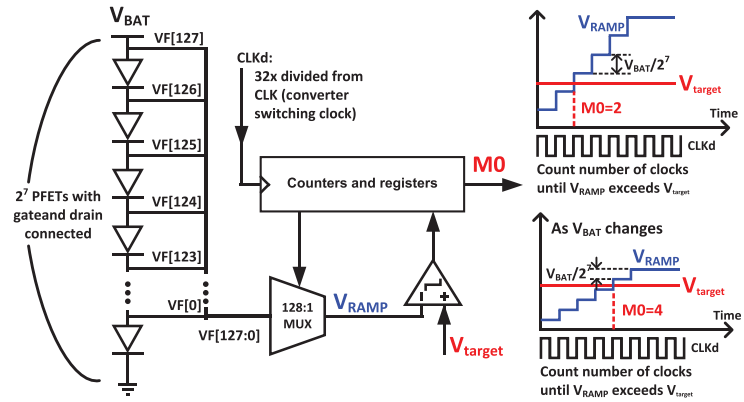

Fig. 11. Feedforward controller details and operation.

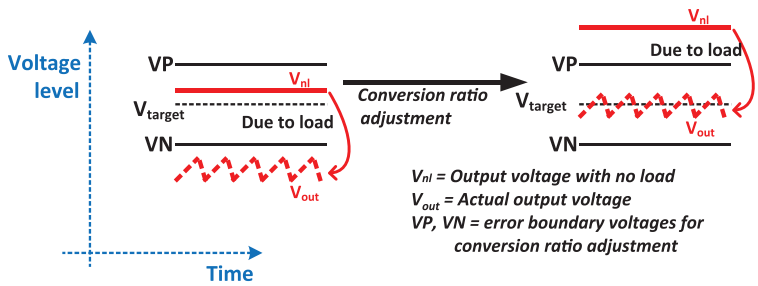

Fig. 12. Conversion ratio adjustment of feedback controller.

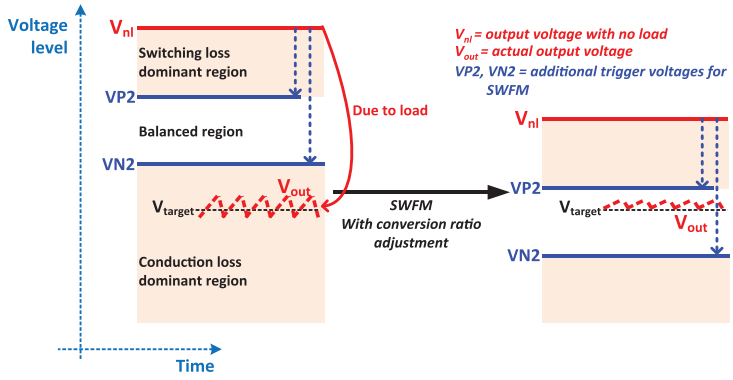

Fig. 13. Switch width and frequency modulation.

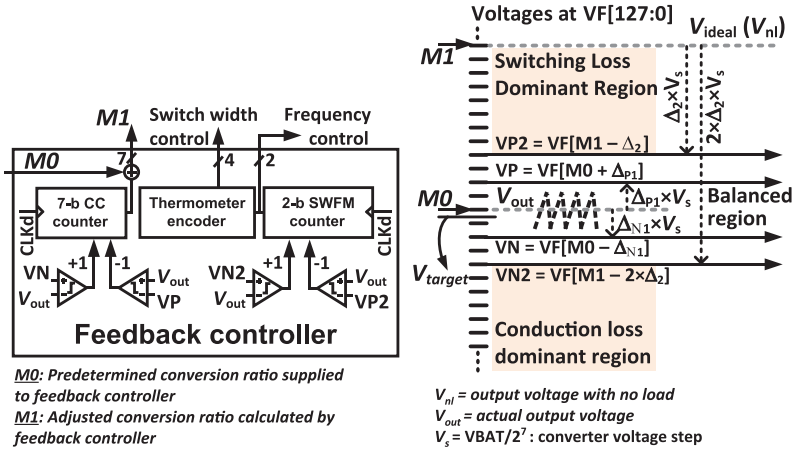

Fig. 14. Feedback controller details and operation (left). Trigger voltage levels (right).

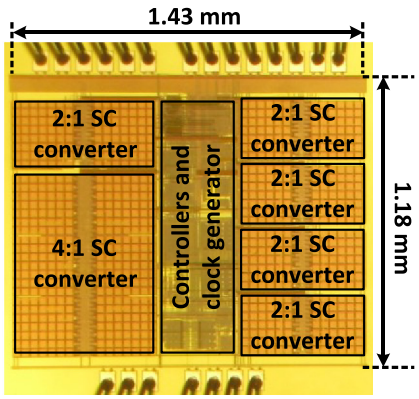

Fig. 15. Die photograph.

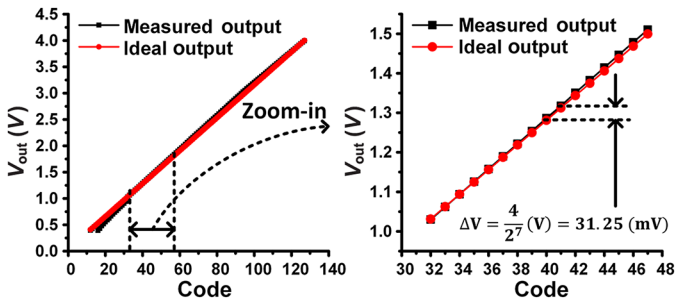

Fig. 16. Measured output voltage levels and ideal output voltage levels of 7 b SAR SC converter at $V_{\mathrm{BAT}} = 4$ V and no load.

$V_s = 31.25\,\mathrm{mV}$ with $V_{\mathrm{BAT}} = 4.0\,\mathrm{V}$). As shown in Fig. 12, V_{OUT} droops in the presence of load, so the FB controller adjusts the conversion ratio to maintain a constant output voltage. For this, two trigger voltages VP and VN are generated from the diode stack with separate 2^7:1 muxes, where $\mathrm{VP} = \mathrm{VF}[M0 + \Delta_{P1}]$ and $\mathrm{VN} = \mathrm{VF}[M0 - \Delta_{N1}]$. V_{OUT} is compared with VP and VN at each cycle and the conversion ratio is adjusted to maintain the condition $\mathrm{VN} < V_{\mathrm{OUT}} < \mathrm{VP}$. By incrementing/decrementing a 7 b counter and adding it to M0, the adjusted configuration code $M1$ ($\geq M0$) is obtained.

To prevent converter efficiency from being limited by conduction loss or series loss that consists of slow-switching limit impedance loss and fast-switching limit impedance loss [13], [18], the frequency and switch widths are dynamically modulated in a binary-weighted fashion by the feedback controller. Two additional trigger voltages VP2 and VN2 are generated, where $\mathrm{VP2} = \mathrm{VF}[M1 - \Delta_2]$ and $\mathrm{VN2} = \mathrm{VF}[M1 - 2\Delta_2]$ (using two additional 2^7:1 muxes). In this implementation, Δ_2 is set to 5 and hence $\Delta_2 \times V_s = 156.25\,\mathrm{mV}$. VP2 and VN2 are referenced to VF[$M1$], which is the ideal (no-load) voltage level of the SC converter at M1. As shown in Fig. 13, when V_{OUT} lies within $\Delta_2 \times V_s$ of this no-load output voltage ($V_{\mathrm{OUT}} > \mathrm{VP2}$), switching loss dominates and switch size and frequency are reduced by decrementing switch width and

frequency modulation (SWFM) counter shown in Fig. 14 (left). Similarly, when $V_{\rm OUT}$ falls below the no-load output voltage $V_{\rm ideal}$ by more than $2 \times \Delta_2 \times V_s$ ($V_{\rm OUT} < {\rm VN2}$), conduction loss is dominant and switch size and frequency are increased. By correctly setting Δ_2, the switching and conduction losses remain balanced over a large load range, hence improving conversion efficiency. The feedback controller is implemented with digital counters, a thermometer encoder, and comparators, as seen in Fig. 14 (left). Trigger voltage levels (VP, VP2, VN, and VN2) are visualized in Fig. 14 (right).

IV. Measurement Results

The SAR SC converter is fabricated in 180 nm CMOS process. Fig. 15 shows the chip photograph. The fabricated test chip with 2.24 nF on-chip capacitance occupies $1.69\,{\rm mm}^2$. MIM capacitor and MOS capacitor are used for on-chip flying capacitors and decoupling capacitors, respectively.

Fig. 16 shows measured outputs and ideal outputs of the 7 b SAR SC converter from this paper with a resolution of 31.25 mV at $V_{\rm BAT} = 4\,{\rm V}$.[1] Fig. 17 shows $V_{\rm OUT}$ regulation results, code change, clock frequency change, and efficiency across load currents at $V_{\rm BAT} = 4\,{\rm V}$ and $V_{\rm target} = 1.2\,{\rm V}$. $V_{\rm OUT}$ is continually compared against trigger voltage levels (VN, VP, VN2, and VP2). As the load current increases from 0 to 300 μA, the conversion code increases to compensate for conduction loss. When $V_{\rm OUT} - V_{\rm ideal} > 2 \times \Delta_2 \times V_s$, the feedback controller increments the 2 b SWFM counter, increasing switch width and clock frequency. Every step increase in the SWFM counter results in an approximately $1.7\times$ increase in clock frequency. Note that when load current decreases and $V_{\rm OUT} - V_{\rm ideal} < \Delta_2 \times V_s$, the feedback controller decrements the SWFM counter, decreasing switch width and clock frequency. Fig. 18 shows a simplified schematic of the clock generator and 4:1 SC converter, and a plot of measured clock frequency and $V_{\rm BAT} - {\rm VDD3Q}$.

Fig. 19 shows the effectiveness of dynamic SWFM; $>$ 50% efficiency is achieved across a load range of 2–300 μA using dynamic SWFM compared to 30–300 μA when using a single setting (SWFM = 3). Efficiency fluctuates slightly at neighboring load currents. This arises due to varying SSL impedance with switch configurations, as was also seen in Fig. 6. Fig. 20 shows load regulation measurement results at $V_{\rm BAT} = 4\,{\rm V}$ for $V_{\rm target} = 0.9$, 1.2, and 1.5 V. The converter achieves peak efficiency of 69%, 65%, and 72% with output voltage regulation within ±54, ±41, and ±81 mV for $V_{\rm target} = 0.9$, 1.2, and 1.5 V, respectively. It is shown that SWFM effectively balances switching loss and conduction loss, enabling a flat efficiency curve across a wide range of load currents.

Fig. 21 (left) shows that a wide range of arbitrary $V_{\rm OUT}$ can be generated due to the highly reconfigurable nature of SAR SC converters. Fig. 21 (right) shows line regulation at target voltages of 0.9, 1.2, and 1.5 V for $V_{\rm BAT}$ values ranging from 3.4 to 4.3 V. $V_{\rm OUT}$ variation depends on VP−VN, which is

[1]In 180 nm CMOS process, thick-gate transistors and thin-gate transistors are rated for maximum of 3.6 and 2.0 V, respectively.

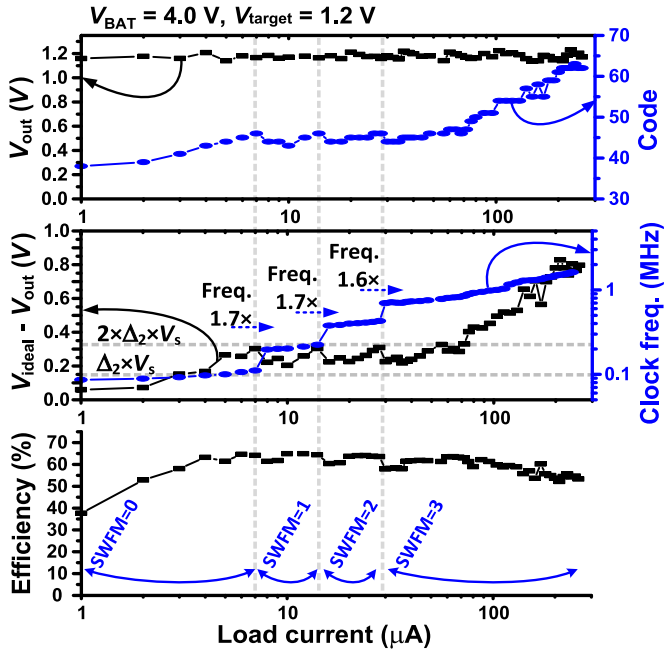

Fig. 17. Measurement results. $V_{\rm OUT}$ and code versus load current (top). $V_{\rm ideal} - V_{\rm OUT}$ and clock frequency versus load current (middle). Efficiency versus load current (bottom).

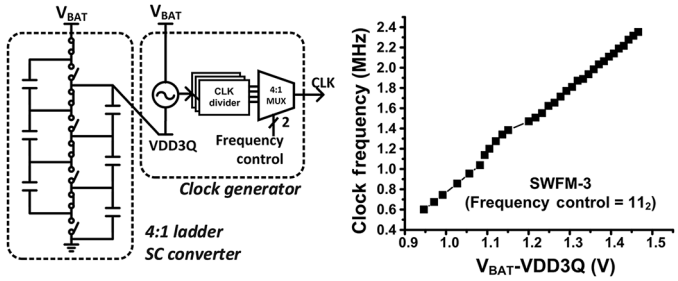

Fig. 18. Simplified schematic of clock generator and 4:1 SC converter (left). Measured clock frequency versus VBAT−VDD3Q (right).

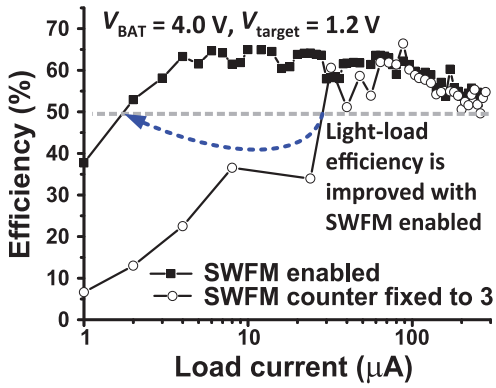

Fig. 19. Measured efficiency versus load current with SWFM enabled, and SWFM fixed to 3.

set at $3 \times V_s$ (93.75 mV), as well as comparator offset in the feedback controller.

Fig. 22 shows transient step response waveforms. Fig. 22 (left) is the transient load step response when load current changes from 10 to 0 μA and from 0 to 50 μA, with $V_{\rm BAT} =$

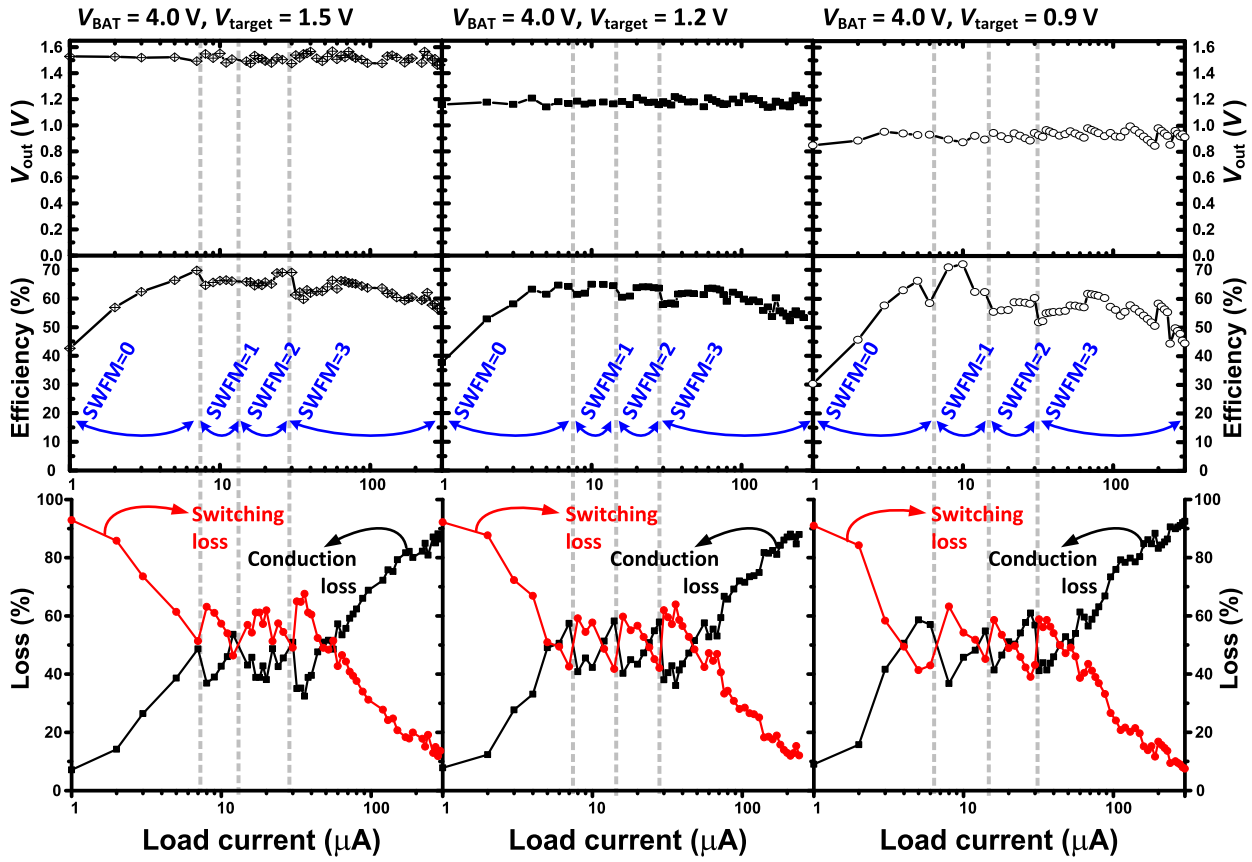

Fig. 20. Measured V_{OUT}, efficiency, and switching/conduction loss versus load current for $V_{\mathrm{target}} = 1.5$ V (left), 1.2 V (middle), and 0.9 V (right).

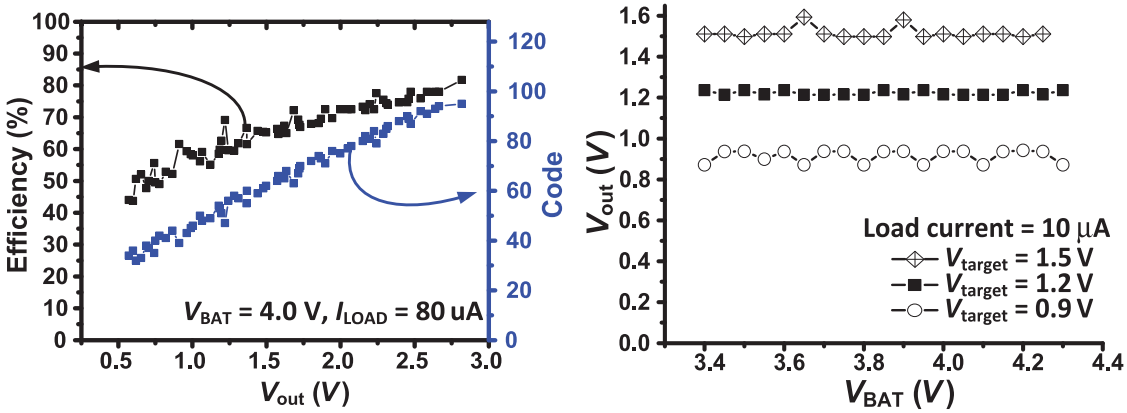

Fig. 21. Efficiency and code versus V_{OUT} for the range of $V_{\mathrm{OUT}} = 0.55 - 2.85\,V$ (left), and line regulation for $V_{\mathrm{target}} = 1.5$ V, 1.2 V and 0.9 V (right).

4 V input and $V_{\mathrm{target}} = 1.2$ V. With the load current changes, SWFM is modulated from modes 1 to 3 and the code is adjusted. In this way, V_{OUT} is maintained close to V_{target}. Fig. 22 (right) shows the transient output voltage response for a V_{target} change from 0.9 to 1.5 V when load current is 10 μA. It takes approximately 34 ms to adjust V_{OUT} in the measurement. Response time depends on the feedforward clock frequency, which is divided by 32× from the converter switching clock. Table II provides a comparison of the implemented test chip to other works, including RSC converters that have recently expanded the proposed SAR-based approach by rearranging the switches to improve conversion efficiency [16], [17]. The test chip achieved power density of $0.27\,\mathrm{mW/mm^2}$, which is relatively low because of slow switching frequency and switch sizes set for optimized efficiency at low power load. Faster switching frequency can improve power density.

V. Conclusion

An SAR SC DC–DC converter is proposed for output regulation, providing conversion ratio resolution of $V_{\mathrm{IN}}/2^{\text{number of stages}}$. The SAR SC converter has smaller R_{SSL} than conventional series-parallel SC and ladder SC converters with the same conversion ratio resolution, respectively, by $O(N/\log_2 N)$ and $O(N^4/\log_2 N)$, where $N =$ the number of available conversion ratios. Also, the SAR

TABLE II
COMPARISON TABLE

Metric	This work	[4]	[5]	[16]	[17]
Topology	7-b SAR	Series-parallel	Series-parallel	4-b recursive binary	3-stg recursive ternary
Cascaded SC?	Yes	No	No	Yes	Yes
Closed-loop?	Yes	Yes	Yes	No	No
Input range (V)	3.4 – 4.3	1.2	1.8	2.5	2.5
Output	> 0.45V (in theory, > $V_{BAT}/2^7$)	0.3 – 1.1 V	0.8 – 1 V	0.1 – 2.18 V	0.1 – 2.24 V
Number of conversion ratios	117 (in theory, 127)	6	1	15	45
Step size	31.25 mV at V_{BAT} = 4 V	N/R	N/R	156 mV	~55 mV
I_{LOAD} range	300 µA	1 mA	8 mA	2 mA	1.86 mA
Clock frequency	80 kHz – 2.7 MHz at V_{BAT} = 4 V, V_{target} = 1.2 V	15 MHz	30 MHz	200 kHz –10 MHz	N/R
Peak efficiency	69% at V_{BAT} = 4 V, V_{target} = 1.5 V 65% at V_{BAT} = 4 V, V_{target} = 1.2 V 72% at V_{BAT} = 4 V, V_{target} = 0.9 V	> 70%	69%	85%	86%
Process (nm)	180	180	45	250	250
Area (mm^2)	1.69	2.56	0.16	4.645	4.3
Capacitance (nF)	2.24	2.5	1.234	3	2.8

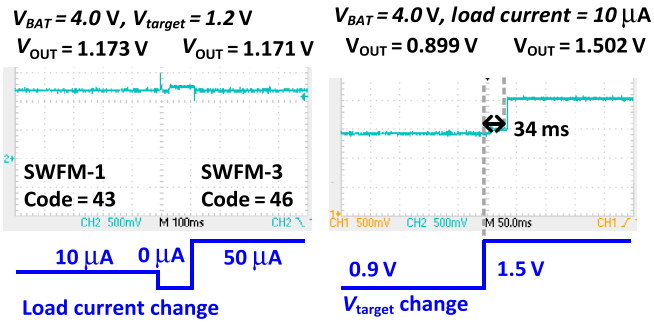

Fig. 22. Transient load step response (left), and transient V_{OUT} response upon V_{target} change (right).

SC converter has P_{BOT} that scales with the number of stages. It was shown that in the moderate load power regime, optimal efficiency can be obtained by scaling frequency with load current change, so that P_{SSL} and P_{BOT} are balanced.

In a test chip fabricated in 180 nm CMOS process, a 7 b SAR SC converter was designed with feedforward and feedback controllers that regulate output voltage with conversion ratio, frequency, and switch width adjustment for operation across a wide range of input and output voltages. The proposed SAR SC converter can generate $2^N - 1$ conversion ratios, and the SC converter in each stage holds a fixed voltage, which can minimize configuration change and stabilization time upon conversion ratio adjustment. This property potentially makes the SAR SC converter a strong candidate for DVS voltage regulation in future work.

REFERENCES

[1] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[2] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% efficiency package bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, Dec. 2013.

[3] J. Xiao *et al.*, "An ultra-low-power digitally controlled buck converter IC for cellular phone applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 383–391.

[4] Y. K. Ramadass and A. P. Chandrakasan, "Voltage scalable switched capacitor DC–DC converter for ultra-low-power on-chip applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2353–2359.

[5] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down DC–DC converter with digital capacitance modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.

[6] T. M. V. Breussegem and M. S. J. Steyaert, "Monolithic capacitive DC–DC converter with single boundary-multiphase control and voltage domain stacking in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1715–1727, Jul. 2011.

[7] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC–DC converter using on-chip ferroelectric capacitors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 374–375.

[8] T. M. Andersen *et al.*, "A sub-ns response on-chip switched-capacitor DC–DC voltage regulator delivering 3.7 W/mm at 90% efficiency using deep-trench capacitors in 32 nm SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 90–91.
[9] R. Jain *et al.*, "A 0.45–1 V fully-integrated distributed switched capacitor DC–DC converter with high density MIM capacitor in 22 nm trigate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.
[10] H.-P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19 W/mm at 73% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 372–373.
[11] V. Ng and S. Sanders, "A 92%-efficiency wide-input-voltage-range switched-capacitor DC–DC converter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 282–283.
[12] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, "A fully integrated successive-approximation switched-capacitor DC–DC converter with 31 mV output voltage resolution," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 370–371.
[13] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
[14] Y.-P. Chen, M. Fojtik, D. Blaauw, and D. Sylvester, "A 2.98 nW bandgap voltage reference using a self-tuning low leakage sample and hold," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2012, pp. 200–201.
[15] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.
[16] L. G. Salem and P. P. Mercier, "A recursive switched capacitor DC–DC converter achieving ratios with high efficiency over a wide output voltage range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, Dec. 2014.
[17] L. G. Salem and P. P. Mercier, "A 45-ratio recursively sliced series-parallel switched-capacitor DC–DC converter achieving 86% efficiency," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.
[18] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC–DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

Suyoung Bang (S'09) received the B.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2010, and the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2013, where he is currently pursuing the Ph.D. degree in electrical engineering.

During his graduate study, he worked with the Circuit Research Labs, IBM, Yorktown Heights, NY, USA, and Intel Corporation, Hillsboro, OR, USA, for on-chip voltage regulator design. His research interests include switched-capacitor DC–DC converter design and analysis, energy-harvesting circuit design, and power management unit design for ultra-low power sensor system.

Mr. Bang received the Doctoral Fellowship from Kwanjeong Educational Foundation in Korea (2010–2014). He was the recipient of the 2012 Intel/Analog Devices/Catalyst Foundation CICC Student Scholarship Award for his work on reconfigurable sleep transistors for GIDL reduction.

David Blaauw (M'94–SM'07–F'12) received the B.S. degree in physics and computer science from Duke University, Durham, NC, USA, in 1986, and the Ph.D. degree in computer science from the University of Illinois, Urbana, IL, USA, in 1991.

After his studies, he worked with Motorola, Inc., Austin, TX, USA, where he was the Manager of the High Performance Design Technology Group. Since August 2001, he has been on the Faculty with the University of Michigan, Ann Arbor, MI, USA, where he is a Professor. He has authored over 450 papers and holds 40 patents. His research interests include VLSI design with particular emphasis on ultra-low-power and high-performance design.

Dr. Blaauw was the Technical Program Chair and General Chair for the International Symposium on Low Power Electronic and Design. He was also the Technical Program Co-Chair of the ACM/IEEE Design Automation Conference and a member of the ISSCC Technical Program Committee.

Dennis Sylvester (S'95–M'00–SM'04–F'11) received the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA, in 1999.

He is a Professor of Electrical Engineering and Computer Science with the University of Michigan, Ann Arbor, MI, USA, and a Director of the Michigan Integrated Circuits Laboratory (MICL). He was a Research Staff with the Advanced Technology Group of Synopsys, Mountain View, CA, USA, and Hewlett-Packard Laboratories, Palo Alto, CA, USA; and a Visiting Professor at the National University of Singapore and Nanyang Technological University, Singapore. He has authored over 375 papers along with 1 book and several book chapters. He holds 20 US patents. His research interests include the design of millimeter-scale computing systems and energy efficient near-threshold computing.

Dr. Sylvester serves as a Consultant and Technical Advisory Board Member for electronic design automation and semiconductor firms in these areas. He cofounded Ambiq Micro, a fabless semiconductor company developing ultra-low power mixed-signal solutions for compact wireless devices. He serves on the technical program committee of the IEEE International Solid-State Circuits Conference and previously served on the executive committee of the ACM/IEEE Design Automation Conference. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CAD and the IEEE TRANSACTIONS ON VLSI Systems, and a Guest Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II. He was the recipient of the David J. Sakrison Memorial Prize for the most outstanding research in the UC-Berkeley EECS Department. He was also the recipient of an NSF CAREER Award, the Beatrice Winner Award at ISSCC, an IBM Faculty Award, an SRC Inventor Recognition Award, eight Best Paper Awards and nominations, the ACM SIGDA Outstanding New Faculty Award, and the University of Michigan Henry Russel Award for distinguished scholarship.