A 110 nW Resistive Frequency Locked On-Chip Oscillator with 34.3 ppm/°C Temperature Stability for System-on-Chip Designs

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***Abstract*— This work presents a sub-μW on-chip oscillator for fully integrated system-on-chip designs. The proposed oscillator introduces a resistive frequency locked loop topology for accurate clock generation. In this topology, a switched-capacitor circuit is controlled by an internal voltage-controlled oscillator (VCO), and the equivalent resistance of this switched-capacitor is matched to a temperature-compensated on-chip resistor using an ultra-low power amplifier. This design yields a temperature-compensated frequency from the internal VCO. The approach eliminates the traditional comparator from the oscillation loop; this comparator typically consumes a significant portion of the total oscillator power and limits temperature stability in conventional RC relaxation oscillators due to its temperature-dependent delay. A test chip is fabricated in 0.18 μm CMOS that exhibits a temperature coefficient of 34.3 ppm/°C with long-term stability of less than 7 ppm (12 second integration time) while consuming 110 nW at 70.4 kHz. A radio transmitter circuit that uses the proposed oscillator as a baseband timing source is also presented to demonstrate a system-on-chip design using this oscillator.**

***Index Terms*— Low power, oscillators, timer, temperature compensation, timer, wireless sensor node.**

I. Introduction

A STABLE clock source is one of the most important requirements for integrated circuit designs. Although recently introduced techniques allow crystal oscillators to provide a very accurate clock while consuming as little as a few nanowatts [1]–[2] for applications such as a Bluetooth Low Energy sleep timer which requires ±500 ppm frequency accuracy, fully integrated on-chip generation of a clock source has become more important as system-on-chip designs have proliferated. More specifically, wireless sensor nodes for Internet-of-Things (IoT) applications have a small form factor and limited board space, making it difficult to integrate crystal oscillators, especially for implantable applications. Fig. 1 compares the physical size of a recently proposed millimeter-sized sensor system that consists of stacked dies with no board mounting [3] with that of a small-sized off-the-shelf crystal [4]. This comparison illustrates the challenge of integrating external crystal oscillators in millimeter-sized IoT devices.

An on-chip oscillator requires low power consumption and energy per cycle, frequency stability over varying ambient temperatures, long-term stability, and low supply voltage sensitivity. On-chip oscillators that consume little power and exhibit low energy per cycle are important for wireless sensor applications such as [5] [6]–[7]. These systems are usually powered by millimeter-sized batteries, and thus, the total energy budget is limited. To reduce power and extend their lifetimes, these systems are highly duty-cycled. They remain in sleep mode the majority of the time and intermittently wake up to measure environmental signals, process the measured data, and wirelessly transmit the data to the outside. As an example, a millimeter-scale wireless imaging system presented in [3] consumes 304 nW in its sleep mode, and an electromagnetic energy harvesting system introduced in [7] requires 190 nW in its idle mode. Low oscillator power consumption is important in a system with low activity where the standby current dominates the total power consumption, as is the case with a wake-up timer or a sleep mode timer. This type of timer is turned on even during sleep mode, when most blocks are power-gated, in order to wake the system periodically, and its power consumption often dominates the total system power consumption in sleep mode.

Low energy consumption per cycle is an important requirement for wireless sensor nodes when the system performs frequent activities and an oscillator's energy consumption can represent a substantial portion of the total system energy. This situation can occur in clocks for a processor, a radio baseband controller, or a power management circuit with switched-capacitor networks. The proposed oscillator is adopted as a clock source to a radio baseband controller [8] which consumes 21.7 nJ/bit. One of the state-of-art switched capacitor DC-DC converters [9] outputs 0.1 nJ/cycle. It implies that the level of energy/cycle of oscillators should be significantly less than 0.1 nJ/cycle to be integrated in such power converter systems. For such applications, the active energy consumption of an oscillator must be kept low because wireless sensor nodes have limited energy budgets.

An oscillator must also show good frequency stability. When implemented in a wake-up timer, an oscillator must maintain a constant system wake-up period across a wide range of temperatures. The frequency stability specification

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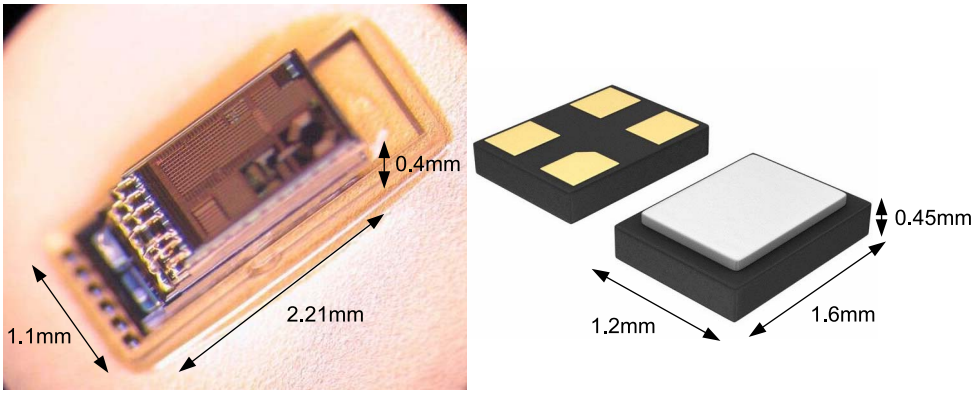

Fig. 1. (a) Photograph of millimeter sized wireless sensor node with no board mounting. (b) Diagram of one of the smallest off-the-shelf crystal components with its size.

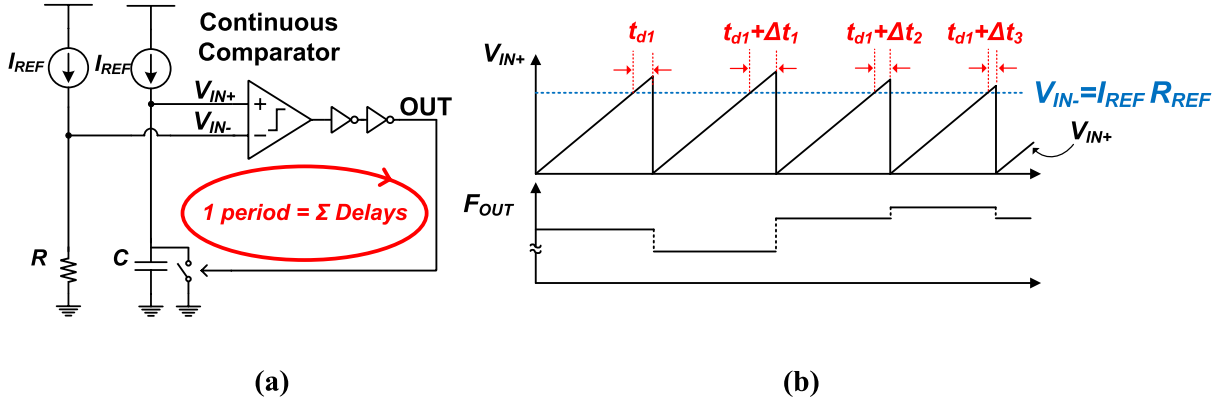

Fig. 2. (a) Conventional RC relaxation oscillator circuit. (b) Its unstable frequency caused by comparator delay variation.

becomes very important when synchronizing nodes for radio transmission. For wireless communication, a transmitter and a receiver must be synchronized to ensure valid data packet transfers. If the oscillators employed in wireless nodes have a high degree of uncertainty and instability, the resulting time window for synchronization must be extended to compensate. Within a packet, the smaller the Allan deviation is, the longer a number of consecutive bits can be transmitted without a separate synchronization header. Between wakeup periods, the frequency drifts due to temperature or supply voltage variations should be smaller than what the receiver can tolerate. More details are explained in Section V. Considering the unstable battery voltage of sensor nodes during their lifetimes and ambient temperature changes that sensors can face, low temperature and supply voltage sensitivity is important.

On-chip clock sources can be generated by various methods such as gate-leakage-based oscillators [10], as well as mobility-based frequency generation, LC oscillators, RC relaxation oscillators, and RC harmonic oscillators as described in [11]. Among the aforementioned approaches, one of the most common structures is an RC relaxation oscillator, illustrated in Fig. 2(a). This conventional RC relaxation oscillator is composed of two identical current sources, a resistor, a capacitor with a reset switch, and a comparator with buffers. The negative input voltage (V_{IN-}) of the comparator is set by the product of the source current (I_{REF}) and the reference resistance (R_{REF}). A source current on the right side charges the capacitor, and the capacitor is reset when a positive input voltage, V_{IN+}, exceeds the threshold voltage (V_{IN-}). The reset signal is generated by the comparator and then buffered by a few inverter stages. In this structure, one clock period is the sum of the RC delay, comparator delay, and buffer delays. The RC delay can be temperature-compensated to the first order fairly easily by serially combining a resistor with a positive temperature coefficient and a resistor with a negative temperature coefficient and trimming the breakdown between the two resistors. On-chip capacitors made of MIM capacitors or traditional metallization layers have negligible temperature coefficients.

However, reducing comparator and buffer delay variation across temperature requires complicated design techniques and remains the main source of temperature instability, as shown in Fig. 2(b). In this figure, the varying comparator delay at each cycle is expressed as Δt_x, and is added to each cycle period (t_{d1}). To address this issue, a feed-forward period control was introduced in [12] to cancel comparator delay variation by measuring it and removing the effect

with boost charging. However, the replica circuits to measure comparator delay nearly double the required area and power. A comparator offset cancellation technique was proposed that switches the comparator input polarity every half period to tackle temperature-dependent comparator offset voltage [13]. However, comparator delay itself remains in the oscillator period, and thus a significant amount of power is consumed to render the delay of comparator and buffers to be less than 0.4% of oscillator period. A current-mode RC relaxation oscillator [14] eliminates capacitor resetting delay by dual-phase operation, but still has comparator delay in the oscillator period. It is important to note that this comparator delay issue creates a power and temperature stability tradeoff relationship in traditional RC relaxation oscillators, meaning that power consumption increases as temperature stability is improved. Another design [15] achieves 38.2 ppm/°C with a circuit technique called local supply tracking threshold voltage, but it relies on a dedicated implant process for a zero temperature coefficient poly resistor, which is not always available in other technologies. A constant charge subtraction method was suggested to address comparator delay variation in [16], but the output frequency is limited by the low power amplifier, producing an 11 Hz clock that can only be used in low frequency applications.

To stabilize comparator delay, a supply-regulated ring oscillator in a temperature compensated loop was introduced in [17]. However, [17] targets a much faster frequency of 10 MHz with a correspondingly much higher power consumption (80 μW) than the work presented here, and also exhibits a relatively high temperature coefficient. An approach that relies on the use of the RC zero voltage crossing time as a timing reference and locks a VCO frequency to this reference time was developed in [18], however the system consumed substantial energy per cycle (11.3 pJ/cycle).

In this paper, a Resistive Frequency Locked on-chip Oscillator (RFLO) is proposed to solve the problems caused by the use of a comparator in existing RC relaxation oscillator structures. This paper is an extension of [19]. This RFLO is based on the principle that a switched-capacitor circuit controlled at a certain frequency can function as a resistor [20]–[21]. The RFLO structure replaces a comparator with an ultra-low power amplifier and uses this amplifier to match the resistance of a switched-capacitor circuit to that of a temperature-compensated on-chip resistor. The frequency of the control signal for the switched-capacitor circuit is the output frequency of this oscillator, and the frequency is stabilized by the resistive frequency locked loop. A recent work [22] embedded a VCO in a feedback loop with a current comparator and a frequency-to-current converter to generate a temperature-compensated clock source. However, that work relies on transistor matchings in a current comparator instead of the active control of an amplifier, resulting in a relatively high temperature sensitivity of 90 ppm/°C and supply voltage sensitivity of 4%/V.

The proposed 70.4 kHz oscillator achieves a temperature sensitivity of 34.3 ppm/°C, supply voltage sensitivity of 0.75%/V, and long term stability of 7 ppm after an integration time of 12 seconds while consuming 110 nW

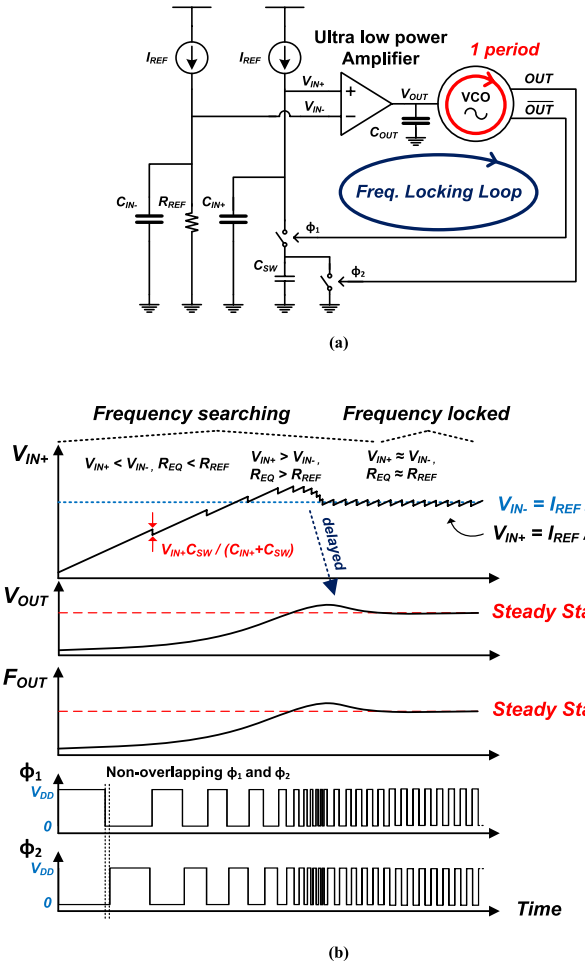

Fig. 3. (a) Circuit diagram of proposed Resistive Frequency Locked on-chip Oscillator. (b) Its conceptual operating waveforms.

at room temperature. This paper is organized as follows. Section II describes the operating principles of the RFLO and its design. Section III describes the sources of temperature-dependent frequency instability and introduces techniques to address each source. Section IV describes the measurement results and chip implementation. Section V shows a radio transmitter circuit integrated with the proposed RFLO as an example of a fully integrated system-on-chip design. Finally, Section VI concludes the paper.

II. Resistive Frequency Locked Oscillator

An RFLO removes the comparator from the oscillation loop and adopts a frequency locked loop with an ultra-low power amplifier. The simplified circuit diagram and its operating waveforms are illustrated in Fig. 3. The basic principle is to generate a stable frequency by matching the equivalent resistance of a switched-capacitor circuit (C_{SW}) to a temperature-compensated on-chip resistor (R_{REF}). A first-order analysis is introduced in this section, followed by an analysis with second-order effects in Section III.

A reference current I_{REF} is injected into R_{REF} to develop a reference voltage $V_{IN-} = I_{REF} \times R_{REF}$,

and this voltage is connected to a negative input of an amplifier. The amplifier forces this voltage to match the voltage of positive input node V_{IN+}, where the same I_{REF} flows through C_{SW}. This V_{IN+}, which is the product of the current and resistance at the node, can be expressed as

$$V_{IN+} = \frac{I_{REF}}{C_{SW} F_{OUT}} \tag{1}$$

because an equivalent resistance of a switched-capacitor circuit operating at a frequency of F_{OUT} is $1/(C_{SW}F_{OUT})$. Here, F_{OUT} is the VCO frequency controlled by the amplifier output, V_{OUT}. By equating V_{IN+} and V_{IN-} as shown in

$$V_{IN+} = V_{IN-} (= I_{REF} R_{REF}) \tag{2}$$

the VCO frequency F_{OUT} is defined by R_{REF} and C_{SW} as derived in

$$F_{OUT} = \frac{1}{R_{REF} C_{SW}}. \tag{3}$$

As the two reference current terms (I_{REF}) in V_{IN+} and V_{IN-} cancel out in the equation, F_{OUT} is insensitive to I_{REF}. Furthermore, assuming the reference currents are independent of the supply voltage, F_{OUT} is also insensitive to supply voltage fluctuation as the supply voltage does not appear in (3). R_{REF} is temperature compensated in this implementation, and C_{SW} is a MIM capacitor with very low temperature dependency, and thus, a highly temperature-stable frequency is generated.

Fig. 3(b) shows the RFLO locking process in time domain, starting from a point where the VCO frequency, F_{OUT}, is lower than the target frequency. In this condition, the charge pumped out of V_{IN+} by C_{SW} is less than the charge flowing in from I_{REF}, and thus, V_{IN+} rises. When V_{IN+} matches V_{IN-}, the VCO frequency can be locked depending on the damping ratio of the frequency locked loop. As an example, an overshooting case is shown in this figure. After V_{IN+} equals V_{IN-}, it slightly exceeds V_{IN-}, and the VCO frequency increases because the VCO is biased at a higher voltage than before. The VCO resets C_{SW} more frequently, and thus, the charge pumped out of V_{IN+} is now greater than the charge flowing in from I_{REF}. Thus, V_{IN+} decreases and again approaches V_{IN-}, and the VCO frequency locks. For more quantitative analysis, impedance at the node V_{IN+} (Z_{VIN+}) and its partial derivative with respect to F_{OUT} can be expressed as

$$Z_{VIN+} = \frac{1}{sC_{IN+}} \parallel \frac{1}{C_{SW} F_{OUT}}$$
$$\frac{dZ_{VIN+}}{dF_{OUT}} = \frac{-C_{SW}}{(sC_{IN+} + C_{SW} F_{OUT0})^2} = \frac{-C_{SW}}{\left(sC_{IN+} + \frac{1}{R_{REF}}\right)^2}. \tag{4}$$

At steady-state, output frequency settles at F_{OUT0}, which is $1/R_{REF}C_{SW}$.

Frequency response of the frequency locked loop is derived in

$$F_{OUT}(s) = A_V \frac{\frac{1}{sC_{OUT}}}{R_{OUT} + \frac{1}{sC_{OUT}}} K_{VCO} I_{REF} \times \left(-\frac{C_{SW}}{\left(sC_{IN+} + \frac{1}{R_{REF}}\right)^2} \right)$$
$$= A_V \frac{1}{1 + sC_{OUT} R_{OUT}} K_{VCO} I_{REF} \times \left(-\frac{C_{SW}}{\left(sC_{IN+} + \frac{1}{R_{REF}}\right)^2} \cdot \right) \tag{5}$$

A_V is an amplifier gain, R_{OUT} (0.3GΩ from simulation) is an amplifier output resistance, C_{OUT} (10 pF) is a capacitor at the node V_{OUT}, and K_{VCO} (1.41 MHz/V from simulation) is the gain of VCO. This loop has one pole at $-\frac{1}{C_{OUT}R_{OUT}}$, and two poles at $-\frac{1}{C_{IN+}R_{REF}}$. The dominant pole is located at $\omega = 330$ rad/s, and two nondominant poles are located at $\omega = 7.5$ k rad/s.

The ripples caused by capacitor switching exist on the V_{IN+} node, but their amplitude is small due to the C_{SW}/C_{IN+} ratio of 0.09 (= 0.9 pF/10 pF). The low bandwidth of the ultra-low power amplifier works as a low pass filter and helps to further reduce ripples and to stabilize F_{OUT}. The amplifier of this design has gain of -9 dB at 70.4 kHz from simulation. C_{OUT} (= 10 pF) and an output resistance of the amplifier (= 0.3GΩ) make a first-order low pass filter with cutoff frequency of 53 Hz, yielding gain of -62 dB at 70.4 kHz. This combination results in a gain of -71 dB at the ripple frequency, suppressing voltage ripple at the node V_{OUT} as low as 4 μV. Two clock signals, $\phi 1$ and $\phi 2$, are non-overlapping clocks. Changes in V_{IN+} and V_{IN-} appear at V_{OUT} with some delays due to the limited bandwidth of the amplifier as shown in Fig. 3(b). However, in a steady state where the frequency is stabilized, this low bandwidth of the amplifier does not disturb accurate clock generation.

The proposed topology has the following key advantages over a traditional RC relaxation oscillator topology. First, it removes the traditional comparator from the oscillation loop, thereby removing the power and temperature stability tradeoff introduced by the comparator. Second, the amplifier, which replaces the power consuming comparator and provides frequency locking, consumes very little power. This is possible because the amplifier must only track the impact of ambient temperature changes on the VCO. These temperature changes are slow, and hence the amplifier can be low-bandwidth and ultra-low power. Third, this structure shows good long-term stability. Any slight deviation in frequency in a particular cycle i results in a slight difference in the charge flowing into and out of node V_{IN+}(the charge is noted as ΔQ_i). Unlike a traditional relaxation oscillator in which the circuit is reset every cycle, and hence the charge discrepancy is lost, this topology carries ΔQ_i over from one cycle to the next and accumulates it on

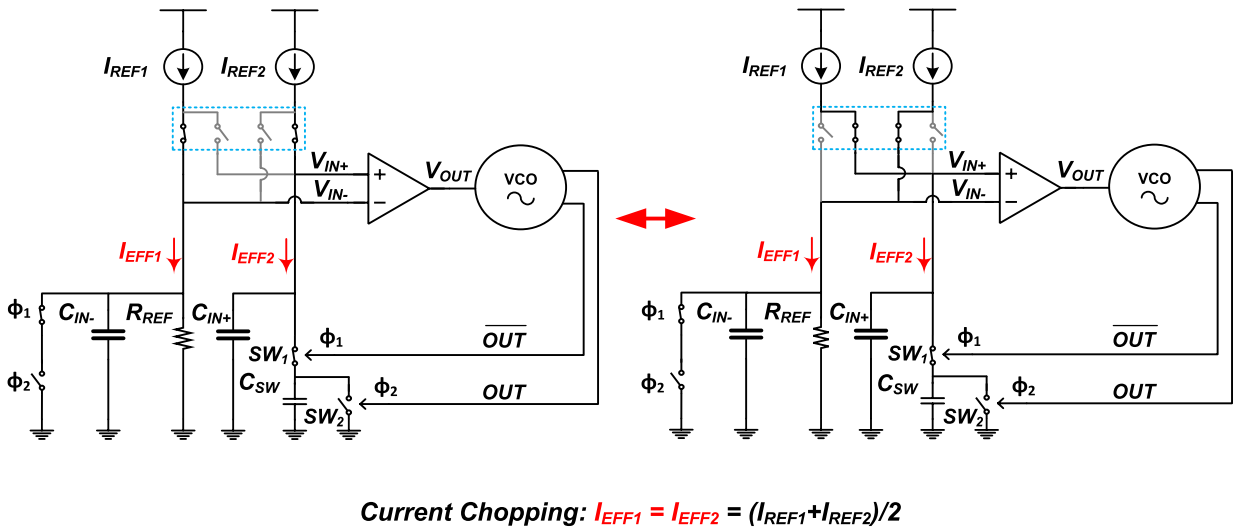

Fig. 4. A schematic of current chopping technique.

capacitor C_{IN+}, as shown in

$$V_\Delta = \sum_{i=0}^{N} \frac{\Delta Q_i}{C_{IN+}}, \quad \text{for N cycles.} \tag{6}$$

If most of the frequency error comes from random noise sources, the sum of ΔQ_i over many cycles approaches zero, resulting in a V_Δ of nearly 0V.

Even with a non-zero V_Δ after N cycles, the amplifier compensates for the error by adjusting the frequency in subsequent cycles, providing excellent long-term frequency stability. The frequency stability after long integration time is mainly limited by flicker noise. Also, an amplifier offset varying over time, long-term drifts of resistors and capacitors can be the sources of the long-term frequency inaccuracy. Finally, this structure shows low supply voltage sensitivity because the frequency is only defined by R_{REF} and C_{SW}, as shown in (3) in the first order analysis. In the second order, gain and an offset voltage of the amplifier slightly vary with the supply voltage. I_{REF}s generated by an internal current reference circuit change with the supply voltage affecting the amplifier DC input operating points. These nonidealities affect how accurately V_{IN+} and V_{IN-} match which defines the frequency accuracy. The VCO frequency is controlled by the amplifier output voltage, and this bias voltage is automatically adjusted by a frequency locked loop when the supply voltage changes.

III. Sources of Temperature Instability and Solutions

This section discusses possible sources of temperature instability in the proposed RFLO design and describes solutions for each source. To begin with, F_{OUT} is only defined by $1/R_{REF}C_{SW}$ under ideal conditions. While MIM capacitors have a very low temperature coefficient, on-chip resistors show a nonzero temperature coefficient. In this work, a negative temperature coefficient (TC) poly resistor without silicide is serially combined with a positive TC diffusion resistor without silicide in order to cancel their temperature dependencies [12]. The ratio between the two resistors is 2-point on-chip trimmed after fabrication to compensate for chip-to-chip process variation. Typical values for a poly resistor and a diffusion resistor are 11.8 and 1.5 MΩ, and a typical current value for each I_{REF} is 12nA. For the diffusion resistor, leakage current through a reverse-biased well diode introduces a non-linear temperature dependency as much as 0.18% of voltage error across the resistor at 80 °C in simulation. This error translates to 14.6 ppm/°C of frequency inaccuracy. Furthermore, as this error is nonlinear, it cannot be effectively corrected by two point on-chip trimming. A segmented N-well technique shown in Fig. 4 [16] is adopted to address this well leakage current, increasing the maximum operating temperature from 50 °C to 80 °C in simulation. Figs. 4(a) and (b) illustrate a schematic and a cross-section of a physical layout of the segmented N-well technique, respectively. For a diffusion resistor, the leakage current of a reverse-biased diode increases as the voltage difference between P+ diffusion and the N-well increases. With this technique, the diffusion resistor is divided into two segments so that the maximum voltage difference is reduced by half. In addition, the inserted buffers prevent leakage currents into the N-well from altering the total current flowing through Terminal A to Terminal B, as shown in Fig. 4. Power and area overhead for this technique are 0.1% and 3.4% of the total circuit.

Mismatch between I_{REF1} and I_{REF2} does not affect temperature stability if the mismatch is constant across temperature; a fixed current mismatch only introduces a fixed frequency offset. However, if the current mismatch varies over temperature, it impacts the temperature stability of F_{OUT}. To address this problem, two current sources, I_{REF1} and I_{REF2}, alternate their connections to each input node of the amplifier as illustrated in Fig. 5. VCO outputs control this alternation. Each amplifier input node is connected to I_{REF1} for one half of its operating time and to I_{REF2} for the other half of its operation. As a result of this chopping scheme, the effective current at each input is the average of I_{REF1} and I_{REF2}, removing frequency errors caused by current mismatch.

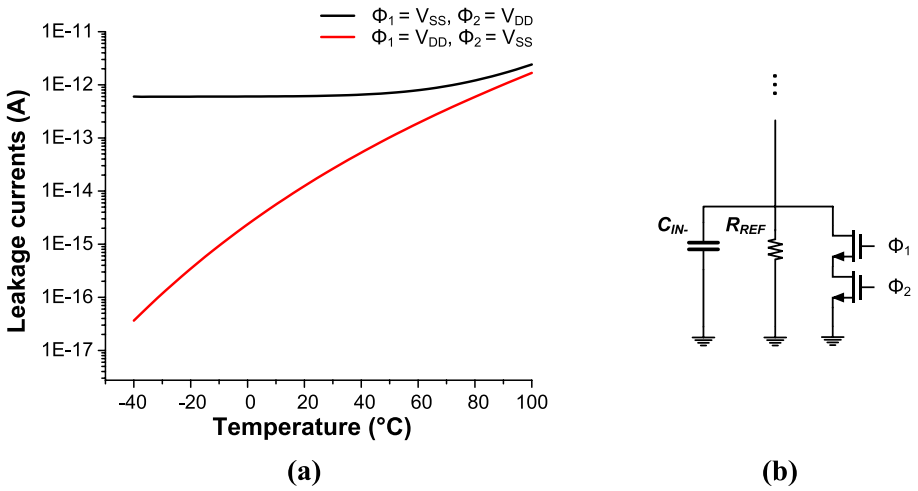

Fig. 5. (a) Simulation results of leakage current of Switches 1 and 2 at different temperatures. (b) A schematic of dummy switches.

Switches, shown as $SW_{1,2}$ in Fig. 5, also have minor impact on temperature stability. If the V_{IN+} or V_{IN-} levels change, the switch parasitic capacitance (C_{PAR}), which consists of transistor gate-to-drain and body-to-drain capacitances, varies non-linearly and alters the total capacitance at V_{IN+}. To reduce this effect, C_{SW} is sized so that C_{PAR} is less than 0.02% of C_{SW}. In addition to this parasitic capacitance issue, the leakage current (I_{leak}) of $SW_{1,2}$ should be properly dealt with. I_{leak} increases from sub-pA levels at −20 °C to ∼2 pA at 80 °C in simulation as shown in Fig. 6 (a), which can create 167 ppm of frequency inaccuracy. The magnitude of I_{leak} differs by switching phases. I_{leak} changes the effective current at V_{IN+} node and worsens temperature stability. To address this effect, identical dummy switches are added at the V_{IN-} node as shown in Fig. 6(b). The following equations summarize how the described current-chopping technique and dummy switches eliminate error sources for frequency accuracy. Equation (7) describes the effective current flowing at V_{IN-} node considering current chopping and switch leakage current as follows:

$$V_{IN-} = \left(\frac{I_{REF1} + I_{REF2}}{2} - I_{leak}\right) R_{REF}. \tag{7}$$

The same amount of current flows through V_{IN+} as described in

$$V_{IN+} = \frac{\frac{I_{REF1}+I_{REF2}}{2} - I_{leak}}{F_{OUT} \times C_{SW}}. \tag{8}$$

As a result, two identical effective currents are cancelled in

$$F_{OUT} = \frac{\frac{I_{REF1}+I_{REF2}}{2} - I_{leak}}{\left(\frac{I_{REF1}+I_{REF2}}{2} - I_{leak}\right) \times R_{REF} \times C_{SW}} = \frac{1}{R_{REF} \times C_{SW}}, \tag{9}$$

and the first-order errors affecting F_{OUT} are mitigated.

The amplifier used in the proposed design is a 1-stage folded cascode structure operating in the subthreshold region [Fig. 7(a)]. This amplifier provides 85 dB DC gain, 1.8 kHz bandwidth, and wide output range of 0.4-0.8 V while consuming only 3.6 nW at room temperature in simulation. An offset voltage of this amplifier (V_{OS}) does not affect temperature stability if V_{OS} is constant over temperature. However, V_{OS} drift over temperature affects temperature stability. Average values of Monte Carlo simulation results of V_{OS} at different temperatures are shown in Fig. 7(b) and a histogram of the total V_{OS} drift from −40 °C to 80 °C of 5,000 run Monte Carlo simulation is shown in Fig 7(c). The average V_{OS} drift is 0.298 mV, which corresponds to 16.7 ppm/°C. An auto-zeroing technique introduced in [19] can reduce V_{OS} itself and V_{OS} drift, but if the V_{OS} changes linearly with temperature, it can be cancelled out by 2-point on-chip trimming in the first order without overhead of auto-zeroing. Simulation results in Fig. 7(d) show that 87% of 5,000 Monte Carlo runs have R-squared value greater than 0.99 (the closer R-squared value is to 1, V_{OS} with respect to temperature is more linear), and the average value of R^2 is 0.993, which de-emphasizes necessity of auto-zeroing. A finite gain of the amplifier (A_V) also generates a frequency offset, and the resulting frequency at steady state is derived in

$$V_{IN+}\left(=\frac{I_{REF}}{C_{SW}F_{OUT}}\right) = \left(1 + \frac{1}{A_V K_{VCO}}\right) V_{IN-} + V_{OS} = \left(1 + \frac{1}{A_V K_{VCO}}\right) I_{REF} R_{REF} + V_{OS} \tag{10}$$

$$F_{OUT} = \frac{1}{\left(1 + \frac{1}{A_V K_{VCO}}\right) C_{SW} R_{REF} + \frac{V_{OS}}{I_{REF}} C_{SW}}. \tag{11}$$

An error from the finite gain decreases as A_V and K_{VCO} increases, and an error from V_{OS} decreases as I_{REF} increases. Each current source is simplified to I_{REF} as current non-idealities are already analyzed in Equation (9).

Fig. 8 describes a bias voltage generation circuit for this amplifier. The 1nA current references described in Fig. 8 are implemented on-chip with the resistor-less techniques introduced in [23].

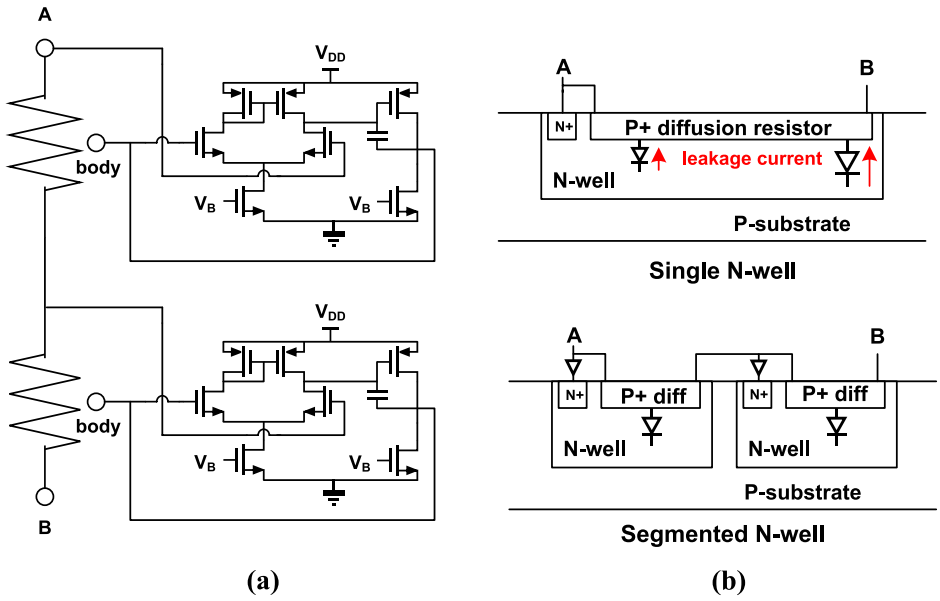

Fig. 6. (a) Schematic of segmented N-well technique to address well leakage current. (b) Cross section of segmented N-well technique shown as a physical layout.

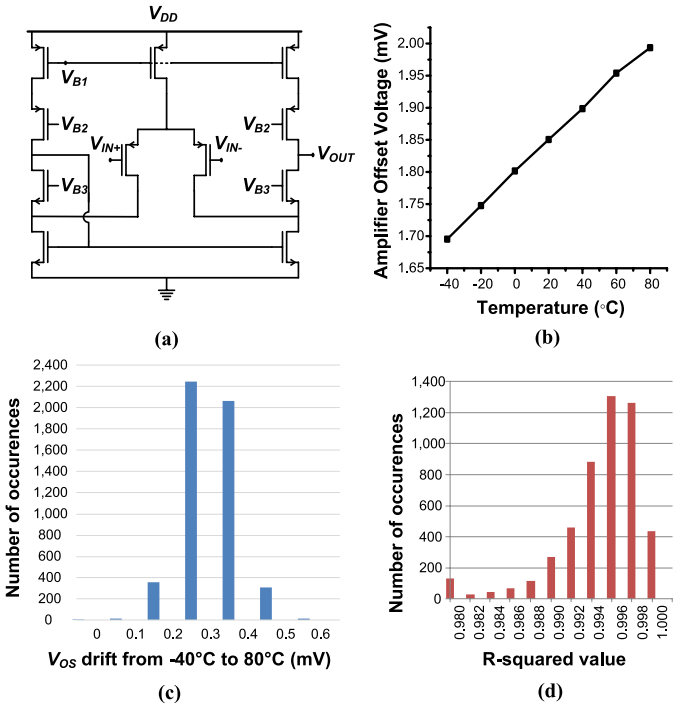

Fig. 7. (a) Schematic of a subthreshold mode ultra-low power amplifier. (b) An average result of Monte Carlo simulation of the amplifier offset voltage at different temperatures. (c) Histogram of total V_{OS} drift from -40 °C to 80 °C of each Monto Carlo runs (total 5,000 runs). (d) Histogram of R-squared value (offset voltage vs. temperature) of each Monto Carlo runs (total 5,000 runs).

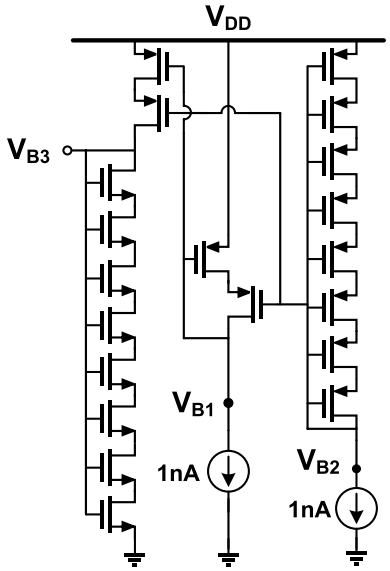

Fig. 8. A bias voltage generation circuit for the ultra-low power amplifier in Fig. 7.

IV. Measurement Results

Fig. 9 shows a circuit diagram of the VCO used in this work. This VCO operates rail-to-rail with a wide frequency range and low power consumption. The VCO frequency is designed to be highly sensitive to bias voltage V_{OUT}. This high sensitivity relaxes the required output operating range of the amplifier. To achieve this high frequency sensitivity to bias voltage, the delay of the first four stages is designed to be exponential with V_{OUT} using high V_T NMOS transistors operating in their subthreshold region where drain current is exponential with gate-to-source voltage. The next four stages are buffers to restore the slew rate with low short-circuit current. The first stage is a stacked inverter with high V_T devices, the second stage is an inverter with high V_T devices, and the last 2 stages are inverters with normal V_T devices. Using this manner of staged output buffers reduces VCO power (10.3 nW in simulation) by 67× at a supply voltage of 1.2V through minimizing the short-circuit current while reducing the signal transition time. As F_{OUT} is set by $1/R_{REF}C_{SW}$ and controlled in a closed loop, the RFLO does not require the VCO to have a linear voltage-frequency relation, thereby relaxing the VCO specification.

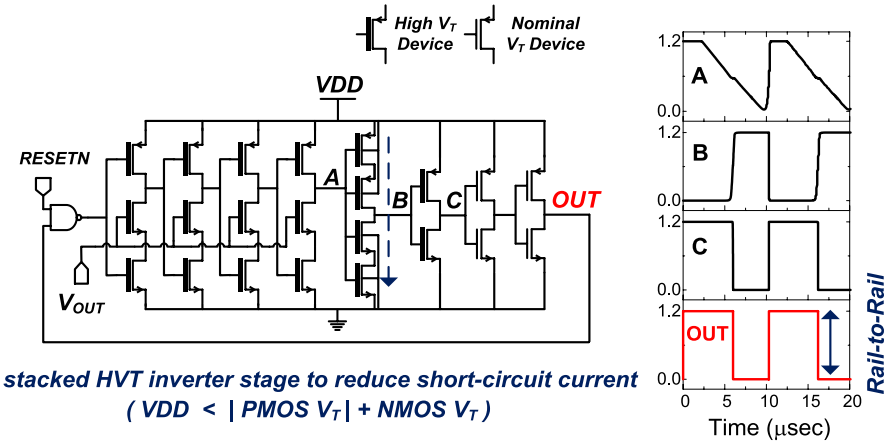

Fig. 9. A schematic of rail-to-rail voltage controlled oscillator and its simulated waveforms.

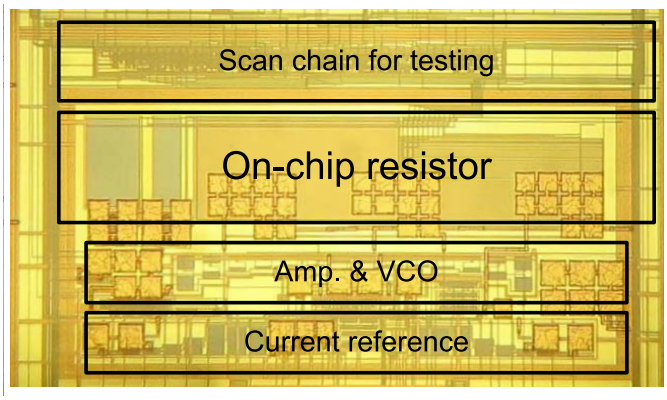

Fig. 10. Die photograph of the proposed RFLO in 0.18 μm CMOS.

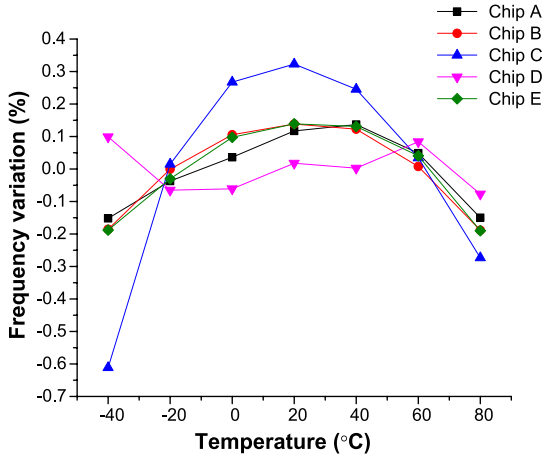

Fig. 11. Measured frequency variation with respect to temperature.

The proposed design was fabricated in 0.18 μm CMOS with total area of 0.26 mm^2. Fig. 10 shows the die photograph. The area occupied by transistors can be reduced by porting this design to advanced technologies. The total area can be further reduced by adopting a duty-cycled resistor technique [24] as the temperature compensated on-chip resistor occupies 0.11 mm^2 (42.3% of the total area) in this design. The duty-cycled resistor technique increases an equivalent resistance

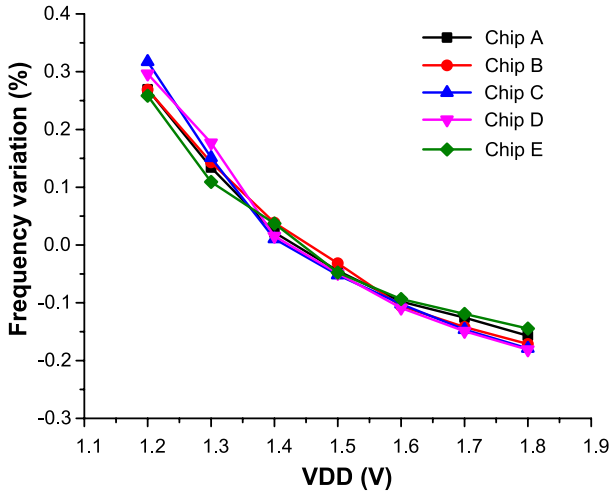

Fig. 12. Measured frequency variation with respect to supply voltage.

of a resistor by 1/duty cycle. The clock frequency of this design is 70.4 kHz and has an average temperature stability of 34.3 ppm/°C between −40 °C and 80 °C for five measured chips as shown in Fig. 11. The ratio of the positive TC on-chip resistor to negative TC resistor is trimmed on-chip at 2 temperatures to have the lowest TC, and the same single setting is maintained for the entire temperature range. The measured frequency is not calibrated off-chip after measurements. This temperature coefficient is the lowest among the reported sub-μW on-chip oscillators shown in Table I. The lowest temperature coefficient measured among the five samples is 14.7 ppm/°C from Chip D, where the first and second order temperature dependencies are cancelled, and the remaining higher order temperature dependencies are exhibited. The clock frequency shows an average supply voltage sensitivity of 0.75%/V in the range of 1.2–1.8 V for the five chips measured, as shown in Fig. 12. A typical supply voltage is 1.3 V. In this fabrication process, nominal V_T devices and high V_T devices in Fig. 9 are 1.8 V devices and 3.3 V IO devices, respectively. All transistors in the amplifier, the amplifier bias generator in Fig. 8, current references, switches for the switched capacitor resistor are 3.3 V IO high V_T devices.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	This work	[12]	[13]	[14]	[15]	[16]	[10]
Process (nm)	**180**	90	65	180	65	180	130
Frequency (Hz)	**70,400**	100,000	18,500	122,000	33,000	11	0.37
TC (ppm/°C)	**34.3**	104.6	38.5	327	38.2	45	375(31[1])
Temp Range (°C)	**-40–80**	-40–90	-40–90	-20–100	-20–90	-10–90	-20–60
Line sensitivity (%/V)	**0.75**	9.4	1	6	0.09	1	490
Power (nW)	**110**	280	120	14.4	190	5.8	0.66[2]
Energy/Cycle (pJ/Cycle)	**1.56**	2.80	6.49	0.12	5.76	527.27	1,783.8
Long term stability (ppm)	**< 7**	N/A	< 20	< 40	< 4	< 15	N/A
Number of samples	**5**	1	1	1	5	5	1
Start-up time (s)	**< 2.5m**	10μ	N/A	N/A	N/A	N/A	N/A
Area (mm^2)	**0.26**	0.12	0.032	0.03	0.015	0.24	0.015

[1] With 10 point calibration using temperature sensor.
[2] Power consumption of temperature sensor is not included.

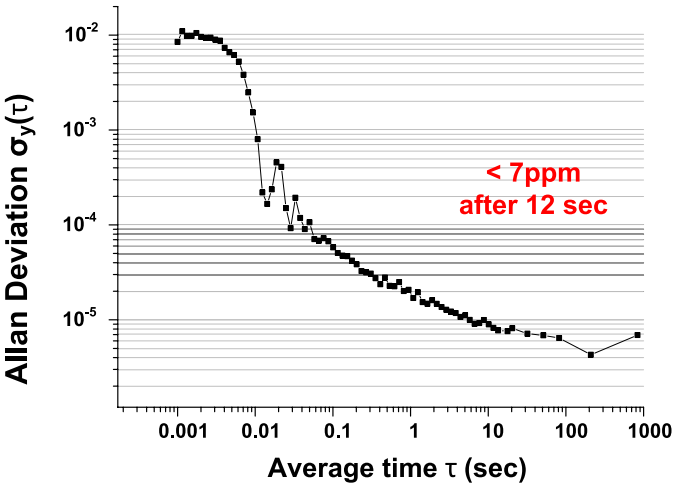

Fig. 13. Measured Allan Deviation.

A digital controller that generates current chopping signals and switch control signals from VCO outputs is composed of only 1.8 V nominal V_T devices. 1.8 V devices are designed to work up to 1.8 V, but for testing, in the short-term, the circuit operated up to 3 V without reliability issues. We used up to 3 V to more extensively verify the circuit techniques for supply sensitivity. The long-term stability (Allan deviation) is less than 7 ppm for an integration time of longer than 12 seconds, as shown in Fig. 13. This long-term stability is the second best among the prior state-of-the-art sub-μW on-chip oscillators.

It is important to analyze how each error sources contribute to absolute frequency inaccuracy. From the measurement results, a typical commercial temperature range of 70°C results in an inaccuracy equivalent to 479.5 mV supply voltage change for the proposed oscillator. Hence, with a typical supply voltage of 1.3 V of this oscillator, the line sensitivity is less critical than the temperature coefficient, as 40% of supply

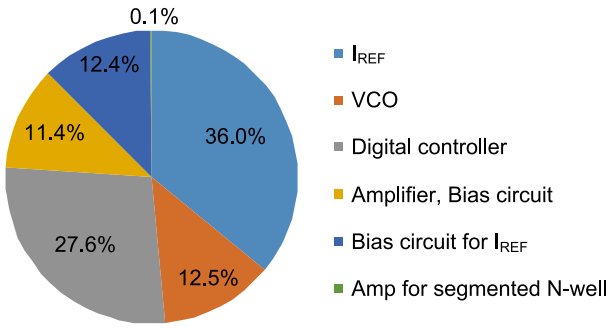

Fig. 14. Breakdown of power consumption.

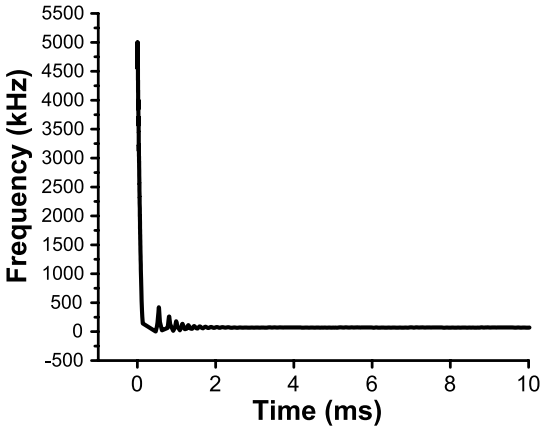

Fig. 15. Measured start-up response of the proposed oscillator.

voltage fluctuation is not usually expected. The temperature coefficient and line sensitivity can be directly compared with each other because both measure instant frequency change due to short-term changes. Allan deviation measures stability due to noise processes rather than environmental effects. Given that, to reduce the line sensitivity further to the level of Allan deviation, embedding a linear regulator can be one option at the expense of some power overhead and actually, we adopted a linear regulator for system integration as described in Section V. Alternatively, temperature and voltage sensitivity can be further reduced using more extensive on-chip trimming as previous works such as [10] executed.

The design consumes 110 nW at room temperature, yielding the second lowest energy consumed per cycle, 1.56 pJ/cycle, among the previous works listed in Table I. Power consumption for each part of the oscillator is described in Fig. 14. A digital controller in the pie chart generates switch control signals and current chopping control signals from VCO outputs. A start-up response is measured as shown in Fig. 15. From this figure, frequency overshoots multiple times before it settles. The frequency locked loop is under-damped from the measurement and the start-up latency is less than 2.5 ms. This latency can be shortened by increasing the frequency locked loop bandwidth and a damping ratio of the loop, but it is only allowed as long as the loop stays stable.

V. SYSTEM INTEGRATION

The proposed RFLO is integrated in a single-chip radio system for wireless sensor nodes [8] demonstrating its capability

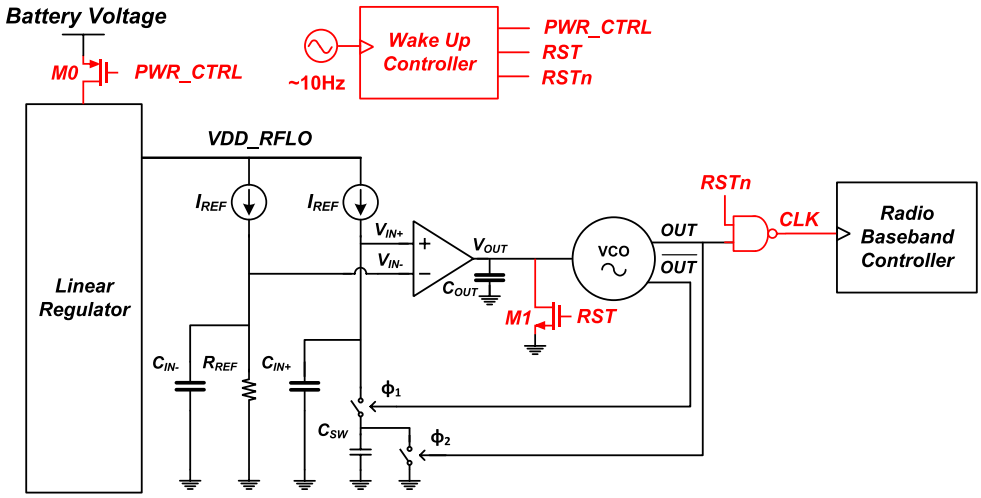

Fig. 16. An RFLO combined with a wake-up controller to function as a clock source for radio baseband controller.

to serve as an on-chip clock for a radio baseband controller. A substantial level of frequency accuracy is required for the radio baseband timer since the baseband controller determines the bit rate which needs to match the bit rate of the paired transceiver so that the data modulation/demodulation does not fall out of synchronization. The accuracy of the baseband timer therefore directly impacts the length of the data packet that can be transmitted. This radio implements pulse position modulation (PPM) with pulse position resolution (T_{PR}) of 4μs and separation between bits (T_{SP}) of 128μs. For M-ary PPM, a symbol length (T_{SYM}) is $M \times T_{PR}+T_{SP}$. A jitter for the Nth symbol position is $N \times T_{SYM}$ multiplied by Allan deviation ($\sigma_{y(N\times TSYM)}$) at integration time of $N \times T_{SYM}$. This jitter should be less than T_{PR} as derived in

$$\frac{T_{PR}}{NT_{SYM}} < \sigma_{y(NT_{SYM})}. \tag{12}$$

With higher N or longer T_{SYM}, this condition becomes harder to satisfy as the Allan deviation improves only sub-linearly with increasing integration time. The radio system requires a packet of 192 bits, and it is able to communicate with T_{SYM} of 136 μs, but bit errors occur with longer T_{SYM}. This corresponds to the proposed calculation as T_{PR} /NT_{SYM} is 153.2 ppm and Allan deviation at integration time of 26.1ms from Fig. 13 is in the range of 150– 200 ppm. For more conventional M-PPM modulation, T_{PR} is T_{SYM} /2 and T_{SP} is 0, simplifying (12) to

$$\frac{1}{2N} < \sigma_{y(NT_{SYM})}. \tag{13}$$

In this prototype, a FPGA-based demodulation code can tolerate a center frequency drift of ±2000 ppm (±500 Hz). Between wakeup periods, if temperature changes by ±58.3°C or the supply voltage fluctuates by ±267 mV, communication fails. To compare this work with previous generations, the oscillator with similar power consumption [13] can operate in the same system within ±51.9 °C temperature variation and ±200 mV supply voltage change. Allan deviation near integration time of 26.1 ms (estimated from their figure) is similar to this work. However the long term Allan deviation is 2.9× higher than this work, lowering N or T_{SYM} by the same ratio.

Unlike conventional radio systems that adopt a crystal oscillator as a clock source, this work is fully integrated, reducing the volume of a millimeter-scale system. An important component required to integrate an RFLO within a wireless sensor node is a wake-up controller, as the sensor node periodically sleeps and the wake-up timer will enable the RFLO during active periods only. The key functions of the wake-up controller are minimizing RFLO power consumption during the system sleep mode and ensuring that upon wake-up the RFLO clock feeds into the system only after it is stabilized. An RFLO combined with a wake-up controller is shown in Fig. 16. During the system's sleep mode, RFLO leakage current is constrained to 20 pA (simulated value) by M0, a high threshold voltage PMOS header. The VCO control voltage (V_{OUT}) is clamped to ground by M1, a high threshold voltage NMOS.

At the beginning of wake-up mode, a linear regulator is powered and generates a supply voltage (*VDD_RFLO*) for the RFLO from the battery voltage. This takes approximately 300 ms, mostly due to the slow stabilization of the voltage reference inside the linear regulator; the reference is not explicitly shown in the figure as it is not the main focus of interest. Using a linear regulator improves frequency stability with respect to supply voltage and jitter performance at the cost of power overhead. A sub-100-pA watchdog timer with a 10-Hz frequency is implemented to measure the *VDD_RFLO* stabilization time. After *VDD_RFLO* is stabilized, the wake-up controller toggles *RST* to low, causing the VCO to start oscillation after which the VCO frequency converges to the target value by the frequency locked loop. Before the frequency stabilizes at its target frequency, the clock is isolated from the radio system with a NAND gate. Simulation verified that a maximum of 600 cycles is required to stabilize the RFLO. An internal counter connected to the RFLO counts

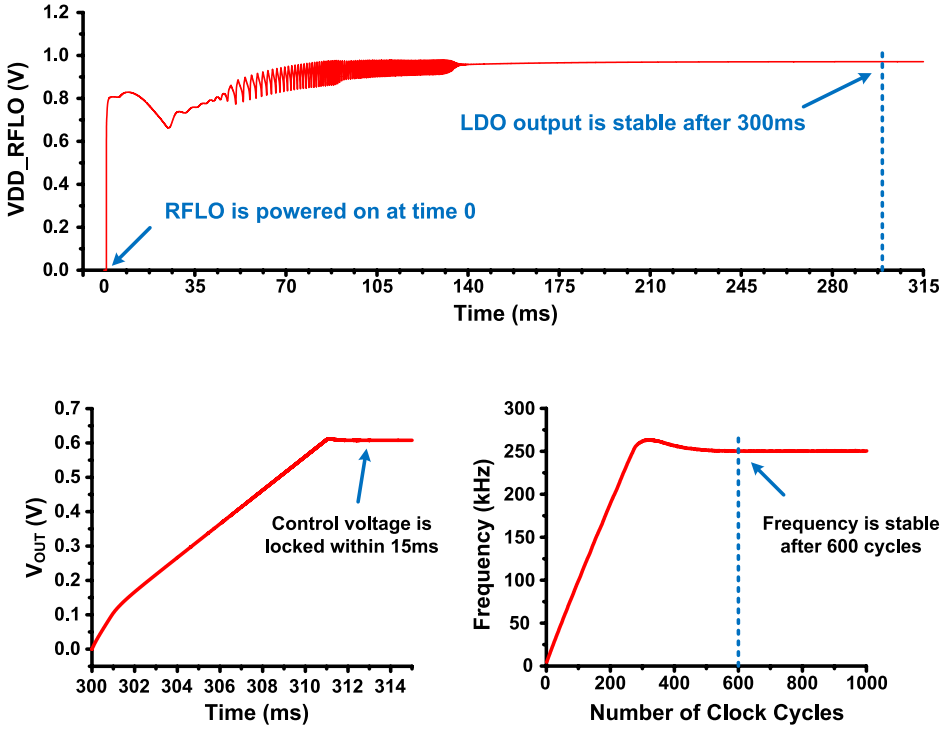

Fig. 17. Simulation results a RFLO supply voltage (*VDD_RFLO*), a VCO control voltage (V_{OUT}), and a frequency of a RFLO during a wake up period.

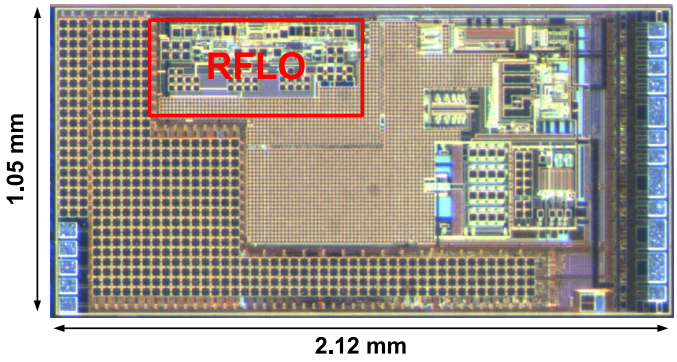

Fig. 18. Die photograph of a radio system integrated with a RFLO.

to 600, after which the RFLO clock is fed into the baseband controller of the radio system. Fig. 17 shows simulated results of *VDD_RFLO*, V_{OUT}, and RFLO frequency during a wake up period. In order to meet the required frequency of the radio system, C_{SW} is reduced by 3.5 times, yielding 250 kHz clock frequency. A lower *VDD_RFLO* of 1 V is used as this is the voltage level the radio system could provide. Simulated power consumption of the oscillator is 110 nW.

For the 300 ms required for *VDD_RFLO* stabilization, the entire system shown in Fig. 16 consumes 35 nJ, while during the additional 600 cycles needed for RFLO stabilization the entire system consumes an additional 1.6 nJ, which is only 7.4% of 1 bit transmission. This 36.6 nJ of total energy consumption during the stabilization period corresponds to less than 2 equivalent transmitted bits of wake-up overhead as a transmission energy consumption is 21.7 nJ/bit. However, reducing the stabilization time for a RFLO is still an important issue for systems that periodically sleep and wakeup, and it can be an interesting future work. This radio system was fabricated in 0.18 μm CMOS technology, and a die photograph is shown in Fig. 18.

VI. Conclusion

An RFLO is introduced in this work. The proposed topology removes the comparator present in traditional RC relaxation oscillators, which is one of the main sources of temperature instability. Instead, an ultra-low power amplifier forms a frequency locking loop with a switched-capacitor circuit to generate a temperature-compensated clock signal. This oscillator produces a 70.4 kHz clock with an average temperature coefficient of 34.3 ppm/°C in the −40 °C to 80 °C range, an average supply voltage sensitivity of 0.75%/V in the 1.2 V to 1.8 V range for five samples, and long-term stability of less than 7 ppm after an integration time of 12 s while consuming 110 nW at room temperature. By avoiding external components, this oscillator targets fully integrated system-on-chip designs, and a radio transmitter system integrated with the oscillator is implemented and characterized.

References

[1] D. Yoon, D. Sylvester, and D. Blaauw, "A 5.58 nW 32.768 kHz DLL-assisted XO for real-time clocks in wireless sensing applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 366–368.

[2] K.-J. Hsiao, "17.7 A 1.89 nW/0.15V self-charged XO for real-time clock generation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 298–299.

[3] G. Kim *et al.*, "A millimeter-scale wireless imaging system with continuous motion detection and energy harvesting," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2014, pp. 1–2.

[4] Ultra Miniature Ceramic SMD Crystal, ABM12 Datasheet, Abracon LLC, Irvine, CA, USA, Sep. 2012.

[5] Y.-P. Chen *et al.*, "An injectable 64 nW ECG mixed-signal SoC in 65 nm for arrhythmia monitoring," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 375–390, Jan. 2015.

[6] Y. Lee *et al.*, "A modular 1 mm3 die-stacked sensing platform with low power I^2C inter-die communication and multi-modal energy harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 229–243, Jan. 2013.

[7] H. Reinisch *et al.*, "An electro-magnetic energy harvesting system with 190 nW idle mode power consumption for a BAW based wireless sensor node," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1728–1741, Jul. 2011.

[8] Y. Shi *et al.*, "A 10 mm3 syringe-implantable near-field radio system on glass substrate," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 448–449.

[9] W. Jung *et al.*, "A 60%-efficiency 20nW-500 μW tri-output fully integrated power management unit with environmental adaptation and load-proportional biasing for IoT systems," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 154–155.

[10] Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, "A 660pW multi-stage temperature-compensated timer for ultra-low-power wireless sensor node synchronization," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 46–48.

[11] S. M. Kashmiri and K. A. A. Makinwa, *Electrothermal Frequency References in Standard CMOS*. New York, NY, USA: Springer-Verlag, 2013.

[12] T. Tokairin *et al.*, "A 280nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2012, pp. 16–17.

[13] A. Paidimarri, D. Griffith, A. Wang, A. P. Chandrakasan, and G. Burra, "A 120 nW 18.5kHz RC oscillator with comparator offset cancellation for ±0.25% temperature stability," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 184–185.

[14] S. Dai and J. K. Rosenstein, "A 14.4 nW 122 KHz dual-phase current-mode relaxation oscillator for near-zero-power sensors," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–4.

[15] D. Griffith, P. T. Røine, J. Murdock, and R. Smith, "A 190nW 33kHz RC oscillator with ±0.21% temperature stability and 4ppm long-term stability," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 300–301.

[16] S. Jeong, L. Inhee, D. Blaauw, and D. Sylvester, "A 5.8 nW CMOS wake-up timer for ultra-low-power wireless applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1754–1763, Aug. 2015.

[17] J. Lee and S. Cho, "A 10MHz 80 μW 67 ppm/°C CMOS reference clock oscillator with a temperature compensated feedback loop in 0.18 μm CMOS," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2009, pp. 226–227.

[18] J. Lee, P. Park, S. Cho, and M. Je, "A 4.7 MHz 53 μW fully differential CMOS reference clock oscillator with −22dB worst-case PSNR for miniaturized SoCs," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[19] M. Choi, S. Bang, T.-K. Jang, D. Blaauw, and D. Sylvester, "A 99 nW 70.4 kHz resistive frequency locking on-chip oscillator with 27.4 ppm/C temperature stability," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2015, pp. C238–C239.

[20] T. O'Shaughnessy, "A CMOS, self calibrating, 100 MHz RC-oscillator for ASIC applications," in *Proc. 8th Annu. IEEE Int. ASIC Conf. Exhibit*, Austin, TX, USA, Sep. 1995, pp. 279–282.

[21] B. R. Gregoire and U.-K. Moon, "A sub 1-V constant G_m-C switched-capacitor current source," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 3, pp. 222–226, Mar. 2007.

[22] K. Ueno, T. Asai, and Y. Amemiya, "A 30-MHz, 90-ppm/°C fully-integrated clock reference generator with frequency-locked loop," in *Proc. IEEE Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2009, pp. 392–395.

[23] M. Choi, I. Lee, T.-K. Jang, D. Blaauw, and D. Sylvester, "A 23 pW, 780 ppm/°C resistor-less current reference using subthreshold MOSFETs," in *Proc. Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 119–122.

[24] T. Jang, M. Choi, S. Jeong, S. Bang, D. Sylvester, and D. Blaauw, "A 4.7nW 13.8 ppm/°C self-biased wakeup timer using a switched-resistor scheme," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 102–103.

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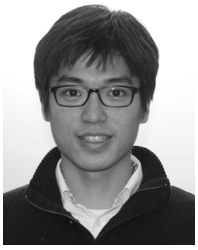

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