Low-Power and Compact Analog-to-Digital Converter Using Spintronic Racetrack Memory Devices

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***Abstract*— Current-induced domain wall (DW) motion in spintronic racetrack memory promises energy-efficient analog computation using compact magnetic nanowires. This paper explores the feasibility of analog-to-digital converter (ADC) based on current-induced DW motion and introduces an n-bit ADC using n racetrack magnetic nanowires. With each magnetic nanowire having a different configuration granularity, an n-bit binary or gray code is generated simultaneously. The proposed ADC structure achieves 21 fJ/conversion-step at 20 MHz with an area of about 10 μm^2. The racetrack ADC is suitable for applications requiring dense ADC arrays, such as image sensors. This paper describes one ultrahigh speed digital pixel sensor imaging system benefiting from the racetrack ADC.**

***Index Terms*— Analog-to-digital converter (ADC), domain wall (DW), emerging circuits and devices, imager sensor, racetrack memory, spin-transfer torque, spintronic.**

I. Introduction

LOW-power and compact data converters are an essential part of sensor nodes as the link between the sensor and data processing. Also, in high-speed massive parallel sensors such as imagers, each photodiode includes a moderate-accuracy but compact analog-to-digital converter (ADC) for parallel data conversion [1]. CMOS implementations of such data converters face two challenges. The first is the difficulty of integrating ADCs with sensors in every pixel or channel due to the large area of analog circuits. This is exacerbated by poor scaling of analog circuits in CMOS due to process variation in advanced technologies [2]. The second is the high static power of analog data converters [3]. As a result, most high-speed image sensors use only column parallel ADCs in their sensor array to balance area/power and performance [4], [5]. However, image sensors with much higher frame rates are in demand for emerging imaging applications such as integral machine vision, time-of-flight imaging, and 3-D high-definition television.

Recently, a number of new materials and novel devices have been proposed to replace MOS transistors in specific applications. The discovery of current-induced domain wall (DW) motion has driven the invention of several spintronic devices that hold promise for nonvolatility, high endurance, high density, and low power [6], [7]. With perpendicular magnetic anisotropy (PMA) in CoFeB/MgO structures, multiple magnetic domains separated by DWs can be maintained in one nanowire for multibit nonvolatile memory [8]–[11]. A four-terminal device mCell using DW switching was proposed for logic computation [12]. DW neurons have also been reported as suitable for current comparison operation and can function as current comparators in SAR ADC [3], [13], [14]. However, the DW neuron ADC does not fully leverage spintronic devices as most parts (including the DAC) are still implemented in CMOS.

This paper presents a novel spintronic-based data converter that leverages the nonvolatility, low power, and high density of spintronic devices. We propose an n-bit racetrack ADC structure using n magnetic nanowires with different configuration granularity for each bit [15]. The current-steering DW motion can convert n bits binary data or gray code in parallel. Exploiting the nonvolatility of racetrack memory, the converted data is stored intrinsically, eliminating the need for additional memory cells and saving time spent on writing data. As most components are spintronic devices, the design achieves compact area, scalability, low static power, and no leakage. Compared to a conventional low-power CMOS SAR ADC, the proposed racetrack ADC can achieve a 1000 $\times$ smaller area with comparable energy efficiency figure-of-merit (FOM). We also describe the potential application of the racetrack ADC to a high-speed imaging system using the 8 bit racetrack ADC as an in-pixel ADC. Results indicate that the frame rate is increased by 50$\times$ compared to a CMOS digital pixel sensor (DPS) while retaining high fill factors as in analog pixel sensors (APSs).

Section II presents the model we developed to describe the relationship between steering current and DW motion velocity in racetrack memory to explore the potential of data conversion with DW motion. Section III shows the basic circuit structure and operations of the proposed ADC. Section IV analyzes the influence of variation, noise, stability, and reliability on the converter. Section V demonstrates simulation results of the proposed design and analyzes the tradeoffs among area, power, performance, and scaling of the ADC. Section VI describes the high-speed imaging system

Manuscript received June 4, 2016; revised August 24, 2016; accepted October 10, 2016. Date of publication December 2, 2016; date of current version February 22, 2017. This work was supported by STARnet, a Semiconductor Research Corporation program sponsored by MARCO and DARPA. *(Corresponding author: Q. Dong.)*

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Digital Object Identifier 10.1109/TVLSI.2016.2622224

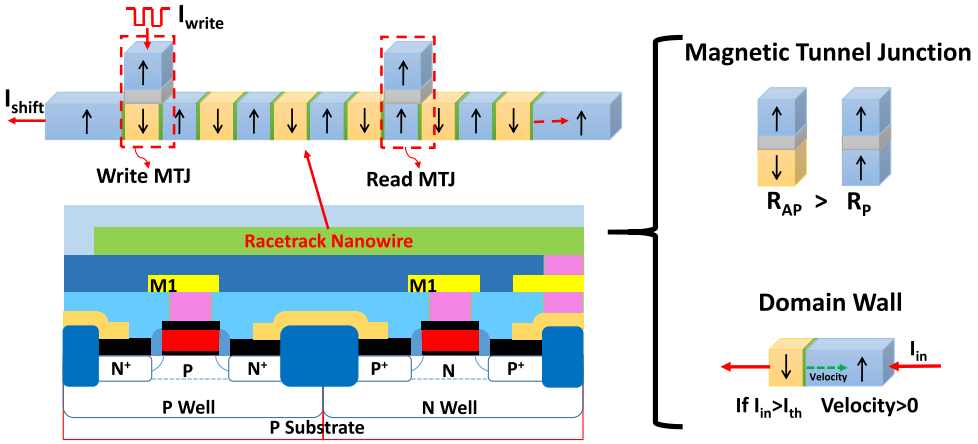

Fig. 1. Structure of a racetrack memory device consisting of a magnetic nanowire and two MTJ heads as the read and write ports. The racetrack nanowire is manufactured on top of MOSFETs, avoiding planar area overhead.

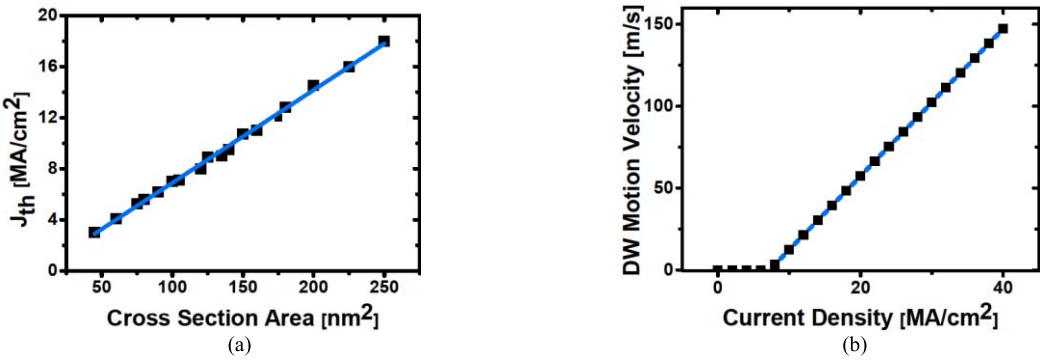

Fig. 2. (a) Threshold current density decreases with reduced cross-sectional area [3], [17]–[19]. (b) Once current density exceeds the threshold, DW motion velocity linearly increases with higher current density based on the compact model in [10].

with the proposed racetrack ADC. The paper is concluded in Section VII.

II. Racetrack Memory Devices

The racetrack memory device is a magnetic nanowire comprising multiple magnet domains separated by DWs [8]–[11]. A single data bit is stored as the local spin polarity within the DW magnet strip at a given position. DWs can be shifted along the magnetic strip by induced horizontal charge current. Fig. 1 shows the structure of a PMA racetrack memory consisting of one magnetic nanowire and two MTJ heads as the read and write ports. Given a current pulse I_{write} on the write MTJ, the magnetic domain beneath that MTJ in the magnetic nanowire will be nucleated through spin-transfer torque. At the same time, the horizontal shift current I_{shift} can move the data along the magnetic stripe. By alternatively asserting write current and shift current, the racetrack can store a sequence of DWs. Previous works have explored the potential of building hundreds of DWs in one magnetic nanowire [8], [11]. With such a high density, the area efficiency can be as high as 1 F^2/bit [10], providing much higher density than other nonvolatile memory technologies. The polarization of the magnetic domain beneath the read MTJ can be detected by sensing the resistance, which is affected through the tunnel magnetoresistance effect. Reported MTJ reading access times for a megabyte-scale array are as fast as 4 ns [16]. Moreover, this device can be implemented above CMOS transistors in the backend process, reducing the total area and interconnection delay.

Spin-dependent electron scattering can cause the charge current through the magnetic nanowire to be spin polarized. When a spin-polarized electron crosses a DW, its spin polarization will rotate 180° from one magnetic domain to the other. To maintain total spin-angular momentum, the change in the current spin-polarization will be transferred to the local magnetization and create a spin-torque, causing the DW to move [8]. The DW moves along the flow of spin-polarized electrons, which is opposite to the direction of the charge current. Both theoretical and experimental studies [3], [17]–[19] have shown that the threshold charge current density for DW motion in a PMA nanowire depends on the nanowire cross-sectional area. According to the adiabatic spin transfer torque model, the threshold current density decreases with reduced width and thickness as shown in Fig. 2(a) [3], [17]–[19]. When the driving current exceeds the threshold current, the DW moves along the nanowire. Higher driving current can generate higher DW motion velocity. Using the compact model in [10],

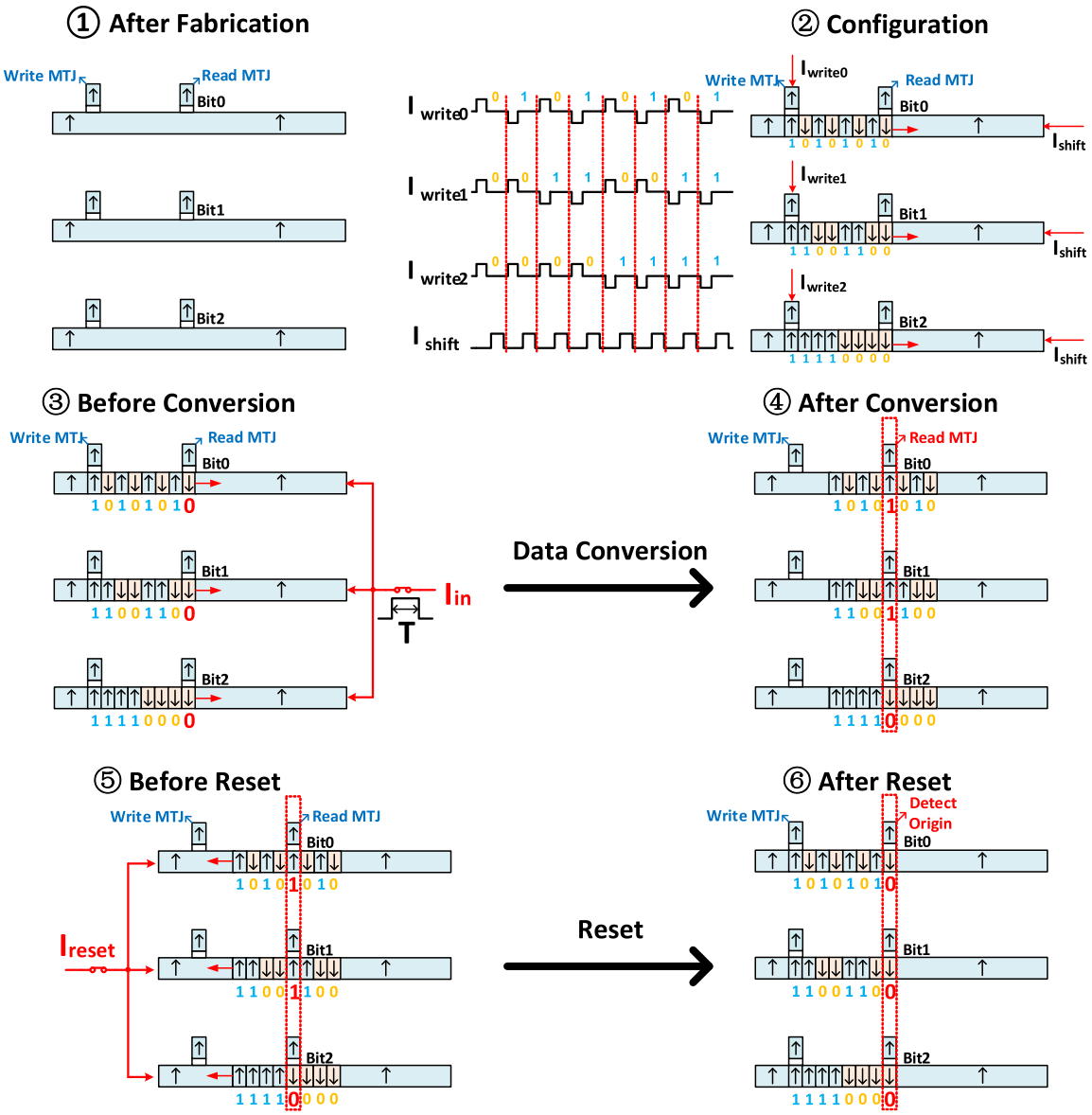

Fig. 3. 3-bit racetrack converter consists of three magnetic nanowires. After fabrication, each nanowire is configured with different DW granularity and represents an individual bit by current injection. During data conversion, current under test will flow through the nanowire, and all DWs will move together. The moving distance is lineally proportionally to the current under test. After conversion, the converter needs to be reset for the next cycle.

DW velocity can be described as

$$v = \frac{\beta \mu P}{\alpha e M_s}(J - J_{\text{th}}) \tag{1}$$

where β is the nonadiabatic coefficient, μ is the Bohr magneton, P is spin polarization percentage of the tunnel current, α is the damping constant, e is the elementary charge, M_s is the demagnetization field, J is current density, and J_{th} is threshold current density. Velocity v can be increased with a higher current density [Fig. 2(b)]. In a certain current range, the relationship between v and J would be quite linear [6], [7], [13]. Given this linear characteristic, current-induced DW motion is suitable for analog computation and data conversion in particular.

III. Proposed Racetrack Converter

A. Overview of Racetrack Converter Operation

1) Configuration: Fig. 3 shows the structure of the proposed racetrack converter with 3 bits as an example. An n-bit converter requires n nanowires (Fig. 4). Each nanowire will have 2^n DWs, one read MTJ, and one write MTJ. Each nanowire will be configured differently such that each generates a single bit, from LSB to MSB. Then, the polarization of the magnetic domain beneath n read MTJs represents the digitalized value from 0 to $2^n - 1$. This configuration is done only once postfabrication, using the write MTJ port. When applying a positive current pulse on the write MTJ, the magnetic domain beneath that MTJ becomes spin-polarized with downward direction representing data 0 and a negative current pulse

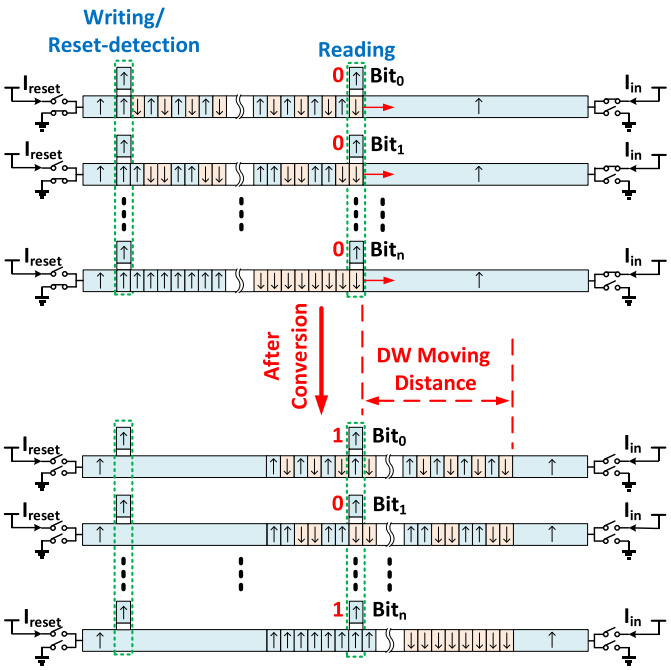

Fig. 4. Data conversion scheme for an n-bit racetrack converter.

generates upward spin-polarized magnetic domain (data 1). With a sequence of alternating write and shift current pulses, corresponding data can be stored on nanowires one by one. Altogether, such a design can store $256*8$ bits on 8 magnetic nanowires to form an 8-bit racetrack data converter. According to [8] and [20], DW write pulse is about 10 ns using 1.2×10^8 A/cm^2 vertical current. Therefore, the write energy is less than 1 pJ/bit [21]. As we only write once, the write power and latency are not important in this application.

2) Data Conversion: As shown in Fig. 3, the input current under measurement flows through the nanowire in the opposite direction of the reset current. In this case, all the DWs move right simultaneously. As the current under measurement for each nanowire has the same value, the DWs in different nanowires move at the same velocity. After a fixed time T, the DWs will stop. The distance X that DWs move can be expressed as

$$X = v * T = \frac{\beta \mu P}{\alpha e M_s} \left(\frac{I}{\text{Area}} - J_{\text{th}} \right) * T. \tag{2}$$

The distance X is linearly proportional to the current I or the time T, which makes racetrack nanowires promising for both current-digital and time-digital converters.

3) Read: The polarization of the magnetic domain beneath the read MTJs stores the digitized value of the distance a DW has moved (ranging from 0 to $2^n - 1$). As the read MTJ head is upward spin-polarized, MTJ resistance with a downward spin-polarized nanowire domain could be 2–3× higher than that with the upward polarized nanowire domain. Therefore, by sensing the resistance of the read MTJ head above a given nanowire, a 0 or 1 state can be defined. Using sense amplifiers, the data can be read out as a digital value. In a more simplified design, write, reset, and read can be performed with a single

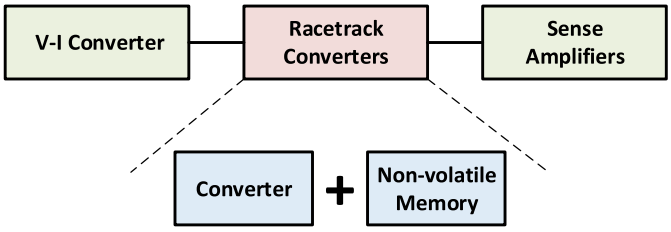

Fig. 5. Racetrack converters function similar to a combination of data converter and nonvolatile memory. Interface circuits to CMOS must provide current to the converter and sense the current at its output.

universal MTJ in the position of the read MTJ in Fig. 3. The writing pulse in that case is applied to the single MTJ to configure the nanowires. With the input shift current flowing in the opposite direction, the data are leftshifted one by one, rather than right. Reset detection is then performed by sensing all the 0 s as the beginning point using the universal MTJ.

4) Reset: After conversion, the write MTJ will subsequently perform reset point detection. Horizontal reset current flows through the nanowire to cause DW motion. When all the DWs move back to their original position, write MTJ resistances undergo their resistance transitions, which is detected by sense amplifiers. Once the resistance change is sensed, the shift current is cut off, signifying the completion of the reset phase. Sensing current is much smaller than writing current and threshold current for DW motion, and therefore does not induce any change in the nanowire. If the latency of the sense amplifier is too long, over-reset or under-reset might happen. To address this problem, two-step reset should be used: 1) employing high current to quickly shift all DWs back with sense amplifiers coarsely detecting all 0s and 2) using small current to move each nanowire slowly with each sense amplifier finely verifying the reset point. After the first step, most of the nanowires will be reset to the original position, but some might have one-bit ahead or behind. As each nanowire has its own sense amplifier and fine reset control, the second step can carefully move each nanowire back to origin separately. The whole verification process can take less than 10 ns, which is only 20% of the whole cycle time (50 ns). Both global coarse reset control and local fine reset control are simple logic gates (Fig. 9.)

B. Racetrack ADC

Most spintronic devices are suitable for current-mode computation because their characteristics have a direct mathematical relationship with current. The operation of mLogic [12], all-spin-logic [22], and DW neuron [3], [13], [14] are all based on current. Our proposed racetrack converter is fully compatible with these current-mode spintronic logic devices. By combining with these other approaches, more complex current-steering mixed-signal systems can be implemented. However, most CMOS modules remain voltage based. To realize integration, interfaces between CMOS and racetrack converter are needed. As shown in Fig. 5, the racetrack converter includes the functionality of both a data converter and nonvolatile memory. The interface circuits with CMOS

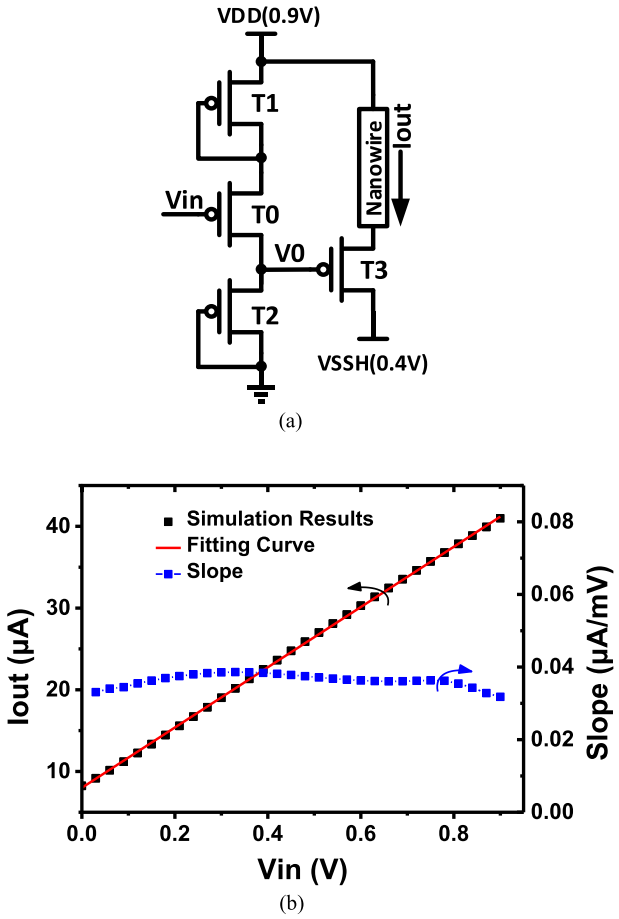

Fig. 6. (a) Schematic of 4T all-pMOS V–I converter and (b) simulation results of its Iout-Vin characteristics.

need to provide current at the input of the converter and sense current at its output. Thus, the interface circuits mainly include sense amplifiers and a voltage-current (V–I) converter for the ADC.

For the ADC, the front-end interface should provide a current linearly dependent on the input voltage. Fig. 6(a) shows a 4T all-pMOS V–I converter with the racetrack nanowire as the load. T0, T1, and T2 in the first stage make up an attenuator (amplifier with gain less than 1). The output voltage of attenuator V0 will linearly follow the change in the input voltage Vin with opposite phase. The range of V0 is smaller than Vin, forcing T3 to operate in the velocity saturation region. As the electrical characteristics of a racetrack nanowire mimic a resistor, the current through the nanowire also changes linearly with input voltage. Moreover, the lower limit of current range is not 0 as T3 operates in the velocity saturation region across the full input voltage range. We can design this lowest current to compensate the threshold current of DW motion [23]. Fig. 6(b) shows the simulation results of the V–I converter's Iout-Vin characteristics. The transconductance of this 4T V–I converter is quite linear, with an adjusted R-square value of 0.99996. Furthermore, this V–I converter is built using all pMOS, which increases its tolerance to process corners. In addition, as a source follower the current is insensitive to the ground voltage of T3. Therefore, VSSH can be raised to achieve lower power.

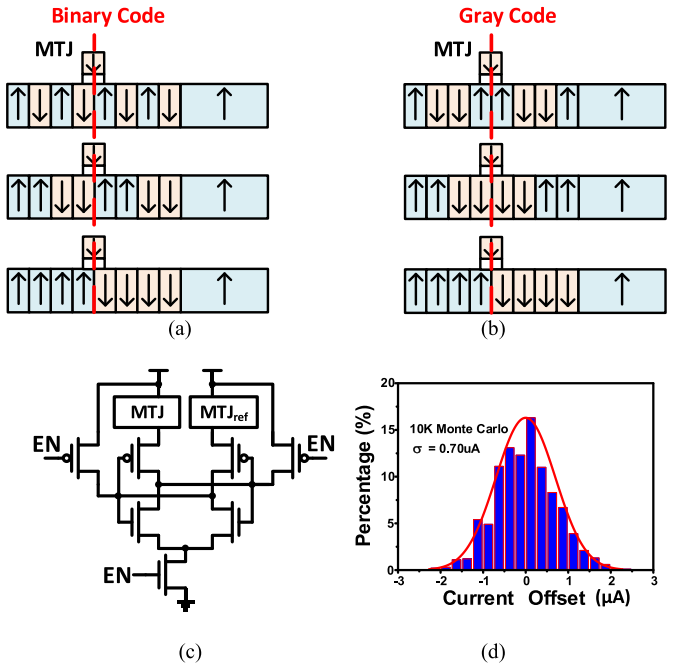

Fig. 7. (a) Midpoint meta-stability problem. (b) Solution with Gray Coding. (c) Schematic of current sense amplifier. (d) Sense amplifier current offset simulaion results.

The racetrack nanowire itself is a type of nonvolatile memory. After conversion, data can be stored immediately in the nonvolatile racetrack memory without area and timing overhead. With traditional CMOS current sense amplifiers [Fig. 7(c)], stored data can be accessed. There is one situation to carefully consider. As shown in Fig. 7(a), when a DW moves to the midpoint beneath the read MTJ, the resistance difference between the read MTJ and reference MTJ (with average resistance value) becomes very small. This may cause meta-stability in the sense amplifier and induce errors. Further, if most bits are approaching their flipping point, the error becomes significant. To avoid multibit flipping, we proposed to use gray code instead of binary code to ensure only one bit changes at a time. Fig. 7(d) shows the current offset distribution of the CMOS current sense amplifier with 10 K Monte Carlo simulation. The standard deviation of the current sense amplifier offset is 0.7 μA, much smaller than the sensing current range (from 20 to 50 μA).

Moreover, we exploit the self-reference sensing scheme to narrow the meta-stability region. As shown in Fig. 8(a), an additional (reference) MTJ is placed next to the read MTJ. This additional MTJ serves as a reference with the opposite phase to the read MTJ. Use the LSB gray code nanowire as an example. If the reference MTJ is placed 2 units distance away from the read MTJ on the top of the same nanowire, the DW polarity beneath the reference MTJ will always be complementary to that of the read MTJ. In the LSB gray code nanowire, bit 2 keeps commentary to bit $0(2-2)$ or bit $4(2+2)$. If the read MTJ resistance is high, that of the reference MTJ is low. When the resistance of the read MTJ approaches its middle value, the resistance of the reference MTJ similarly approaches its middle value from the opposite direction. As illustrated in

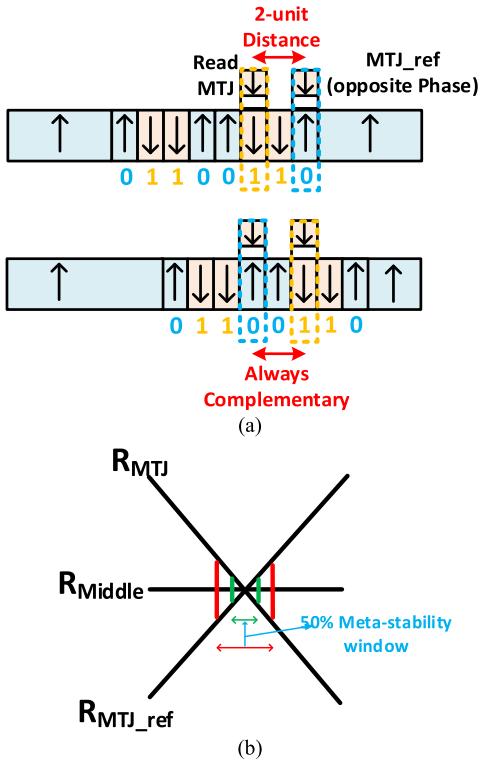

Fig. 8. (a) Self-reference sensing using the LSB gray code nanowire as an example. If the reference MTJ is placed 2 units distance away from the read MTJ, the DW polarity beneath the reference MTJ will always be complementary to that of the read MTJ. (b) Sensing dead zone can be narrowed by 2× using self-reference sensing.

Fig. 8(b), this technique shortens the meta-stability window of the sense amplifier by 50%. For other bits in 3-bit gray code, a 4-unit distance will keep results always complementary. Neither Gray coding nor self-sensing induces area or delay overheads.

Fig. 9 shows the block diagram of an 8-bit racetrack ADC including shared V–I converter, eight rancetrack nanowires, and eight sense amplifiers. Write, shift, and reset switches are also shown in the figure. To minimize the mismatch among these nanowires, an offset compensation circuit is included in each nanowire. The main idea of the method is to add a tunable resistor connected in series with each naowire. The simplest implementation of this tunable resistor is ratioed linear-region transistors connected in parallel. The number of connected on-state transistors can be tuned digitally according to the threshold current mismacth of the nanwire. Calibration is required to determine the value of the tuning bits.

IV. Uncertainty Analysis and Discussion

A. Process Variation

Both CMOS process variation and racetrack nanowire variation will influence data conversion accuracy. For the CMOS part of the design, the 4T V–I converter is tolerant to systematic variation due to its all-pMOS implementation. In particular, systematic variation creates only a minor offset to the V–I conversion curve with little impact on slope and linearity. The offset can be canceled using a simple N-well bias compensation method. However, the V–I converter remains sensitive to random variations induced by random dopant fluctuation and line edge roughness (LER). We upsize the pMOS transistors to alleviate the influence of these random variations. In addition, random variation also leads to sense amplifier offset. Device sizing and/or autozero calibration techniques [24] can be employed to enhance mismatch tolerance.

For the racetrack nanowire itself, the major sources of variation include: 1) MTJ layer area; 2) tunneling oxide thickness; and 3) cross-sectional area of the nanowire. Both 1) and 2) affect MTJ resistance [25] and may lead to read failure. The proposed self-reference sensing alleviates this influence. MTJ area can also impact the dynamic spin-polarization characteristic during configuration; this can be ameliorated by extending the write time and performing verification after configuration to ensure successful spin-polarization of each domain. The nanowire cross-sectional area can affect the threshold current density for DWs to move and shift the $(v - J)$th curve of DWs. LER-induced cross-sectional area random variation is potentially the most severe variation for the proposed racetrack converter. Fortunately, similar to threshold voltage mismatch in CMOS devices, the threshold current mismatch arising from cross-sectional area random variation can be alleviated by variation-aware circuit design techniques (current offset compensation methods) or postsilicon calibration techniques. We proposed one mismatch compensation method as shown in Fig. 9.

This paper focuses on the basic structure of a racetrack nanowire-based converter architecture, however, advanced design techniques commonly used in CMOS converters, such as time-interleaving [26], can also be applied to improve its conversion accuracy or performance. Moreover, thanks to the extremely small area, an additional bit can be included to compensate for potential accuracy losses arising from variation with only 12.5% area and power overhead for 8-bit ADC, as an example. While adding one additional bit in CMOS ADC may even take about 100% area consumption, because the CMOS ADC area is in a quadratic relationship to the number of bits. However, the racetrack ADC only requires one extra nanowire and one extra sense amplifier to add one bit. If the target is 8 bits ADC function, a 9-bit racetrack ADC can be used to realize the 8-bit function with only 13% extra area overhead and the accuracy can be improved compared to using only 8-bit ADC.

B. Noise

The proposed racetrack converter works in current mode during data conversion. Compared with a conventional voltage mode CMOS converter, current mode computation suffers less from noise [27]. Moreover, during conversion a constant current flows through the nanowires without any switching. Therefore, the proposed racetrack converter is immune to switching-related noise, making thermal noise the dominant noise source during data conversion. Both the V–I converter and racetrack nanowires will contribute to thermal noise. Spintronic devices generate much less thermal noise than MOS transistors because of their smaller resistance [28]. Based on previous analysis, the total integrated thermal noise current of

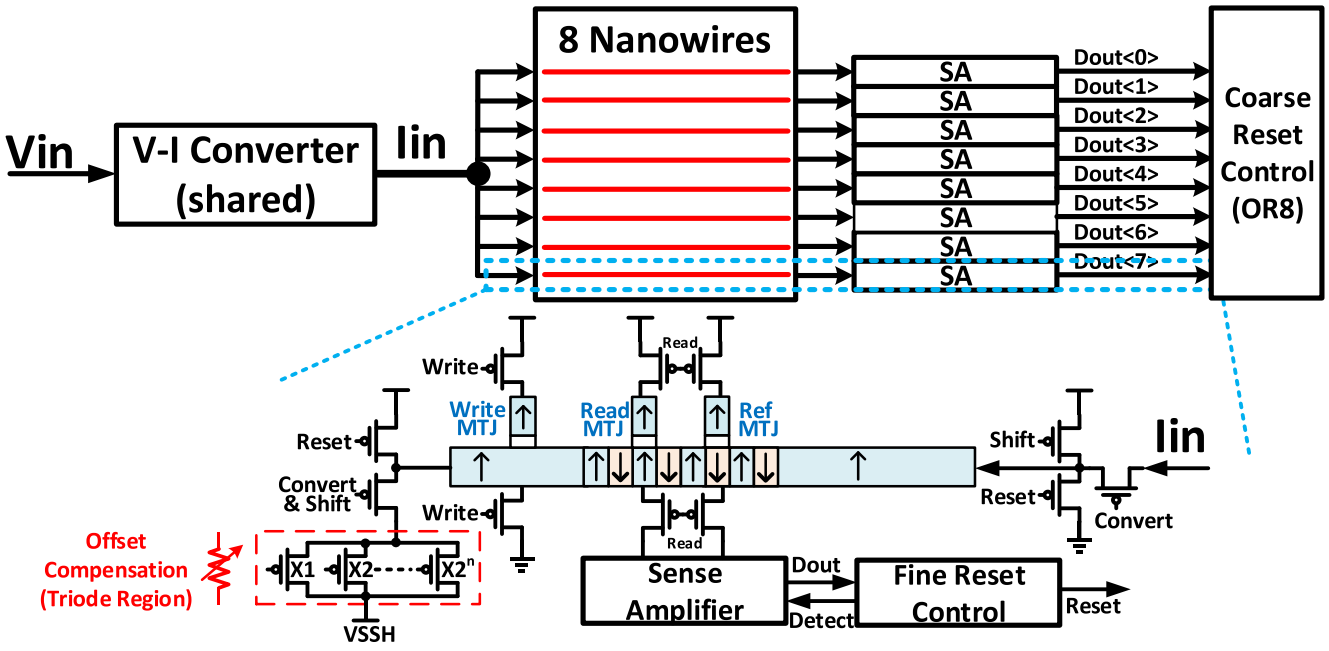

Fig. 9. Eight-bit ADC block diagram and offset compensation method.

the converter could potentially be three orders of magnitude smaller than the input current. The simulated noise standard deviation (both thermal and flicker) of both V–I converter and nanowire is ~0.42 mV.

C. Stability and Reliability

Using PMA magnetic material, the current-driven motion in a DW is not sensitive to pinning and local magnetic fields or temperature [6], [8]. 10-year retention at 150 °C can be achieved and endurances above 10^{10} cycles have been reported with 10^9A/cm^2 write current density in 90 nm technology, which demonstrates the great reliability [7], [19], [29], [30]. Thanks to the low resistance of the nanowire (~10 kΩ for 3.5 nm × 30 nm × 16 μm [12]), the joule heating power is less than 10 uW, comparable to CMOS.

This combination of high endurance and excellent retention indicates that the technology is a good match for high sampling rate nonvolatile data conversion. Moreover, as converted data will be sent to a processing module immediately after conversion, there are no concerns with thermal stability-related retention.

V. Simulation Results and Analysis

We build compact Verilog-A models of MTJ and racetrack nanowire based on published experimental data [6], [7], [9], [10]. The dimensions of each nanowire are designed to be 3.5 nm × 30 nm × 16 μm, compatible with a 32 nm technology. Co-simulation with CMOS circuits (a commercial 32 nm SOI technology) is performed by SPICE simulator. Fig. 10 shows the layout design of the 8-bit ADC. The CMOS circuits and nanowires are stacked and their areas are matched.

Fig. 11 shows data conversion simulation results of an 8 bit racetrack ADC. The ADC input voltage range is [0], [0.9V]

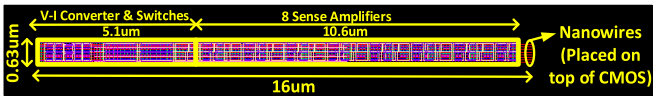

Fig. 10. Layout of the 8-bit ADC with 10 μm^2 total area.

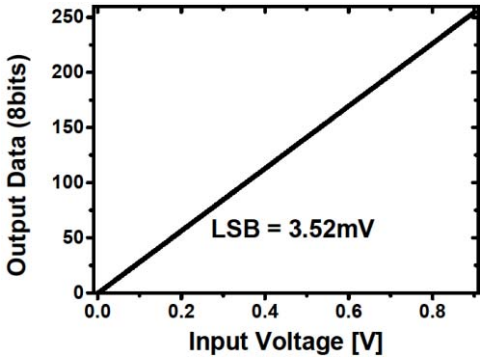

Fig. 11. Simulated data conversion of the ADC.

with 3.52 mV LSB. The ADC has a variable input voltage with fixed sampling time for DWs to move.

The V–I converter changes the ADC input voltage to a current for data conversion. The current range is 7–40 μA (6.7-38 MA/cm^2) for this 32 nm technology. The V–I converter can tune the output current range to guarantee the DW velocity increase linearly with higher current density. In state-of-the-art experimental results, the needed current density to move the DW by 250 nm within 2 ns is 18 MA/cm^2 at 90 nm technology [7], [29]. Moreover, [7] experimentally shows a quite linear relationship of DW velocity upon current density range from 18 to 50 MA/cm^2.

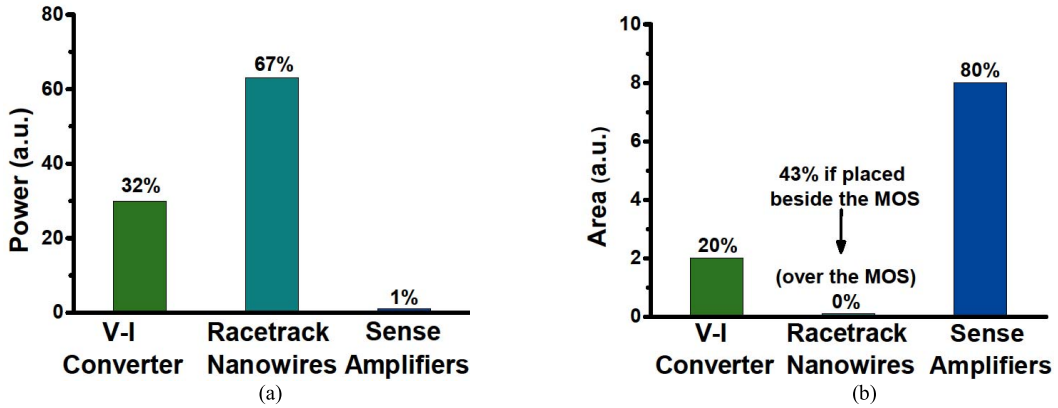

Fig. 12. (a) Power and area. (b) Breakdown of each ADC component. Racetrack nanowires consume the most power, though area overhead can be ameliorated by placement above MOSFETs.

TABLE I
COMPARISON WITH RECENT 8-bit LOW-POWER CMOS ADCS WITH COMPARABLE SAMPLING RATES

	CMOS ADC [36]	CMOS ADC [37]	Racetrack ADC
Technology (nm)	90	40	32
Sample Rate (MHz)	10	20	20
Resolution (b)	8	8	8
Power (μW)	26.3	84.9	96.5
FOM (fJ/conv.)	12	19.2	21
SNDR (dB)	48.50	44.90	46.21
ENOB	7.70	7.17	7.38
Area (mm^2)	**0.021**	**0.0153**	**0.00001**

As the threshold current density will decrease with reduced cross-sectional area [17]–[19], less than 6.7 MA/cm^2 threshold current density for 32 nm technology is achievable as mentioned in [3] and [12]–[14]. Also, good linearity of current density range from 6.7 to 38 MA/cm^2 in 32 nm technology should be achievable. The minimum DW velocity at 6.7 MA/cm^2 will be 1m/s, with which one bit code (30 nm) can be shifted within 20 MHz cycle time.

Fig. 12 shows the power and area breakdown of each component. Among the three parts, the racetrack nanowires dominate power consumption, taking more than half of the total power. The nanowires operate continuously during conversion and possess resistor-alike electrical characteristics.

Sense amplifiers only operate for a short time (less than 1 ns) after conversion and remain in a low-power standby mode during conversion. Compared with sense amplifiers, the V–I converter consumes more power yet less area. By raising VSSH, V–I converter power can be lowered. As racetrack nanowires can be placed on the top of the MOS, they do not induce extra area overhead if carefully designed.

Table I shows the characteristics of a racetrack ADC in 32 nm technology. At 20 MHz, the total power is 96 μW. Furthermore, the area is only 10 μm^2, which is three orders of magnitude smaller than the state-of-the-art CMOS ultralow-power SAR ADCs with comparable FOMs (∼20 fJ/conversion-step). Racetrack ADC power consumption is input dependent. As shown in Fig. 13(a), higher input voltages generate higher currents through the nanowires and V–I converters, consuming higher power. The average power also increases with a higher sample rate of the ADC [Fig. 13(b)]. However, because of the uncertain DW velocity linearity at ultrahigh currents, we consider a modest operating frequency of 20 MHz to ensure reliability. With a wider linear region of DW velocity, higher sampling rates can be achieved.

Another advantage of the proposed racetrack ADC is that the total area and power increase linearly with resolution rather than exponentially [Fig. 13(c)]. Adding one bit requires only one additional magnetic nanowire and one sense amplifier. Racetrack ADCs also benefit from the significant scalability of spintronic devices. With technology scaling [31], [32], the total nanowire length can be shortened, which will lower the required velocity to achieve the same sample rate. The cross-sectional area will be minimized, lowering the threshold current density of DW. As DW motion is based on the current density, a smaller cross-sectional area also translates to smaller current needed to achieve the same velocity. Therefore, to realize a constant sampling rate, the average power reduces cubically with scaling Fig. 13(d).

There are four major factors affecting the ADC nonlinearity: 1) nonlinearity of the DW velocity upon current density; 2) mismatch of the nanowire; 3) sense amplifier offset; and 4) nonlinearity of the V–I converter.

For 1), the nonlinearity of the DW velocity upon current density can deteriorate the DNL. However, it is hard to estimate the accurate nonlinearity with insufficient and sparse published experimental data. With a compact model, it is ideally linear. For 2), nanowire mismatch will also shift the DNL. According to [33] and [34], the standard deviation of DW mismatch can be approximately 5%. Fortunately, with the proposed mismatch-compensation method (Fig. 9) the nanowire mismatch can be minimized to less than 2%, affecting DNL with a 2% variance. For 3), the sense amplifier offset will shift each code randomly. Using Monte Carlo simulation, the standard deviation of the current offset is 0.7 uA. With 0.1 V across the read MTJ and the reference MTJ, the current

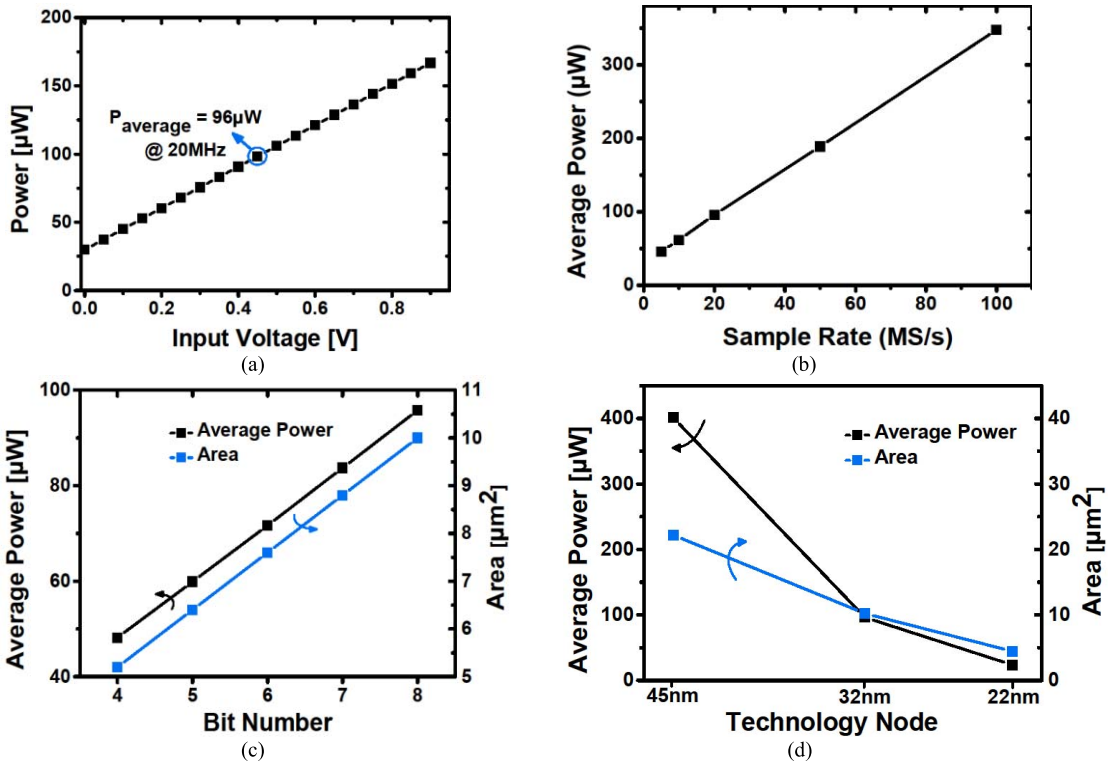

Fig. 13. (a) Relationship between power and input voltage. (b) Average power increases with higher sample rate. (c) Total area and power increase linearly with more bits. (d) Average power reduces cubically with technology scaling.

under sensing ranges from 20 to 50 uA. Thanks to our self-reference technique, the effective sigma offset is 0.35 uA, which can shift DNL by 1.2% LSB. For 4), according to the simulated results, the nonlinearity of the V–I converter will contribute a 5nA shift in average, which is about 4% LSB. In total, the standard deviation of the DNL shift is 7.2% LSB.

We also did noise simulation of both V–I converter and nanowires (as resistors). The standard deviation of the noise (both thermal and flicker) is 0.42 mV which is 12% LSB. By using the method in [35], the SNDR is 46.21 with 12% LSB noise and 7.2% DNL shift. The ENOB is 7.38.

VI. High-Speed Image Sensor With Racetrack ADCs

High speed imaging systems employing in-pixel ADC, also known as DPS have several advantages over widely used conventional APS architecture with columnwise ADC, including much higher speed, better scalability, and less noise (read-related column fixed-pattern noise and column readout noise). In particular, frame rate can be improved by more than 10× over APS with column-based ADC. With in-pixel ADC, only digital data is read out, which is faster and consumes lower power than reading analog values followed by conversion. However, the major bottleneck limiting the application of CMOS DPS is the large pixel size and low fill factor due to the area overhead of ADC and memory. Reference [1] reported a high-speed DPS with per-pixel single-slope moderate-accuracy ADC and 8-bit 3T DRAM. The dynamic range and frame rate are greatly enhanced with DPS architecture yet area and fill factor are unreasonably high [4], [5].

The proposed racetrack ADC is a combination of ADC and nonvolatile memory with extremely compact area, making it well suited to the DPS image architecture that commonly relies on a CMOS moderate-accuracy ADC and separate memory. Fig. 14 shows the DPS block diagram with the proposed racetrack ADC in each pixel. Unlike a CMOS single-slope ADC that requires analog ramp voltage from peripheral DAC and write-in data for memory, a racetrack ADC only requires CLK from a peripheral block during conversion, simplifying the required peripheral circuits and alleviating noise and I-R drop (Fig. 15). The system structure is similar to a typical nonvolatile memory bank. Sense amplifiers are placed at the bottom of the array (Fig. 14) and shared by the array. Therefore, their area are not included in the pixel cell. Both read and configuration operations are performed row by row like a nonvolatile memory. During read, when one row get accessed, the read MTJs will be connected to the shared sense amplifiers to read out the data. After one row read-out, the address will change and activate the other row alternately. After read of the whole array, all racetrack nanowires need to be reset for the next conversion. Configuration is also performed row by row. When one row gets activated, BLs will be connected to each write MTJs header through pMOS switches. Write current flow through BLs to the write MTJ and flip the polarity beneath it, and then shift current flow through the WL with pMOS switches. Conversion will be done inside each pixel all at the same time.

Both the V–I converter and access transistors can be implemented with only pMOS devices, further minimizing the required area as large N-P well spacing is not needed.

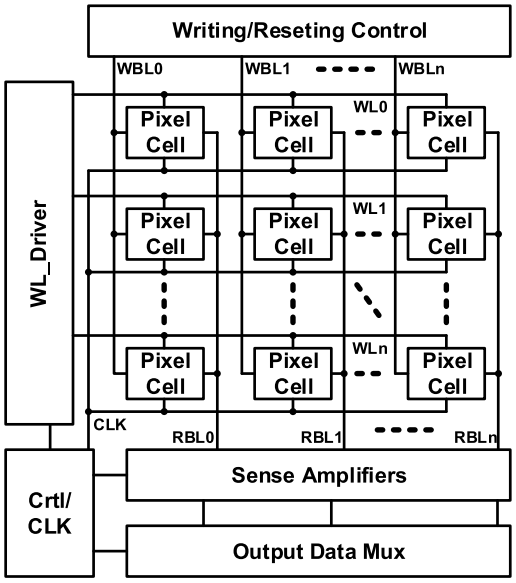

Fig. 14. DPS block diagram implemented with racetrack ADC.

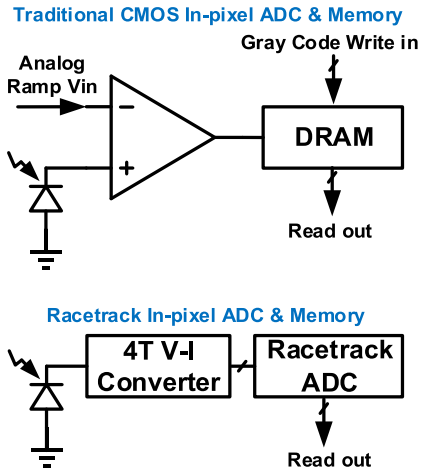

Fig. 15. Digital pixel cell comparison. Unlike CMOS single-slope ADCs, the racetrack ADC does not require analog ramp voltage and write-in data. Readout can be done with shared sense amplifiers like memory readout.

Moreover, the racetrack nanowires can be placed on the top of pMOS transistors. In this way, the nanowires will not induce extra area overhead. Fig. 16 illustrates the layout implementation of 2×3 pixels. The nanowire is somewhat long but very narrow, hence 1×3 pixels can be arranged together to match nanowire length with 3×8 nanowires placed above the access pMOS. In this arrangement, area is still dictated by transistors rather than the nanowires. Thus, the fill factor is significantly improved over CMOS alone.

Table II compares CMOS APS and DPS image sensors with a racetrack DPS image sensor. Sensor fill factor matches CMOS APS and is $3\times$ better than CMOS DPS. Frame rate is improved by $50\times$ with a lower power consumption. The proposed racetrack ADC is very promising for this high-speed imaging application.

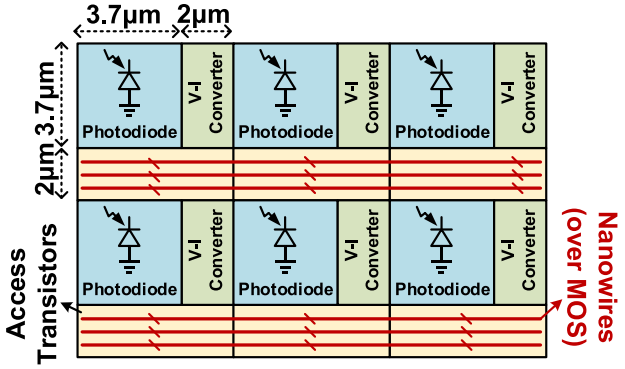

Fig. 16. Layout implementation of 2×3 pixels. Racetrack nanowires can be placed on top of the access transistors.

TABLE II
COMPARISON BETWEEN CMOS APS, CMOS DPS, AND RACETRACK DPS

	CMOS APS [4]	CMOS DPS [1]	Racetrack DPS
Sensor Fill Factor	40%	15%	42%
Frame Rate	3 500	10 000	>500 000
ADC Resolution (b)	12	8	8
ADC Conv. Time (ns)	500	25	50
Energy Per Frame (µJ)	280	5	0.04 [16]

VII. CONCLUSION

We analyze the potential of current-induced DW motion for data converter application and present an ADC design scheme based on racetrack magnetic nanowires. The 8-bit ADC can achieve 21 fJ/conversion-step, while the area is less than 10 μm^2, which is $1000\times$ smaller than state-of-the-art CMOS ADCs with similar energy efficiency. The results indicate that racetrack converters hold promise for future low-power small-area applications requiring multiple ADCs. A high-speed racetrack ADC-based DPS image sensor system is also proposed to show one potential application of this design.

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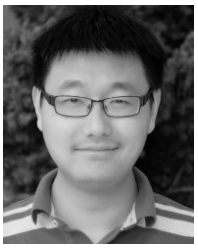

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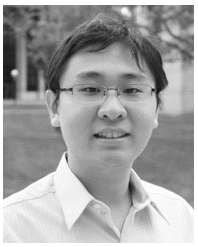

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