

Circuit and System Designs of Ultra-Low Power Sensor Nodes With Illustration in a Miniaturized GNSS Logger for Position Tracking: Part II—Data Communication, Energy Harvesting, Power Management, and Digital Circuits

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Abstract—This two-part paper reviews recent innovations in circuit design that have accelerated the miniaturization of sensor nodes. In this second part of the paper, we focus on key building blocks of miniaturized sensor nodes, such as data transceivers, energy harvesters, power management units, and digital logic circuits. System level design considerations are also discussed to provide guidelines for the design of a miniaturized system. As an example prototype design, a 2.7-cm³ global navigation satellite system (GNSS) logger is proposed. This paper includes a die-stacked sensor platform composed of an ARM cortex M0 processor, energy harvester, power management unit, solar cell, optical receiver, sensor layer, and RF transmitter that exploits the discussed design techniques for ultra-low power operation. The GNSS logger can store GNSS signals of >1 k positions on a single battery charging without additional energy harvesting.

Index Terms—Internet of things, IoT, sensor node, ultra-low power, wireless sensor node, GNSS.

I. INTRODUCTION

PART I of this paper [1] reviewed circuit techniques used in the sensor's front-end, a key element in data collection. Here, in Part II, we will review other key building blocks of a sensor node that are essential for its stand-alone operation.

Data communication is one of the key functions of wireless sensor nodes. The ability of physical objects to share and to process acquired information from the physical world has been referred as the internet of things (IoT). This trend in innovation has received considerable attention in both academia and the semiconductor industry due to its substantial potential to

elevate the quality of machine service. Sensor nodes, located at the leaf of the interactive network, play an important role as the source of information. However, small form factors and limited energy capacities pose difficult challenges in the design of data transceivers for miniaturized sensor nodes. Therefore, research on robust and energy efficient communication methods has been conducted to overcome such challenges. In section II, circuit techniques to overcome a limited antenna efficiency and energy budget are introduced.

An efficient energy chain from the energy harvester through the battery to the power management unit is another essential building block of a sensor node. Minimum harvestable power is emphasized to sustain the sensor node's operation since very small input power ranges of sub-nano-watt to micro-watt originate from its form factor. Also, the power management unit needs to efficiently operate under a wide variation of loading conditions, including sub-nano-watt levels during sleep mode, micro-watt levels in wake-up and milli-watt levels during data communication. Circuit techniques for energy harvesters and power management units are discussed in sections III and IV. Further, circuit techniques for reducing the power consumption of digital logic gates are introduced in section V.

Finally, a proto-type design of a miniaturized global navigation satellite system (GNSS) is proposed in section VI. An energy harvester, a power management unit and RF and optical transceivers are implemented to support energy-efficient, stand-alone operation. A sensor interface layer is also implemented to monitor environmental variables such as temperature and pressure.

II. DATA COMMUNICATION

Many wireless sensor node applications require that the size be less than a cubic cm, sometimes nearing a cubic mm. Therefore, there is a basic challenge of degraded antenna radiation efficiency for RF communication due to the small form factor [2]–[8]. Furthermore, an active radio system

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requires a battery, power management unit, accurate timing reference and processing unit, which are usually too bulky to be integrated into a miniaturized sensor node. Small passive RF tags (12 mm^3) [9] can be an alternative solution to the relatively large active radios. However, the functions of passive RFID tags are limited due to the lack of an integrated power source [10]. Therefore, circuit techniques as well as integration methodologies that will facilitate the miniaturization of the necessary circuit building blocks are critical.

In contrast, optical communication using a light-emitting diode (LED) as the transmitter and a photovoltaic (PV) cell as the receiver can be implemented with high efficiency using very little space, making this approach suitable for line-of-sight (LoS) communication. For instance, LEDs smaller than 0.08 mm^2 are commercially available, and photovoltaic cells can be as small as 0.07 mm^2 [11].

A. RF Communication

Conventional RF transmitters include a local oscillator (LO) and a power amplifier (PA). An LO is usually implemented using an accurate frequency reference (crystal oscillator) and a phase-locked loop. Although an accurate LO enables advanced communication protocols, certain characteristics make it unsuitable for use in an ultra-low power sensor node. First, the crystal requires a start-up time on the order of milliseconds [12]. This long start-up time wastes a substantial amount of energy because the system is in active mode during this time. The lock time of phase-locked loop (PLL) also contributes to the loading time and therefore also to the energy waste. Second, the base power consumption of such architecture is high due to the limited Q-factor of the monolithic inductor and the complex building blocks. Therefore, there is a need for simpler transmitter architecture.

Electrically small antennas, whose largest dimension is smaller than $\lambda/10$, are commonly adopted in miniaturized sensor nodes. These miniaturized sensor nodes, therefore, suffer from high Q-factor and low radiation efficiency of their antennas. In addition, the selection of a low carrier frequency to reduce power consumption and channel attenuation (e.g. tissue absorption) further exacerbates this problem. To overcome these challenges and reduce power consumption, an architecture that eliminates PA and LO generator is shown in [13]. It introduces a minimum-shift keying (MSK) transmitter consuming $350 \mu\text{W}$ using a power oscillator as shown in Fig. 1. The proposed architecture employs a loop antenna on a printed circuit board (PCB) as a resonating component together with an on-chip capacitor array. Instead of introducing PA to drive the PCB antenna, it directly resonates the antenna with a negative-gm circuit as part of the power oscillator.

Several advantages are gained through this method. If a conventional PA drives the antenna, the small frequency difference between the carrier frequency and the antenna resonant frequency causes a reduction in the efficiency of the PA due to the high Q-factor. In contrast, if the antenna is directly resonated in the power oscillator, the carrier frequency naturally equals the antenna resonant frequency, so this problem

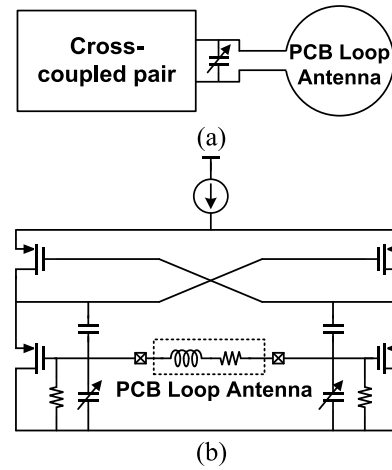


Fig. 1. (a) Conceptual diagram and (b) Schematic of a power oscillator [11].

is avoided entirely. Furthermore, the absence of LO and PA further relaxes power consumption and space requirements. Yet, this architecture introduces the problem of having inaccurate carrier frequency. But when there is asymmetry in the power and space budget between the sensor node and the base station, the frequency inaccuracy of the transmitter can be compensated in the base station. The power oscillator-based wireless transmitter for sensor node applications is adopted in [14]–[16], manifesting its benefit.

A complete system including a 2.4-GHz radio transmitter for a medical implant application is proposed in [14] and [17]. This work's goal is to operate the transmitter with less than 1 nW energy harvested from the Endocochlear Potential (EP), which is an electrochemical gradient in the inner ear. This energy limitation restricts the system's average power consumption to 250 pW . To meet such an extreme energy constraint with a small antenna whose radiation efficiency is as low as 0.8% , the system is deeply duty-cycled (0.00002%) and employs an energy harvester with ultra-low quiescent power consumption (544 pW). By assuming that a base station, such as a smart phone or a smart watch, is placed nearby, the communication distance can be restricted to one meter, which helps to reduce the transmitter power. The carrier frequency is also one of the important factors that determine the transmitter power. Due to the small antenna size, a higher carrier frequency is preferred to maximize the radiation efficiency. However, a higher carrier frequency causes larger tissue absorption of the RF signals. Reference [14] reports quantitative research on the antenna efficiency in several Industrial, Scientific, and Medical (ISM) bands and identifies 2.4 GHz as the optimal frequency to minimize the transmitter energy considering both radiation efficiency and tissue absorption.

The next area of potential improvement in the energy efficiency of an ultra-low power radio is a sensor-initiated protocol. Due to the aforementioned energy overhead as well as the size, crystal oscillators are difficult to integrate in a sensor node. The lack of an accurate timing reference in a sensor node forces the inclusion of a wake-up receiver so that the sensor node can wake up at appropriate times to enable its data radio [18]. However, such a wake-up receiver still consumes

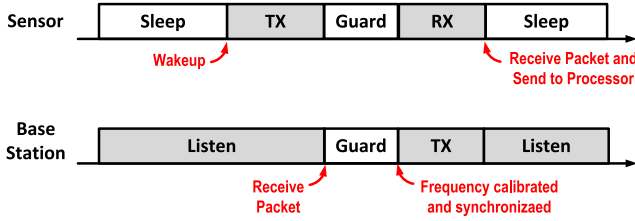


Fig. 2. A sensor-initiated synchronization protocol proposed in [10], [16], and [23].

at least tens of microwatts, limiting the number of sensor node applications that can exploit a wake-up receiver [18]–[22].

A sensor-initiated synchronization protocol to address this is proposed in [10], [16], and [23]. Fig. 2 shows a simplified timing diagram of sensor-initiated synchronization. Initially, a sensor node is in sleep mode, and the base station is in listening mode, waiting for a header from the sensor node transmission. The sensor node then transmits its acquired data using pulse position modulation (PPM). The data interval of the data packet indicates the frequency of the timer in the sensor node. Then, the base station prepares data to send during the guard time. This guard time is determined by the frequency of the timer in the sensor node so that the sensor node can initiate its receiver exactly when the base station begins the transmission, thereby removing complex base band processing traditionally needed to accommodate the frequency uncertainty of the sensor node and saving power.

B. Optical Communication

An optical receiver can be much smaller and more power-efficient than that required for RF communication when the communication distance is less than a meter, and the sensor node is located in line-of-sight [11], [24]. Optical receivers adopt a PV cell as a light receiver, which can be integrated in a CMOS die [11] or energy harvester using light [24]. Therefore, such a system can be as small as a cubic mm due to the absence of an RF antenna [25]–[29]. Another advantage of an optical receiver compared with its RF counterpart is the power consumption and the energy-per-bit. A wake-up receiver can consume less than one nW [11], [24], which makes it suitable for use in a mm-scale wireless sensor node, and the energy-per-bit is less than 100 pJ/b, which is over 20-fold less than that of RF receivers.

However, the presence of background light sources such as sunlight, incandescent light and fluorescent light may perturb the communication, resulting in an inferior bit rate. [24] proposes a dual-mode optical receiver that enables sub-nW asynchronous wake-up, a programmable data rate and background light tracking. A simplified circuit diagram of such a receiver is shown in Fig. 3. Assuming the background light is changing slowly, the background light cancellation loop subtracts the current generated by the background light, I_{NOISE} , from the total output current from the PV cell. A fast switching current is then delivered to M1 of Fig. 3 to be compared with the voltage reference. The signal voltage is amplified by the post amplifier stages, and the data are recovered after oversampling the resulting digital output. Another advantage

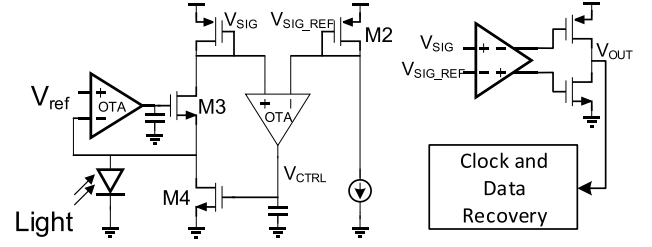


Fig. 3. Schematic of a background noise cancelling GOC receiver proposed in [24].

of this circuit is the maximum bit rate of the signal. A voltage mode optical receiver [11] has a bandwidth limitation that originates from the capacitance-to-current ratio of a PV cell, which is physically constrained. On the other hand, the circuit demonstrated in [24] adopts a current mode architecture in which the diode voltage is regulated to a voltage reference, V_{REF} . The anode of the PV cell, V_{DIODE} , is virtual ground, so the maximum speed of the receiver is determined by the input impedance of the voltage regulation loop.

III. ENERGY HARVESTING

Minimum harvestable input power ($P_{\text{in,min}}$) is a critical factor for a miniaturized sensor node to sustain its operation with a duty-cycled operation. Assuming that the system is at a steady state where the input power is equal to the used power, the duty cycle of the system can be determined as the following:

$$\eta_h P_{\text{in}} \cdot (t_{\text{active}} + t_{\text{sleep}}) = P_{\text{active}} \cdot t_{\text{active}} + P_{\text{sleep}} \cdot t_{\text{sleep}}$$

$$\text{DutyCycle} = \frac{t_{\text{active}}}{t_{\text{sleep}} + t_{\text{active}}} = \frac{\eta_h P_{\text{in}} - P_{\text{sleep}}}{P_{\text{active}} - P_{\text{sleep}}} \quad (1)$$

where η_h , P_{in} , P_{active} , P_{sleep} , t_{active} and t_{sleep} are harvester efficiency, input power, active mode power, sleep mode power, active time and sleep time, respectively. It can be seen that a sensor node may sustain its operation as long as the acquired power ($\eta_h \cdot P_{\text{in}}$) is larger than P_{sleep} .

On the other hand, the input power of a miniaturized sensor node is highly constrained due to its small form factor. In this section, we discuss circuit techniques to improve the $P_{\text{in,min}}$ and η_h when inductive coupling and photovoltaic cells are used.

A. Inductive Coupling

Conventional wireless power receivers are designed with a voltage rectifier and a DC–DC converter as described in Fig. 4. The threshold voltage of the diodes in a voltage rectifier sets the minimum voltage level that the inductive antenna needs to provide, requiring higher input power. In addition, the limited efficiency of the DC–DC converter degrades the efficiency of the harvesters [30].

A resonant current mode wireless power receiver minimizes the energy loss caused by the voltage mode rectifier and the DC–DC converter [31]. Fig. 4 shows a block diagram of the proposed work, which places a capacitor in parallel with a

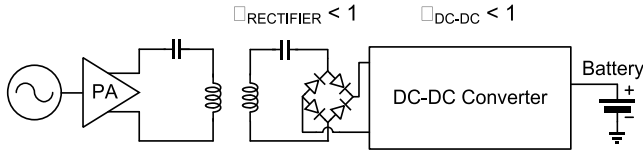


Fig. 4. Block diagram of the conventional wireless transfer circuits.

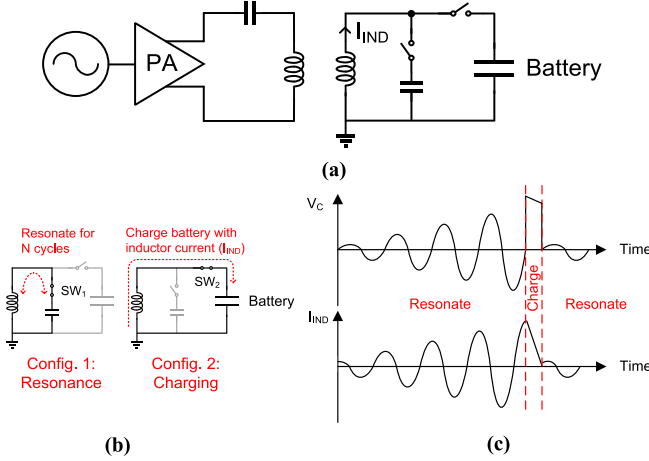


Fig. 5. A current mode resonant power receiver proposed in [31]. (a) schematic (b) switch configuration (c) voltage and current waveforms.

receiver coil, forming an LC resonator. The received energy accumulates in the parallel LC resonator for multiple cycles and is transferred to a battery in current mode. The transient signal waveform of the voltage of the LC resonator, V_C , and current in the receiver coil, I_{IND} , are plotted in Fig. 5. The switch that connects the receiver coil to the battery (SW_2) is enabled when the coil current reaches its peak, i.e. all the resonance energy is stored in the inductor as a magnetic field. After the inductor current reaches zero, SW_2 is disabled, initiating a new accumulation of energy in the resonator. This work improves $P_{in,min}$ by eliminating the energy loss caused by the voltage rectifier and the DC-DC converter. The number of accumulation cycles is tunable so that the LC resonator accumulates energy for more cycles when the input power is low, building up enough energy to overcome the energy loss during the battery charging operation, further improving $P_{in,min}$. The reported $P_{in,min}$ is $0.6 \mu W$, and its peak efficiency is 67.7% at $4.2 \mu W$ input power.

B. Photovoltaic Cell

A light harvester using a photovoltaic cell can provide a much lower $P_{in,min}$, down to sub-nW levels [32]. As shown in Fig. 6 (a), a conventional light harvester utilizes a photovoltaic cell and a DC-DC converter to charge a battery. The voltage on the diode is determined using a maximum-power-point-tracking circuit.

A direct energy transfer method with a PV cell switching matrix is proposed in [32]. Instead of level converting the voltage from a PV cell to the battery, the PV cells are configured in series so that its output voltage is directly used to charge a battery as described in Fig. 6 (b). A PV cell network configures the number of series diodes depending on the input light intensity and provides 78–95% efficiency in both dim indoor (100 lux) and direct sunlight (100 klux) conditions.

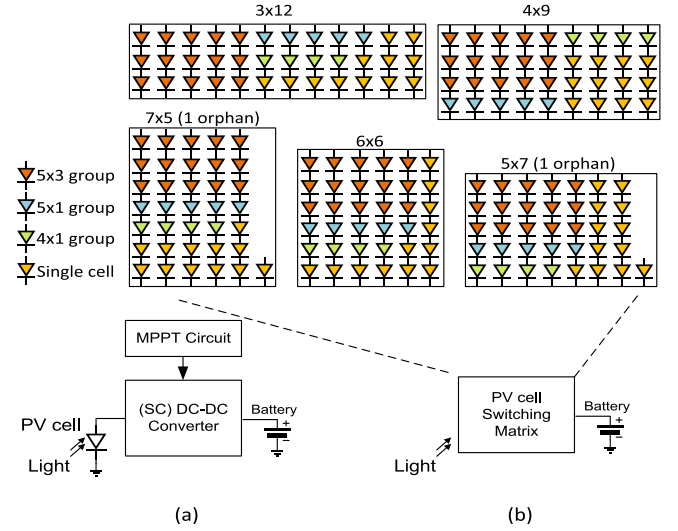


Fig. 6. (a) Conventional light energy harvester using a PV cell. (b) A reconfigurable PV-cell network proposed in [32].

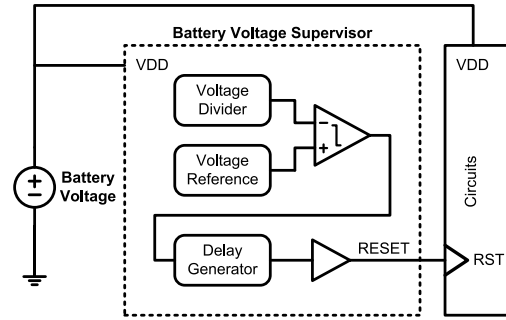


Fig. 7. Conventional battery voltage supervisor circuit structure.

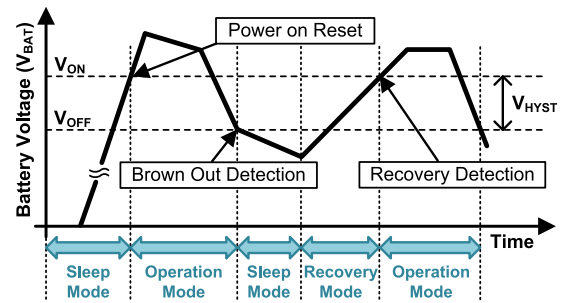


Fig. 8. Operation of a battery voltage supervisor according to the battery voltage.

C. Battery Management

Battery reliability is one of the key challenges; thus, it is important to design the charging scenario well. As the system size decreases, the battery size should also decrease. The decreased battery size increases the internal resistance (R_{BAT}) and therefore the effect of the IR drop. Moreover, R_{BAT} increases as a battery ages over charge/discharge cycles [33]–[36]. The change in R_{BAT} is problematic for sensor systems. To prevent permanent damage to the battery and the sensor system, a low-power battery voltage supervisor (BVS) is implemented [37], [38].

The battery voltage is monitored by a conventional BVS, which includes a battery voltage divider, a comparator and a delay generator, as described in Fig. 7. There are three important functions of the BVS, as shown in Fig. 8. First, Power-on Reset (PoR) generates a reset signal when the battery is initially connected. The system is enabled when the battery voltage exceeds the higher threshold voltage (V_{ON}). Second, Brown-Out Detection (BOD) detects low battery voltages that can damage the battery and the sensor system. When the battery voltage falls below the lower threshold voltage (V_{OFF}), the BVS disconnects the battery from the system. Finally, Recovery Detection reactivates the system when sufficient voltage is sensed. The difference between the threshold voltages provides hysteresis ($V_{HYST} = V_{ON} - V_{OFF}$) to avoid the system oscillating between the operation and sleep modes.

However, the constant small V_{HYST} of the BVS is not ideal for advanced miniature sensor systems. The increased IR drop in the minimized systems makes the systems unstable, oscillating between on and off. In [39], a large-constant-hysteresis BVS is proposed to handle the large and constant R_{BAT} , and the large V_{HYST} solves the oscillation problem. The proposed design can handle an R_{BAT} of up to 17 k Ω with 635 pW power consumption at 3.6 V power supply voltage. In addition, an adaptive-hysteresis BVS is described that updates V_{HYST} depending on the R_{BAT} measurement results [40]. It can endure a varying R_{BAT} up to 63 k Ω with 3.6 nW power consumption.

IV. POWER MANAGEMENT

Monolithic implementation and good efficiency are fundamental requirements for a power management unit (PMU) for miniaturized sensor nodes. In addition, there are several other factors that need to be considered.

Each building block of a wireless sensor node requires different supply voltage levels, which can minimize its energy consumption. For instance, digital logic gates best operate near the threshold voltage to minimize the dynamic power consumption, whereas static random access memory (SRAM) requires more than twice the threshold voltage to maintain a proper noise margin. Also, analog front-end circuitries such as amplifiers, ADCs and filters require various supply voltages depending on their noise specifications and signal dynamic ranges. Thus, a PMU that generates multiple output voltages is an essential element in a wireless sensor node.

The output voltage resolution of a PMU is also an important factor. A millimeter scale battery typically exhibits a very high output resistance of up to tens of kilo-ohms. Therefore, the IR drop of the battery varies widely according to the static current of the system. In addition, the battery open-circuit-voltage itself varies widely depending on the remaining energy [35]. Therefore, DC–DC converters in the PMU need to provide output voltages with accurate resolution so that the each building block of the system may receive its optimum supply voltage regardless of the battery voltage changes.

Scalability of load power is important to maintain good efficiency depending on the mode of operation. For instance

a wireless sensor node consumes nano-watts in sleep mode, micro-watts in active mode and milli-watts in radio communication mode [41], [42]. Quiescent power consumption of the DC–DC converter should adjust to the output power level, making a switched-capacitor based DC–DC converter suitable to the application since its switching loss can be easily scaled by configuring the switching frequency.

The successive-approximation (SAR) switched-capacitor DC–DC converter proposed in [43] utilizes a series of 2:1 converters to realize 2^N output levels. The charge sharing loss is reduced by offering a large number of conversion ratios. The detailed implementation of the SAR operation is explained in Fig. 9 when the configuration code is 1010₂. Each 2:1 switched converter produces its output, V_{mid} , which is defined as $(V_{high} + V_{low})/2$. When the configuration code of the n^{th} stage is 1, $V_{high,n}$ and $V_{low,n}$ are connected to $V_{high,n-1}$ and $V_{mid,n-1}$, respectively. When the configuration code of the n^{th} stage is 0, $V_{high,n}$ and $V_{low,n}$ are connected to $V_{mid,n-1}$ and $V_{low,n-1}$, respectively. As an example, the switch configurations for a 4-stage DC–DC converter with the configuration code are shown in Fig. 9 (c), and the output voltage of each 2:1 switched capacitor is plotted in Fig. 9 (d). The output voltage, V_{OUT} , is defined as $V_{BAT} \times (C+1)/2^N$ where C is the configuration code.

A schematic of the 2:1 switched capacitor is depicted in Fig. 9 (a). This work AC couples the clock to each transistor using capacitors and cross-coupled pairs to make V_{gs} of the switches identical regardless of input and output DC voltages.

Reference [44] proposes a SAR switched-capacitor DC–DC converter that improves the conduction efficiency compared with [43]. In [44], either V_{high} or V_{low} of each 2:1 switched capacitor is directly connected to the supply rails, V_{BAT} or GND, as shown in Fig. 10. By maximizing the number of connections to the supply rails, the effective output resistance of the DC–DC converter is decreased, and the conduction loss is improved. This approach has been further improved by increasing the number of conversion ratios in [45], providing more fine grained voltage control.

The output voltages of a PMU can be regulated by monitoring them and modulating the switching frequency in order to set them close to the target references [46]–[50]. The switching loss of the DC–DC converter is dynamically adjusted according to the load current in such schemes. The conduction loss is also kept constant as the ratio of $(V_{OUT,NL} - V_{OUT})/V_{OUT,NL}$ where $V_{OUT,NL}$ is the no-load output voltage. Therefore, output voltage regulation using the switching frequency can make the DC–DC converter operate near its maximum efficiency point across wide variation of load current. A feedforward control using the conversion ratio can further improve the regulation, thereby increasing the system reliability [51]. The switching frequency is usually controlled using a voltage-controlled oscillator (VCO) with a feedback loop. Due to the limited response time of such an implementation, a sudden increase of the load current can cause significant voltage droop. This is more critical for a miniaturized system since the high battery resistance further reduces the output voltage by lowering V_{BAT} . Reference [51] proposes a feedforward control of the conversion ratio so that the output voltage can be

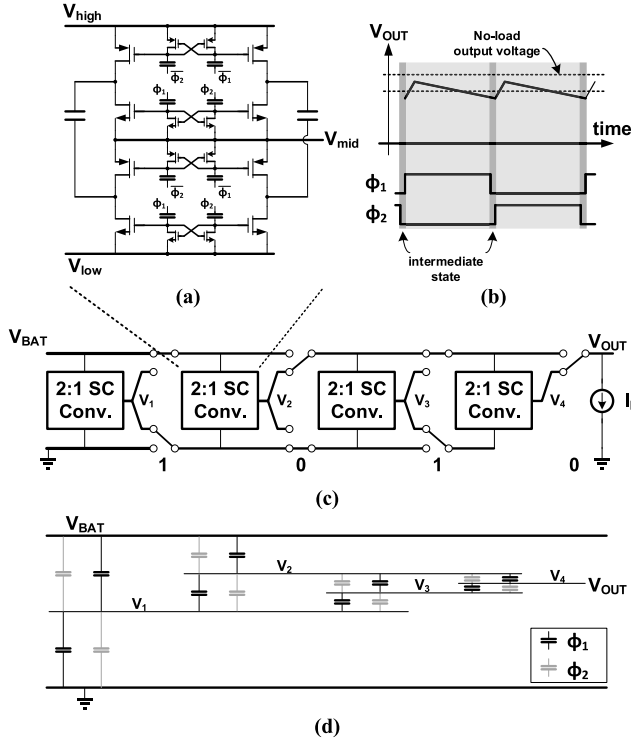


Fig. 9. A power management unit proposed in [43]. (a) 2:1 switched capacitor unit (b) time domain output voltage (c) a series structure to generate 2^N output voltage levels and (d) output voltages of the 2:1 switched capacitor cells.

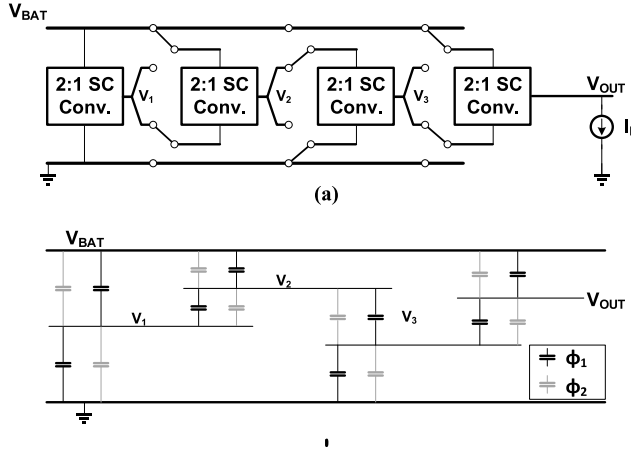


Fig. 10. (a) A reconfigurable structure proposed in [44] and (b) output voltages of the 2:1 switched capacitor cells.

instantly increased when a sudden voltage droop is detected. A system level design of a PMU for IoT sensor nodes is proposed in [45]. This work generates 0.6V, 1.2V and 3.3V with an output load current range from 20 nW to 500 μ W.

V. DIGITAL CIRCUITS

Process scaling following Moore's law has driven improvements in performance, power reduction and larger scale integration, especially targeting high-performance and strong inversion operation. Although scaling with deep submicron technologies has achieved tremendous gain for high-performance systems, it is also associated with larger leakage, larger interconnect capacitance and lagging supply scaling, which prohibits its use in miniaturized sensor nodes. Instead,

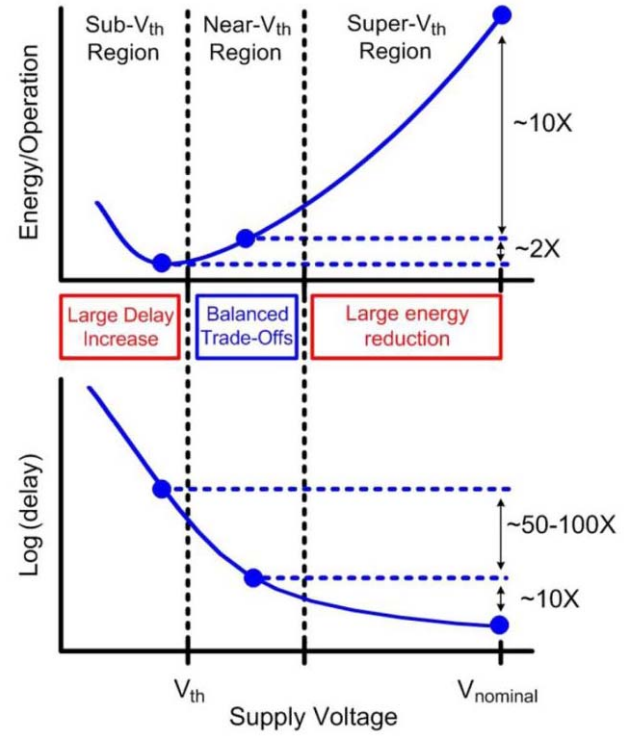


Fig. 11. Energy-per-operation and delay of logic gates depending on the supply voltage [56].

for miniaturized sensor nodes, the primary concern is low energy consumption because of the small battery capacity and limited harvestable energy. Digital circuits operating in a near- or sub-threshold region have gained great attention as a way to reduce either the power consumption or energy per operation [52]–[60]. Digital circuits operating under such low supply voltages can exhibit lower energy per operation, primarily benefited by the reduced dynamic power consumption, which is quadratically proportional to the supply voltage. At the same time, the interval of an operation during which the circuits consume their leakage current increases as a consequence of the slow evaluation time. Hence, the energy overhead from the leakage current is especially pronounced when the supply voltage is reduced below the threshold voltage of the devices due to the exponential relationship between the delay and the supply voltage. Therefore, the energy per operation is optimized when a balance is achieved between the reduction of the dynamic energy and the increase of the leakage energy, as shown in Fig. 11 [55], [57], [58], [61]. In addition, the optimal V_{DD} is affected by the idle period [59], process variation [53], body biasing [62], mismatch and activity factor [52]. In this section, recent circuit level techniques for digital circuits are discussed.

A circuit technique for the optimization of the supply and threshold voltages is proposed in [62]. In this approach, the replica path delay of multiply-accumulate (MAC) units are monitored to optimize the threshold voltage of the devices so that the leakage current is minimized given the supply voltage and the operating frequency, as shown in Fig. 12. The body voltages of PMOS (V_{BPP}) and NMOS (V_{BBN}) are stabilized using a delay-locked loop composed of a phase

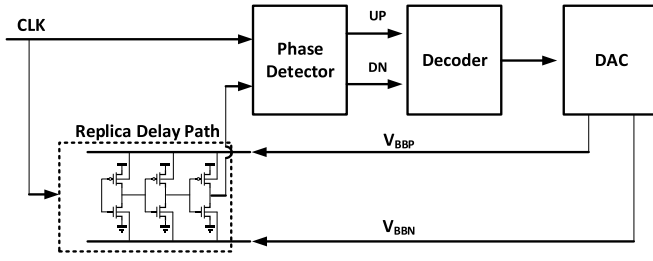


Fig. 12. Schematic of a delay-locked loop for adaptive body-biasing of logic circuits [62].

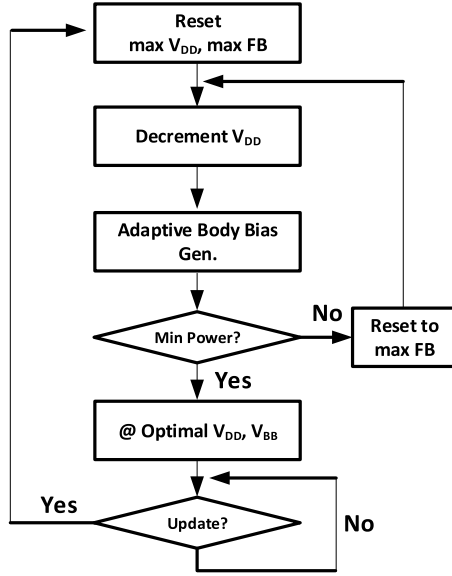


Fig. 13. A flow chart of the optimization procedure of V_{DD} and body-biasing voltage (V_{BB}) [62].

detector, a decoder, a digital-to-analog converter (DAC) and body-tuned replica delay cells. The replica path delay is equal to the reference period in the steady state. The combination of V_{DD} and body-biasing voltages are further optimized by sweeping the supply voltage to find the optimal combination for minimum power, as shown in the flow chart in Fig. 13. Initially, V_{DD} is set to maximum, and the body voltages are set to a maximum forward biasing condition. Then, V_{DD} is decreased by one step using a DC-DC converter, and the body voltages are adjusted using the delay locked loop. This procedure is repeated until a minimum power state is achieved.

In addition to minimizing the energy-per-operation, there is also a need to minimize power consumption, sacrificing energy efficiency. Most of the miniaturized sensor nodes adopt duty-cycling of the active mode in order to reduce the average power consumption to a level of harvestable power, as explained in section VI. However, this scenario is based on the assumption that the system has a reliable battery that serves as an energy buffer during sleep mode. However, such recursive charge and discharge actions degrade the battery reliability and shorten the system life time. For instance the 5,000 discharge cycles reported in [35] with a 30 min wakeup period limit the system life time to 3.5 months [63]. Therefore, a design methodology that lowers the active power consumption to a level of harvestable energy is required.

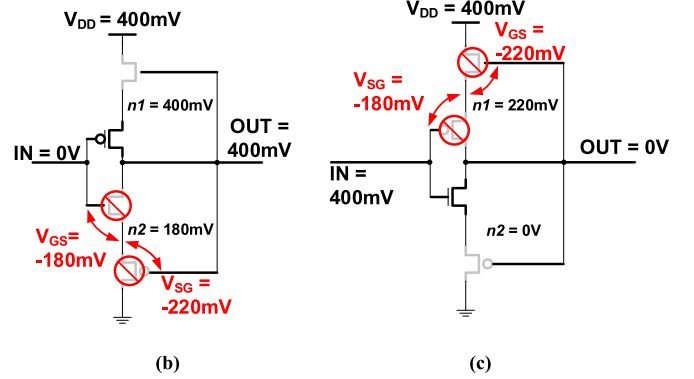
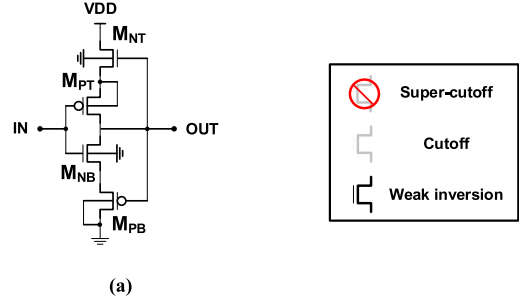


Fig. 14. (a) Schematic of a dynamic leakage-suppression logic inverter proposed in [63]. Transistor states (b) when input is equal to 0 and (c) when input is V_{DD} .

Power consumption can be decreased by lowering V_{DD} . However, a reduced on/off ratio limits the minimum supply voltage to 200–300 mV for reliable logic operation under PVT variations. A Schmitt-trigger logic that can operate with 62 mV supply voltage is proposed in [64]. This approach could reduce the power consumption with an extremely low V_{DD} , but the leakage current level is similar to the conventional logic gates, limiting the power reduction level to a linear relationship with V_{DD} .

A dynamic leakage-suppression logic (DLS) that drastically reduces the leakage current is proposed in [63]. The operation principle is explained in Fig. 14. The bottom PMOS, M_{PB} and top NMOS, M_{NT} are attached as power-gating transistors to an inverter composed of M_{PT} and M_{NB} to guarantee that all of the transistors on the leakage paths are in a super-cutoff state after stabilization. As an example, Fig. 14 (b) shows the case when 0 V is applied to the input. The intermediate node, $n1$, is connected to V_{DD} through M_{NT} , and $n2$ is set to approximately half of V_{DD} . It can be seen that V_{sg} of M_{PB} and V_{gs} of M_{NB} become negative, creating a super-cutoff state. Similarly, both M_{NT} and M_{PT} are in a super-cutoff state when the input is high. As a result, the leakage current of the proposed logic gate is approximately 320 times smaller than that of a standard low-leakage stacked inverter. Reference [63] proposes a prototype design of Cortex-M0+ processor in 180-nm CMOS technology, which consumes 0.295 pW under 550 mV supply.

VI. GNSS LOGGER

In this section, we introduce a prototype design of a GNSS logger implemented for position-tracking of an object. There is a growing demand for miniaturized low power GPS receivers for use in child safety devices, drones, smart watches, smart

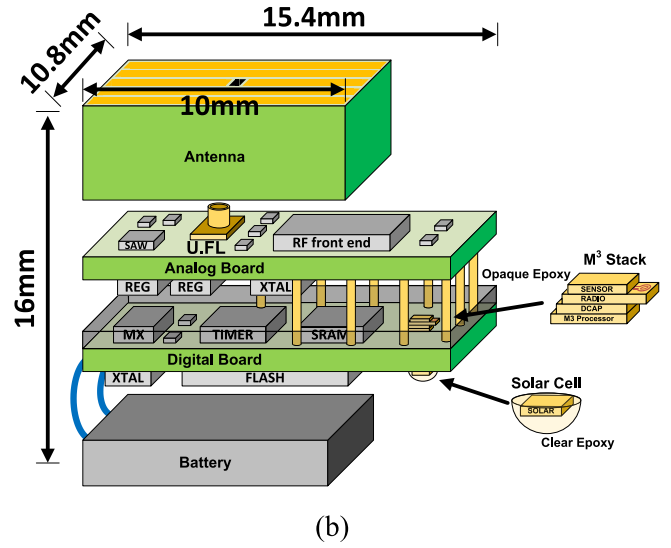
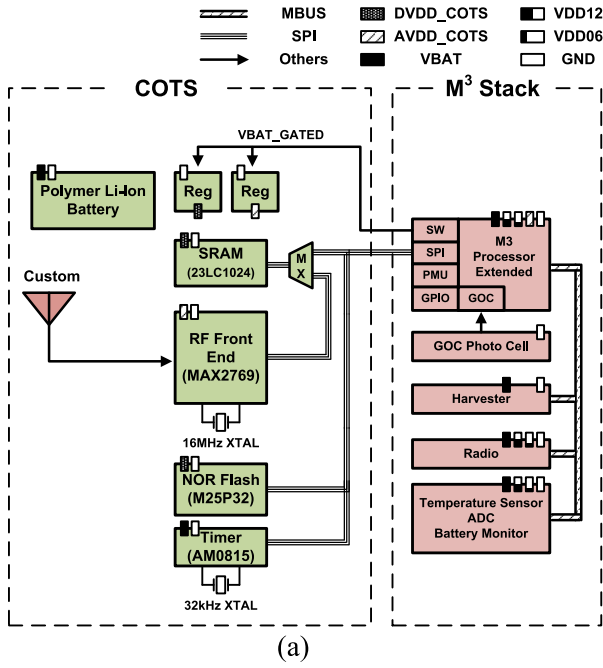


Fig. 15. (a) Block diagram of the proposed GNSS logger and (b) conceptual graph of its assembly.

grids, wearable devices and devices for tracking pets and vehicles. Many of these applications do not require a high rate or real time position-tracking, so the power requirement is significantly reduced by heavily duty-cycling. The power of the GNSS signal is lower than the channel noise, and the small form factor makes it even smaller due to the small radiation efficiency. In this work, we developed a custom electrical antenna that achieved 20.66% radiation efficiency. In addition, we implemented an autonomous system to sustain its operation with duty-cycling and energy harvesting by adopting the circuit techniques proposed in the previous sections of this paper.

Block diagram of the prototype design is shown in Fig. 15. The system is managed by a Michigan Micro Mote (M³) [27], which is a die-stacked system composed of an ARM Cortex-M0 processor layer (section V), energy harvester (section III), decoupling capacitor, global optical communication (GOC) receiver (section II-B), sensor layer (Part I) and RF transmitter (section II-A). The processor layer includes 8 kB SRAM, which is programmed by using the GOC receiver. A power gating switch in the processor layer is used to turn off the external components. A gate-induced drain leakage (GIDL) reduction technique [65] is adopted to improve the on-off ratio of the switch. The off-leakage and on-resistance are measured as 0.4 nA and 4.1 Ω , respectively. A serial peripheral interface (SPI) and a set of general purpose input/output (GPIO) are used to control the external components. A PMU based on a successive-approximation switched-capacitor DC-DC converter (section VII, [43]) provides supply voltages to the M³ stack layers. Its quiescent power and driving capability is programmable using the clock frequency so that the output driving strength is small and operates in low power mode during the sleep mode, while the output driving strength is high and operates in high mode during the active mode. The radio layer transmits the GPS data to the base station.

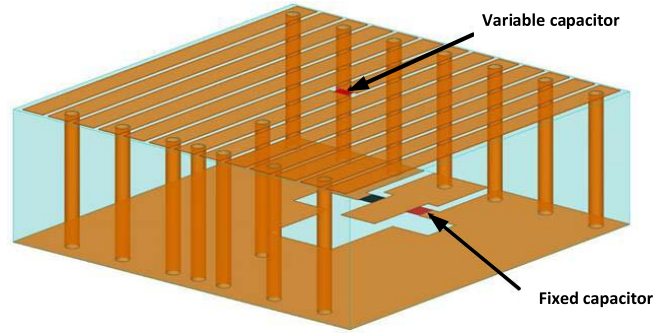


Fig. 16. A CAD drawing of the printed antenna for the GNSS logger.

The radio uses a monolithic inductor as an antenna to reduce the area requirement (section V-A, [66]) and provide a maximum bit rate of 40.7 kbps with 4.7 nJ/bit energy consumption. The sensor layer measures the temperature and battery voltage of the system, which can potentially be used to further calibrate the RF front end and operation interval [29], [33], [67].

The electrically small antenna developed for the GNSS logger is connected to the analog board through a U.FL connection. A printed 3D loop geometry, depicted in Fig. 16, is chosen for this application. The orange areas correspond to the metallized portions. A variable capacitor (top) and a fixed capacitor (bottom) are used for matching to 50 Ω . The antenna dimensions are 10×10×3.175 mm³, and it is printed on Rogers RT/duroid@5880. The copper sheet on the bottom side acts as a shield between the antenna and the rest of the system. In order to account for fabrication tolerances, a variable capacitor (cap trimmer) is used as one of the capacitors.

The antenna is simulated in ANSYS Electronics. Its radiation pattern is shown in Fig. 17 (a), and its simulated

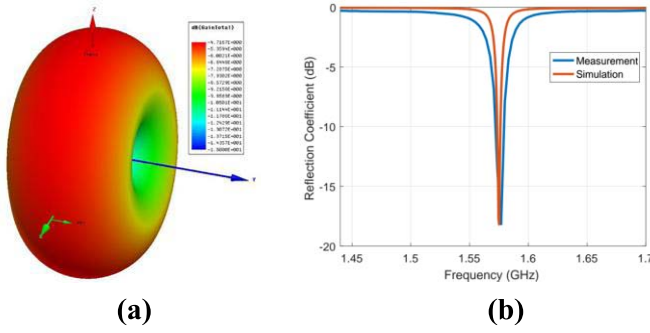


Fig. 17. (a) The radiation pattern of the loop antenna (b) Simulation and measurement results of the reflection coefficient of the antenna.

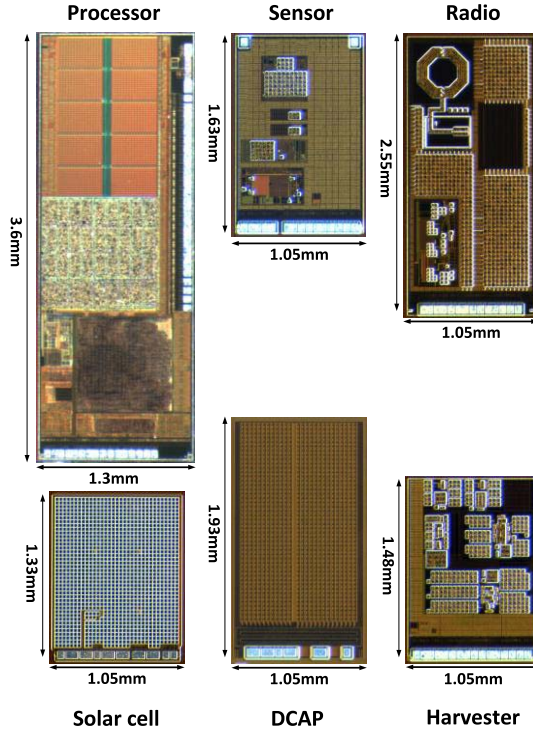


Fig. 18. Die photos of M³ system.

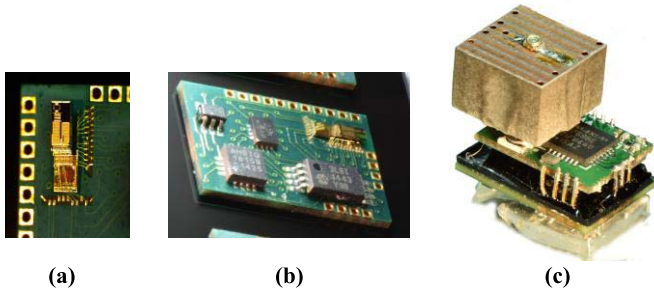


Fig. 19. Photo graphs of the proposed system (a) On-PCB die stacking and wirebonding (b) board assembly (c) entire system.

radiation efficiency is 20.66%. The reflection coefficient of the antenna, obtained through simulation and measurement, is plotted in Fig. 17 (b), and it matches well at the frequency of interest (1.57542 GHz).

The RF front-end and IF stage of the GNSS receiver incorporate commercial products and a custom antenna. The

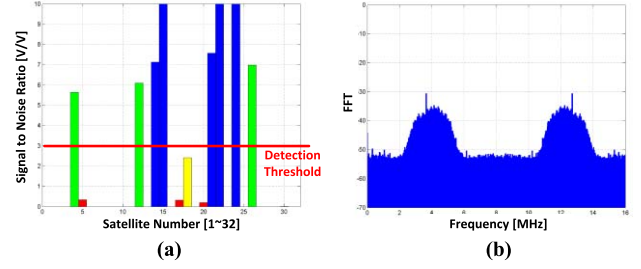


Fig. 20. (a) Measured correlation results of the output of the GNSS logger (b) Fast Fourier transform of the IF signal.

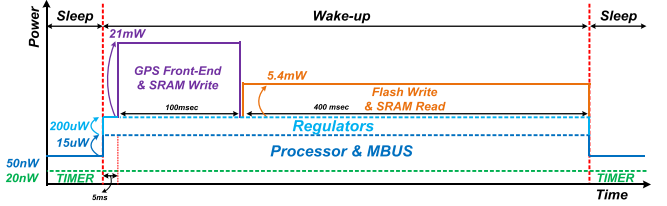


Fig. 21. (a) Measured correlation results of the output of the GNSS logger (b) Fast Fourier transform of the IF signal.

MAX2769 RF front end chip is configured to use 4 MHz IF, and the quadrature data is produced at a rate of 16 MHz. The stream of data is stored in SRAM (23LC1024) and then transferred to a NOR flash (M25P32) together with the reception time produced by the wake-up timer (AM0815). The correlation of the received data is processed in the base station after retrieving the data using the RF transmitter in the M³-stack.

The system timing diagram is shown in Fig. 21. The system is designed to have a programmable sleep time that can vary from a few minutes to multiple hours. After sleep, the system wakes up and initiates regulators, RF front-ends and SRAM within 5 ms. This time period is dominated by the startup of the 16 MHz crystal driven by the MAX2769. Then, the receiver is enabled to collect the data into the SRAM for 100 ms. The GPS data is transferred to a flash memory before the system goes back to sleep. The total energy consumption of the system is summarized in Fig. 22. The system includes a 12 mAh polymer Li-ion battery, which can provide sufficient energy to collect 1,791 fixes without harvesting energy. The system can sustain its operation permanently with 12 klux light when the system operates at 10-min intervals.

Fig. 18 shows the micrographs of the chips used to build the M³ stack, and Fig. 19 shows the digital board as well as the overall system. The size of the proposed system is $1.54 \times 1.08 \times 1.6 \text{ cm}^3$. The digital board includes the M³ stack, SRAM, flash and timer chips. The top side of the digital board is coated with black epoxy, which mechanically protects the M3 stack and blocks light. The bottom side is coated with clear epoxy to allow light to reach the PV cell. The antenna is connected to the analog board using a U.FL connector.

For testing, a GNSS signal is recorded for 30 minutes with a GNSS signal generator, LS01, and repeated using a horn antenna. The system is programmed to wake up every minute and acquire the received the GNSS signal. The measurement results of the GNSS logger after the correlation are shown in Fig. 20. The system records IF GNSS signal quantized

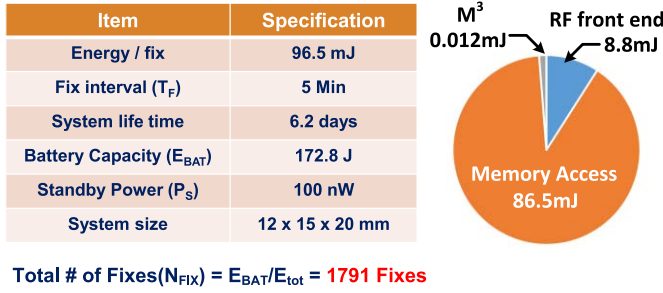


Fig. 22. Breakdown of the energy consumption.

with 2-bit ADC for 100 ms. The correlation is performed in a base station after obtaining the data through radio communication. The system successfully acquired 8-10 satellites for each acquisition, which can potentially enable ultra-low power miniaturized position tracking functions for child safety applications, drones, wearable devices and smart watches.

VII. CONCLUSION

Part II of this paper reviewed the challenges in the miniaturization of a wireless sensor node. Reduced antenna efficiency and high power consumption are identified as the two main difficulties in the implementation of a millimeter scale radio. A power oscillator that directly resonates the antenna with a negative-gm circuit was introduced as a possible solution to the problem. A sensor-initiated protocol is introduced as a method to overcome the frequency inaccuracy caused by the absence of an accurate timing reference in miniaturized sensor nodes. Optical communication is also mentioned as a good alternative communication method when a node is placed in the line-of-sight.

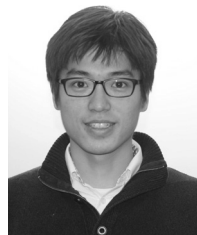
Efficient energy supply chains are also covered in Part II of this paper. As with RF data communication, a reduced antenna form factor incurs severe efficiency degradation in an RF power receiver. A resonant current mode power receiver is introduced as a possible solution. A photovoltaic cell-based energy harvester, battery management circuits and efficient PMU schemes are also explained.

As a proto-type design, a 2.7cm³ stand-alone GNSS logger is presented. The proposed logger has the capability to sustain its operation without energy harvesting for 5 days while acquiring GNSS data at five-minute intervals.

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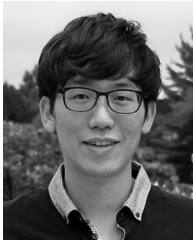
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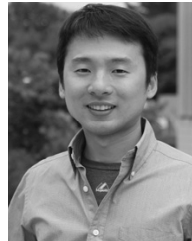
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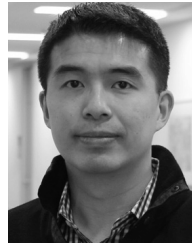
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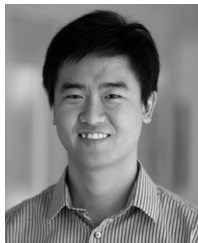


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