SUPREET JELOKA

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EDUCATION

University of Michigan, Ann Arbor September 2011 - Present
Ph.D. Candidate (Electrical Engineering : VLSI)
Advisor : Professor David Blaauw

University of Michigan, Ann Arbor September 2011 - April 2013
M.S. (Electrical Engineering : VLSI) CGPA 4/4

National Institute of Technology, Warangal (NITW), AP, India August 2003 – April 2007
Bachelor of Technology (Electronics & Communication Engineering) CGPA 9.02/10.00

PROFESSIONAL EXPERIENCE

Qualcomm Incorporated, San Diego **Intern Corporate R&D** Jun 2013 - Aug 2013

- SRAM bit cell design for low voltage of operation

Qualcomm Incorporated, San Diego **Intern QCT** May 2012 - Aug 2012

- Low power Implementation Team : Dynamic Voltage Frequency Scaling and Power Calculator

Freescale Semiconductor, Noida, India **Senior Design Engineer** Oct2010 – Jul 2011
Freescale Semiconductor, Noida, India **Design Engineer** Jul2007 – Sep2010

- Worked on seven System on Chip (SoC) design from concept to qualification phase
- Design For Test (DFT) architecture definition
- Scan, Logic BIST , Memory BIST, Analog IP test infrastructure and Silicon Bring-up
- Member of Freescale Global Test Coverage Team and Low power Design Team

TEACHING & RESEARCH EXPERIENCE

University of Michigan **Graduate Student Instructor (EECS427: VLSI Design I)** Fall 2012(Class size :63)
University of Michigan **Graduate Student Instructor (EECS427: VLSI Design I)** Winter 2012(Class size :29)
University of Michigan **Graduate Student Research Assistant** Fall 2013 – Present

- Current Projects
  - Energy recycling non-volatile memory design
  - Ultra-low energy SONOS Flash. Awaiting silicon for testing
- Configurable memory – Using SRAM bit-cell to obtain CAM functionality
- Logic-in-memory - Computation within SRAM array
- Interconnect Design - Arbitration schemes and circuits, 3D interconnect topology

PUBLICATIONS / PATENTS

- **S. Jeloka**, N. Akesh, D. Sylvester and D. Blaauw, “A 28nm configurable memory (TCAM / BCAM / SRAM) using push-rule 6T bit cell enabling logic-in-memory,” JSSC (Special issue – VLSI), April 2016.
- **S. Jeloka**, N. Akesh, D. Sylvester and D. Blaauw, “A Configurable TCAM / BCAM / SRAM Using 28nm Push-Rule 6T Bit Cell,” Symposium on VLSI Circuits, June 2015

- **S. Jeloka**, R. Das, R. Dreslinski, T. Mudge, D. Blaauw, "Hi-Rise: A High-Radix Switch for 3D Integration with Single-cycle Arbitration," IEEE/ACM International Symposium on Microarchitecture, December 2014
- S. Rao, **S. Jeloka**, R. Das, D. Blaauw, R. Dreslinski, and T. Mudge, "VIX: Virtual Input Crossbars for efficient switch allocation," Design Automation Conference, June 2014
- N. Abeyratne, **S. Jeloka**, Y. Kang, D. Blaauw, R. Dreslinski, R. Das and T. Mudge, "Quality-of-Service for a High-Radix Switch," Design Automation Conference, June 2014
- **S. Jeloka** and D. Blaauw, "Storage device, method and storage medium - Re-configurable memory circuit with in-memory compute capabilities," US patent filed, December 2014
- **S. Jeloka**, N. Abeyratne, R. Dreslinski, R. Das, T. Mudge , and D. Blaauw, "Single cycle arbitration - Circuit for on-chip virtual clock based QoS in swizzle switch," US patent filed, July 2013
- Co-Innovator for "System and method for scan testing integrated circuits - Enhanced Throughput Scan Design," US patent filed, 2010.
- Co-Author for "Debug of Scan Chain Failures on Silicon" - IEEE European Test Symposium, 2010
- First Innovator for "Low power design with buffer reuse" - Defensive Publication 2011

RELEVANT COURSE PROJECTS

- Cache design for near-threshold computing (UMich – 2013)
- Cache coherency models and its formal verification (UMich - 2013)
- Processor Design: MIPS R10k based 64 bit Out of Order 4-way Superscalar Processor (UMich – 2012)
- Custom Design: Extremely low standby leakage 8T SRAM design (UMich – 2011)
- ASIC Design: 16 Bit RISC processor with custom design for ALU, Reg file, other blocks (UMich- 2011)

HONORS AND AWARDS

- Special Engineering Scholarship, Silicon Laboratories Inc. , Winter 2014
- Roberto Padovani Scholarship, Qualcomm R&D, 2013
- Honorable Mention for GSI of EECS427, University of Michigan, Fall 2012
- Chandran Memorial Scholarship: Given annually to one VLSI Student, University of Michigan, 2012
- 2nd Prize at AMD/Michigan Design Contest in EECS627(VLSI Design II), University of Michigan, 2012
- 1st Prize at AMD/Michigan Design Contest in EECS427(VLSI Design I), University of Michigan, 2011
- One out of the twelve recipients of Narotam Sekhsaria Scholarship for higher studies, 2011
- Four 'Bravo' recognition awards at Freescale: three for dft design, one for post silicon debug (2007-11)
- Runner up at Free Your Mind, a Freescale wide innovation contest
- Thrice Awarded 'Institute merit scholarship' at NITW (2003-07)

TECHNICAL SKILLS

- Graduate Courses
  - VLSI Design I/II, Computer Architecture, Parallel Computer Architecture, Micro Architecture, Digital Integrated Technology, Digital Systems Testing, DSP Systems
- CAD tools and Programming Languages
  - Simulation tools: HSpice, Spectre, Ncverilog, VCS, Incisive Formal Verifier
  - Physical Design Tools : Virtuoso, Calibre, Design compiler, Encounter, IC Compiler, Primetime
  - HDLs : Verilog, VHDL, SystemVerilog
  - DFT tools: Fastscan, TestKompress, YieldAssist, MBISTArchitect, LBISTArchitect, Virage bist
  - Programming Languages: Perl, C++ and Assembly