Jeongsup Lee – Curriculum Vitae December 11, 2016, Ann Arbor, MI, USA

CONTACT INFORMATION
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RESEARCH INTERESTS

My research interests are in the areas of analog and mixed-mode integrated circuits. I am interested in finding innovative solutions for the applications such as communication and biomedical electronics.

EDUCATION

University of Michigan - Ann Arbor, Ann Arbor, Michigan, USA

Ph.D student, Electrical and Computer Engineering, September 2015 – Present
Advisor: Prof. Dennis Sylvester

Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea

M.S., Electrical and Computer Engineering, March 2007 – February 2009
Thesis: A Low-Power Context-Based Adaptive Variable Length Decoder for H.264/AVC Baseline Profile Using TotalZeros Caches
Advisor: Prof. In-Cheol Park

Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea

B.S., Electrical and Computer Engineering, March 2002 – February 2007

EXPERIENCE

TeraSquare Inc., Seoul, Korea

Staff Analog Design Engineer **2012 – 2015**

- ❑ 12.5Gbps Transceiver IC development
  - CML-less 12.5Gbps SST-type Tx design
- ❑ Quad CDR IC development for IEEE 100GE (TS-C44014T/TS-C44014R)
  - 28Gbps CML-type Tx design
  - Internal automatic phase calibration circuit design
- ❑ IEEE 100GE MLG2.0 reverse gearbox IC development (TS-CM41013)
  - CML-less 11.2Gbps SST-type Tx design
- ❑ IEEE 100GE parallel CDR IC development (TS-C44013)
  - Digital top design for 8-lane 28Gbps TRx
  - Digital controller design for internal automatic DC calibration circuit
  - Bandgap reference & current mirror array design for full-chip current distribution

TLI Inc., Seongnam, Korea

Digital System Engineer **2009 – 2012**

- ❑ eDP 1-lane T-Con IC (TL2368DP) development as the project leader (IC top designer)
  - Overall chip spec. definition & test strategy establishment & top integration
  - eDP 1-lane digital IP design
  - BIST design & PWM generator design for LCD backlight control
  - Mass production test setup (Using VERIGY 93K machine)
  - Failure analysis during the LG display Co LTd.'s pre-mass-production test

❑ DisplayPort (DP) v1.1a IP development
- DP link layer design
- PCB Schematic Design
  - Reliability(HTOL, THB) test board design
  - PLL & Audio amp board design for DisplayPort audio function test
- Test & Validation
  - DisplayPort v1.1a Link layer validation using customized FPGA board
  - DisplayPort v1.1a PHY/Link compliance test setup & validation
  - Apple Inc.'s internal DisplayPort v1.1a compliance test setup & validation
- Programming
  - MCU firmware coding for DisplayPort AUX channel control (Using C language)
  - Auto DisplayPort PHY test program development for Apple Inc.'s compliance test
- Mass production (sales quantity $>$ 1M)

Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea

Research Assistant **2007 – 2009**

❑ Embedded processor & on-chip bus development
- 32-bit RISC(Core-A) Instruction Set Simulator (ISS) design
- Co-simulation with verilog-based Core-A and C-based ISS

PUBLICATIONS

1. Soon-Won Kwon, Joon-Yeong Lee, Jinhee Lee, Kwangseok Han, Taeho Kim, Sangeun Lee, **Jeong-Sup Lee**, Taehoon Yoon, Hyosup Won, Jinho Park, and Hyeon-Min Bae, "An Automatic Loop Gain Control Algorithm for Bang-Bang CDRs," in *IEEE Trans. Circuits Syst. I*, vol.62, no.12, pp.2817-2828, Dec. 2015.
2. Taehoon Yoon, Joon-Yeong Lee, Kwangseok Han, **Jeong-Sup Lee**, Sangeun Lee, Taeho Kim, Hyosup Won, Jinho Park, and Hyeon-Min Bae, "A 100-GbE Reverse Gearbox IC in 40nm CMOS for Supportin Legacy 10- and 40-GbE Standards," in *IEEE Symp. VLSI Circuits*, 2015.
3. Hyosup Won, Taehoon Yoon, Jinho Han, Joon-Yeong Lee, Jong-Hyeok Yoon, Taeho Kim, **Jeong-Sup Lee**, Sangeun Lee, Kwangseok Han, Jinhee Lee, Jinho Park, and Hyeon-Min Bae, "A 0.87-W Transceiver IC for 100-Gigabit Ethernet in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol.50, no.2, pp.399-413 ,Feb. 2015.
4. **Jeong-Sup Lee** and In-Cheol Park, "Capacitor Array Structure and Switch Control for Energy-Efficient SAR Analog-to-Digital Converters **[Best Student Paper Finalist]**," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seattle, USA, pp. 236-239, May 2008.

SKILLS

Languages
C, C++, Visual C#, Perl, Verilog-A, Verilog
Tools
Verdi, Design Compiler, PrimeTime, NC-verilog, Tetramax ATPG, Conformal LEC, Virtuoso, Spectre, Calibre DRC/LVS/PEX, Cadence AMS simulator

REFERENCES

Available upon request