

A Constant Energy-Per-Cycle Ring Oscillator Over a Wide Frequency Range for Wireless Sensor Nodes

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Abstract—This paper presents an energy-efficient oscillator for wireless sensor nodes (WSNs). It avoids short-circuit current by minimizing the time spent in the input voltage range from V_{thn} to $[V_{dd} - |V_{thp}|]$. A current-feeding scheme with gate voltage control enables the oscillator to operate over a wide frequency range. A test chip is fabricated in a $0.18\ \mu\text{m}$ CMOS process. The measurements show that the proposed oscillator achieves a constant energy-per-cycle (EpC) of $0.8\ \text{pJ/cycle}$ over the 21–60 MHz frequency range and is more efficient than a conventional current-starved ring oscillator (CSRO) below 300 kHz at 1.8 V supply voltage. As an application example, the proposed oscillator is implemented in a switched-capacitor DC–DC converter. The converter is 11%–56% more efficient for load power values ranging from 583 pW to 2.9 nW than a converter using a conventional CSRO.

Index Terms—Current starved, energy efficient, leakage based, low power, oscillator, switched-capacitor DC–DC, converter, wide frequency range, wireless sensor node (WSN).

I. INTRODUCTION

WIRELESS sensor nodes (WSNs) are an important part of the emerging Internet of Things [1], opening up new applications in areas related to medicine, infrastructure, and surveillance [2]–[5]. Recent trends in WSNs have focused on designing energy-efficient systems to realize energy autonomy using an energy harvester [6], [7]. For this goal, WSNs adaptively optimize themselves according to harvested energy, load power, and battery voltage condition using circuits such as voltage converters, dynamic frequency scaled circuits, and adaptive analog/RF circuits [7]–[12]. One adaptive technique involves changing the operation speed by modulating the clock frequency for optimum efficiency [10]–[12].

As an example, Fig. 1 shows a switched-capacitor DC–DC converter in a WSN with a lithium battery. It delivers power from a high battery voltage to a level where load circuits efficiently operate (e.g., 0.6 V for microprocessors [13] and 0.45 V for SRAM [14]). Its energy efficiency mainly depends on switching and conduction losses [15]. Switching loss arises from energy spent to charge (or discharge) parasitic capacitance and drive power switches. Conduction loss results from the ON-resistance of power switches due to the Joule effect. As the operating frequency increases, the switching loss rises

Manuscript received July 07, 2015; revised September 22, 2015 and November 19, 2015; accepted January 04, 2016. Date of publication February 02, 2016; date of current version March 02, 2016. This paper was approved by Associate Editor Marian Verhelst.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2517133

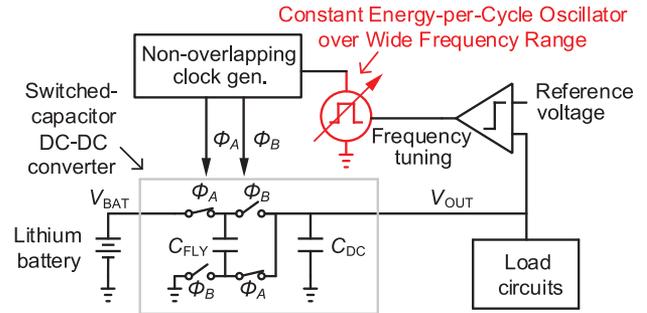


Fig. 1. Capacitive step-down converter in a WSN with a lithium battery.

according to $CV_{dd}^2 f$, whereas conduction loss decreases in the slow-switching limit (SSL) and becomes saturated in the fast-switching limit (FSL) [16]. The ideal operating point (i.e., that offering the highest efficiency) occurs at a frequency where the sum of those losses is minimized. However, this point varies according to the load power condition. For instance, the converter in [13] uses a switching frequency of 340 Hz for a 1–10 nW load power in standby mode, whereas it uses 335 kHz for 1–10 μW loads in active mode.

The oscillator in a WSN must not only cover a wide frequency range but also consume power proportional to the frequency, which becomes critical as the frequency is lowered. This quality ensures that the oscillator does not dominate the overall power at slow speeds and low load conditions. For this requirement, a ring oscillator is a good candidate due to its wide tuning range, small silicon area, and compact design. However, in ring oscillator circuits, the proportionality of power with frequency has not typically been considered as an important factor [17]–[23]. Although [24] proposed a ring oscillator that consumes power proportional to the frequency, the circuit was not verified in silicon, and its lowest frequency range is limited to 1.75 kHz.

This paper proposes a constant energy-per-cycle ring oscillator (CERO) in which the power is proportional to the frequency over a wide frequency range in order to maintain energy efficiency for adaptive circuits in WSNs. It is based on an oscillator topology that charges (or discharges) capacitance using the sub-threshold (weak inversion) current of a MOS transistor without short-circuit current [25]. The current and the oscillator are referred to as “leakage” and “leakage-based oscillator,” respectively, in this paper. The CERO employs a current-feeding scheme with gate voltage control in a leakage-based oscillator to efficiently control the output frequency. Due to the rapid escape from the voltage range between V_{thn} (NMOS threshold voltage) and $[V_{dd} - |V_{thp}|]$ (PMOS threshold voltage), the oscillator power consumption scales linearly with the frequency

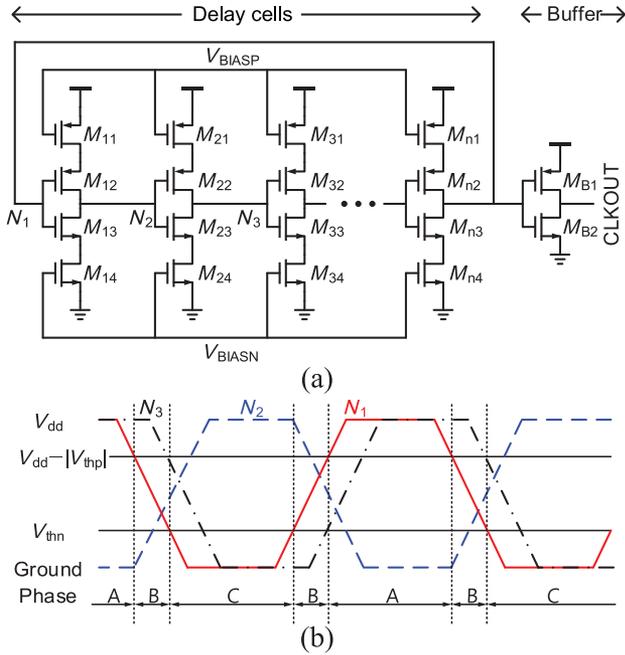


Fig. 2. CSRO. (a) Circuit diagram. (b) Internal node waveforms.

by largely avoiding short-circuit current. The prototype oscillator is implemented in a standard $0.18\ \mu\text{m}$ CMOS process. It achieves a constant $0.8\ \text{pJ/cycle}$ over the $21\ \text{Hz}$ – $60\ \text{MHz}$ frequency range at a power supply of $1.8\ \text{V}$, which is a higher efficiency than that of a current-starved ring oscillator (CSRO) below $300\ \text{kHz}$.

This paper is organized as follows. Section II describes a conventional CSRO and identifies its limitations in the targeted application space. Section III presents the proposed energy efficient oscillator, and Section IV reports the test chip measurement results. Section V shows an application example of a switched-capacitor DC–DC converter implemented with the proposed oscillator. Finally, Section VI concludes this paper.

II. CONVENTIONAL CSRO

Fig. 2(a) shows a conventional CSRO [26]. Its delay stage consists of a delay generator (M_{X2} and M_{X3}) and a current-starving circuit (M_{X1} and M_{X4}). Charging (or discharging) current depends on the source-to-drain resistance of the current-starving circuit, which is controlled by its gate voltage (V_{BIASP} and V_{BIASN}). The gate voltage control enables the oscillator to tune the output clock frequency. An internal signal (N_1) is connected to a logic inverter (M_{B1} and M_{B2}) to buffer the output.

Fig. 2(b) shows the simplified waveform of the internal nodes (N_1 , N_2 , and N_3) in steady state. In Phases A and C, the first delay cell uses current only for charging or discharging its load capacitance since either M_{12} or M_{13} is turned OFF. In Phase B, however, $V(N_1)$ lies between V_{thn} and $[V_{\text{dd}} - |V_{\text{thp}}|]$ and turns ON both transistors, causing short-circuit current.

The current through the delay cells is limited by the current-starving transistor, and the limited current is proportional to the output clock frequency. Thus, the increased average power due to the short-circuit current through the delay cell scales

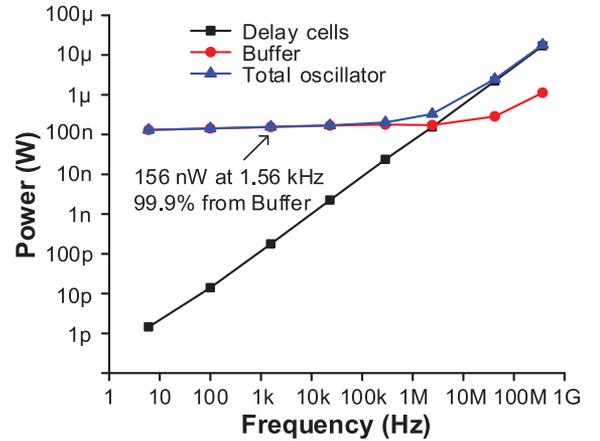


Fig. 3. Simulated power consumption of a seven-stage CSRO with an inverter output buffer across frequencies.

with frequency and is acceptable, although the absolute power consumption is increased. However, the short-circuit current through the inverter buffer is not limited and significantly increases oscillator power consumption, as shown in Fig. 3. The output buffer dominates the total oscillator power below $1\ \text{MHz}$, since the short-circuit current through the buffer does not scale down at slower frequencies. For example, at $1.56\ \text{kHz}$ clock generation, the buffer consumes 99.9% of the oscillator power. Thus, circuits using this oscillator cannot reduce their power consumption below $130\ \text{nW}$, even in a low-power standby mode.

III. PROPOSED ENERGY-EFFICIENT OSCILLATORS

A. Proposed CERO

To overcome the poor power scalability over frequency of CSROs, we propose a CERO, for which power scales linearly with frequency. Fig. 4(a) shows the circuit diagram of the delay cell. It uses leakage-based oscillator topology, which was initially designed for a fixed, slow frequency (e.g., $100\ \text{Hz}$ with $10\ \text{pW}$) [25]. To adjust the output clock speed, a gate voltage control scheme is introduced.

The delay cell includes input transistors (M_{1A} , M_{1B} , M_{4A} , and M_{4B}) and back-to-back inverters (M_{2A} , M_{2B} , M_{3A} , and M_{3B}). The input and output signals use differential configurations. The back-to-back inverters accelerate the changing output status to reduce short-circuit current. In addition, current control transistors (M_{CPA} , M_{CPB} , M_{CNA} , and M_{CNB}) are added to change the switching frequency by adjusting the charging and discharging currents.

The CSRO and CERO modulate their output frequencies in opposite manners. Specifically, CSRO changes its output frequency by limiting current, whereas the proposed approach for the CERO injects more current to change the frequency. To achieve a higher clock frequency, more charging (or discharging) current is added via the current control transistors. The oscillator frequency can potentially be modified using different load capacitances and transistor sizes, but a gate voltage control scheme is selected to minimize the overhead from additional capacitance.

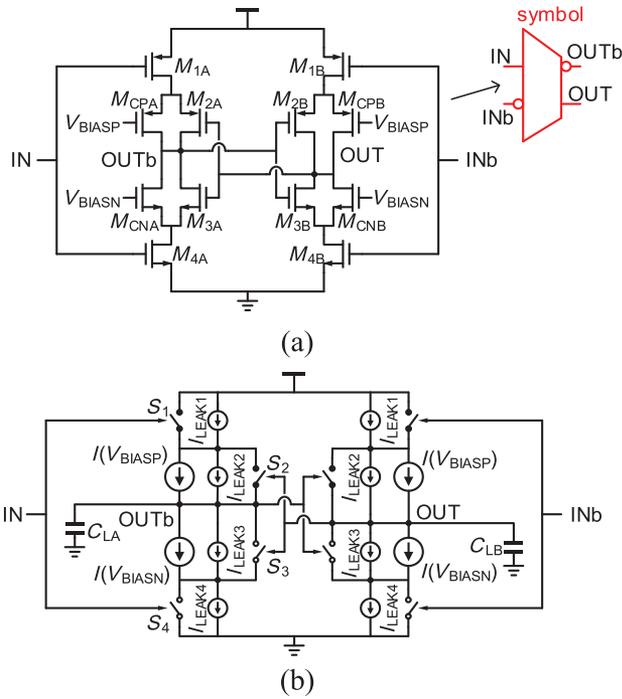


Fig. 4. Delay cell of proposed CERO. (a) Circuit diagram. (b) Simplified model.

Fig. 4(b) shows a simplified model of a delay cell of the proposed oscillator. The current control transistors are represented by current sources of $I(V_{BIASP})$ and $I(V_{BIASN})$, and the input transistors and back-to-back inverters are modeled by ideal switches with leakage current sources $I_{LEAK1-4}$. C_{LA} and C_{LB} are the sum of the parasitic capacitance charged or discharged.

Fig. 5(a) shows the three-stage proposed oscillator as an example of a CERO. Two inverters are added as buffers for balanced output transitions. To better explain circuit operation, the condition without additional current ($I(V_{BIASX}) \approx 0$ A) is first discussed for simplicity. Based on the model shown in Fig. 4 (b), Fig. 5(b) and (c) shows the oscillator internal signals in steady state and the circuit behavior of the first stage delay cell, respectively. Here, N_{1A} , N_{1B} , N_{2A} , and N_{2B} are IN, INb, OUTb, and OUT of the first-stage delay cell in the oscillator, respectively. For simplification, only the left half of the circuit is displayed.

In Phase A, N_{2B} (OUT) is lower than V_{thn} , and N_{1A} (IN) becomes equal to the supply voltage. Thus, S_2 and S_4 are connected, whereas S_1 and S_3 are disconnected. There are two leakage paths: 1) comes from I_{LEAK3} and S_4 and 2) derives from I_{LEAK1} and S_2 . Since V_{ds} of M_{3A} is larger than V_{sd} of M_{1A} due to the high N_{2A} (OUTb), the leakage path to ground dominates. Fig. 6(a) shows the simulated drain current of a minimum-size NMOS transistor with $V_{gs} = 0$ V. It shows that $I_{ds} = 0$ A at $V_{ds} = 0$ V, while $I_{ds} = 21$ fA at $V_{ds} = V_{dd} - |V_{thp}|$. The dependency of I_{ds} on V_{ds} can be found in the subthreshold current equation of the EKV model [27] (letting $V_{gs} = 0$ V) expressed as follows:

$$I_{ds} = 2n\mu C_{ox} \frac{W}{L} U_T^2 e^{-\frac{V_{th}}{U_T}} \left(1 - e^{-\frac{V_{ds}}{U_T}} \right). \quad (1)$$

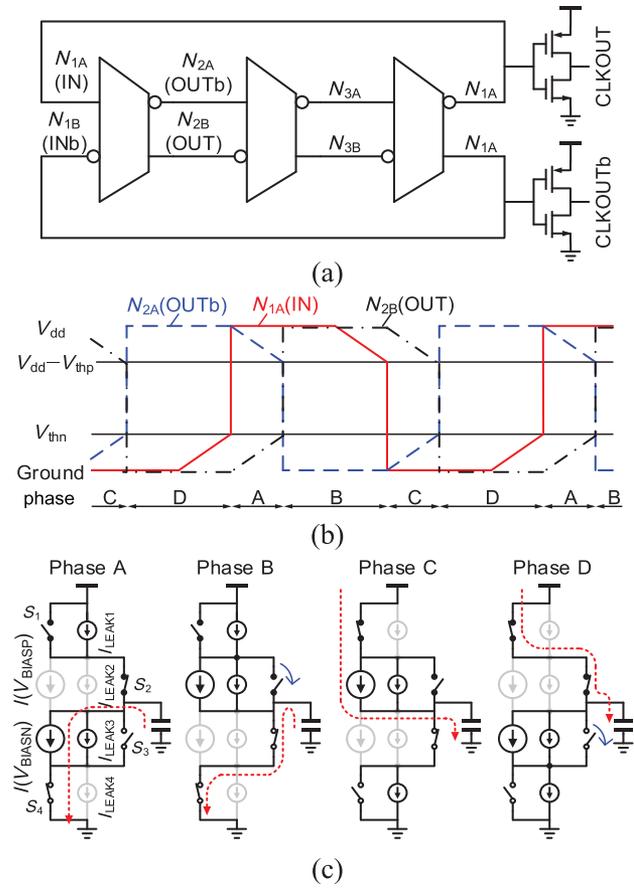


Fig. 5. Three-stage proposed CERO. (a) Oscillator implementation. (b) Internal nodes. (c) Circuit status of a delay cell.

Here, μ is the mobility, C_{ox} is the oxide capacitance, W is the transistor width, L is the transistor length, n is the slope factor ($n \equiv dV_g/dV_p$, where V_p is the pinchoff voltage), and U_T is the thermal voltage (kT/q). Furthermore, the current can increase due to drain-induced barrier lowering (DIBL) and gate-induced drain leakage (GIDL) in advanced technologies.

Fig. 6(b) shows the output discharging current (the difference between the pull-down and pull-up current) in the single delay cell [Fig. 4(a)] when IN and INb are the supply voltage and ground, respectively. As the output voltage (OUTb) changes from the supply voltage to ground, the output discharging current is always positive, which guarantees the output voltage transition to ground. Similarly, the opposite input condition (0 V IN and 1.8 V INb) drives OUTb to the supply voltage. With higher additional bias current, $I(V_{BIASN})$ or $I(V_{BIASP})$, the current does not change its sign but only increases the amplitude, decreasing the charging or discharging time. The period of the oscillator mainly depends on the discharging current ($I_{LEAK3} + I_{BIASN} - I_{LEAK1}$), along with the output charging current ($I_{LEAK2} + I_{BIASP} - I_{LEAK4}$) in Phase C, which is the complementary of Phase A.

Fig. 6(c) shows the voltage transfer curve of the single delay cell. Its hysteresis becomes larger (up to 91% of the supply voltage) as the bias current is reduced. The output voltage transition happens when one of the input transistors becomes weaker than the transistors of the back-to-back inverters. For example,

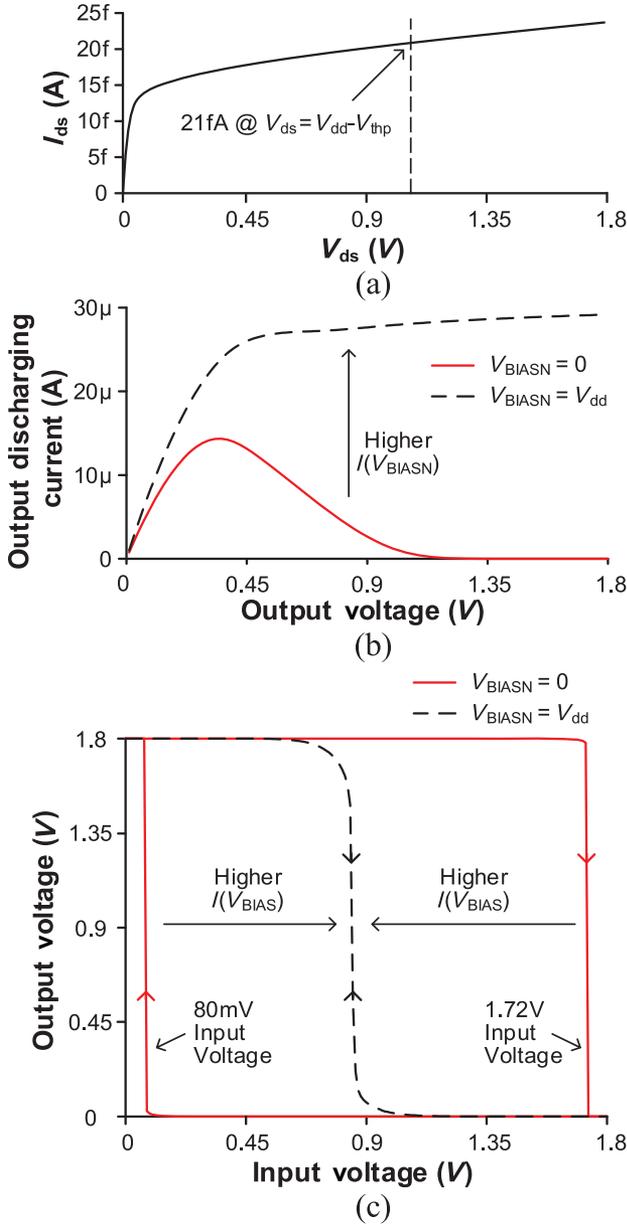


Fig. 6. Simulated single delay cell. (a) I_{ds} versus V_{ds} (minimum-size transistor). (b) Output discharging current across output voltages. (c) Voltage transfer curve (Input: IN/Output: OUTb).

when N_{1A} (IN) becomes 1.72 V in the beginning of Phase A, I_{LEAK1} equals I_{LEAK3} . As N_{1A} (IN) increases above 1.72 V, N_{2A} (OUTb) decreases since M_{1A} becomes weaker, and $I_{LEAK1} < I_{LEAK3}$. Due to the hysteresis, the output transition is stable as the input voltage changes.

Phase B begins when N_{2A} (OUTb) drops below $[V_{dd} - |V_{thp}|]$ and N_{2B} (OUT) rises above V_{thn} , turning ON S_3 (Fig. 5). Since N_{1A} (IN) is still higher than $[V_{dd} - |V_{thp}|]$, S_4 is connected, whereas S_1 is disconnected. This situation leads to the immediate discharging of C_{LA} and charging of C_{LB} (Fig. 4). S_2 is connected in the beginning of the phase but disconnected as N_{2B} (OUT) is charged above $[V_{dd} - |V_{thp}|]$. However, this situation does not affect the output voltage transition since the pull-down current is larger than the pull-up

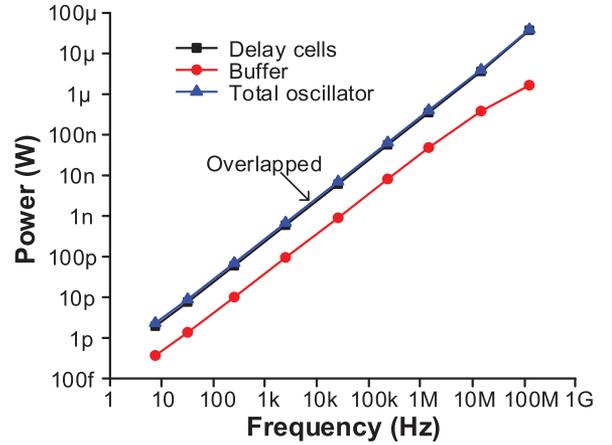


Fig. 7. Simulated power consumption of a seven-stage proposed CERO with an inverter output buffer across frequencies.

current, which is limited by I_{LEAK1} and turned OFF S_1 . The discharged output voltage (N_{2A} , OUTb) increases the strength of M_{2B} and raises the speed at which the complementary output voltage (N_{2B} , OUT) is pulled up. The higher N_{2B} (OUT) enhances the conductance of M_{3A} and increases the speed at which N_{2A} (OUTb) is pulled up. This positive feedback is formed by the back-to-back inverters that work as a latch and enable the rapid voltage transition. It helps effectively avoid short-circuit current in the oscillator itself and buffers by minimizing the time spent in the input voltage range between V_{thn} and $[V_{dd} - |V_{thp}|]$. Note that the short-circuit current through a buffer degrades energy efficiency in the conventional CSRO. Phases C and D are complementary to Phases A and B, respectively.

Since the voltage transition time in Phases B and D is negligible, the clock period of this oscillator is dictated by the sum of the discharging time of OUTb from V_{dd} to $[V_{dd} - |V_{thp}|]$ (the charging time of OUT from ground to V_{thn}) during Phase A and the charging time of OUTb from ground to V_{thn} (the discharging time of OUT from V_{dd} to $[V_{dd} - |V_{thp}|]$) during Phase C. Due to the small leakage currents employed, this oscillator generates a clock with a long period. It can generate a slow clock with higher energy efficiency than CSRO since the short-circuit current issue is resolved, as described above.

To cover a wide frequency range, including higher frequencies, the oscillator output frequency can be modulated by controlling V_{BIASP} and V_{BIASN} and thus changing $I(V_{BIASP})$ and $I(V_{BIASN})$, respectively. This changes the charging (or discharging) slope of the internal voltages shown in Fig. 5(b) in the voltage range below V_{thn} or above $[V_{dd} - |V_{thp}|]$. As shown in Fig. 5(c), the supplemented current paths through the additional transistors increase the discharging current in Phase A and the charging current in Phase C. Hence, the discharging and charging currents become $[I_{LEAK3} + I(V_{BIASN}) - I_{LEAK1}]$ and $[I_{LEAK2} + I(V_{BIASP}) - I_{LEAK4}]$, respectively. Fig. 7 shows the simulated power consumption of the proposed CERO across frequencies, which demonstrates its power proportionality with frequency. Compared with the conventional CSRO (Fig. 3), the CERO achieves a constant energy-per-cycle (EpC) (0.3 pJ/cycle

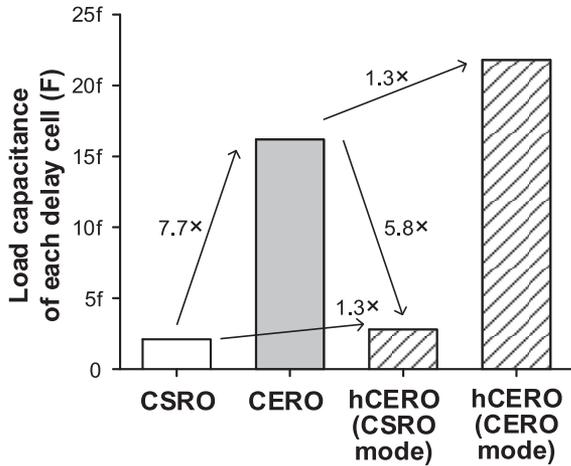


Fig. 8. Simulated capacitance of each delay cell in CSRO, CERO, and hCERO.

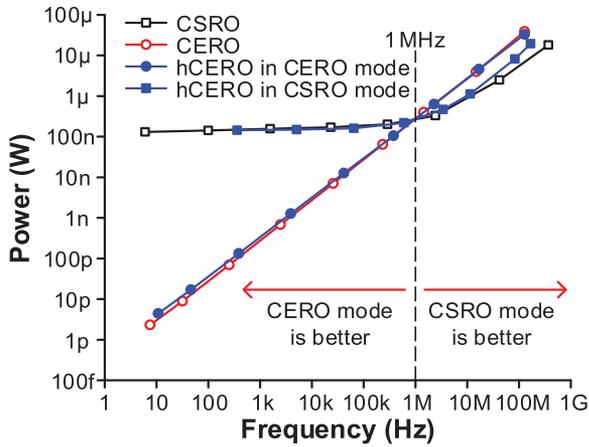


Fig. 9. Simulated power consumption of CSRO, CERO, and hCERO across frequencies.

from 7.5 Hz to 128 MHz in simulation) by avoiding the short-circuit current through the buffer. Here, the EpC is the amount of required energy for one clock cycle, which is a commonly used figure-of-merit for energy-efficient oscillators [28], [29].

B. Extension To CERO (Hybrid CERO)

The CERO achieves a power consumption that scales directly with the frequency. Compared with CSRO, however, its load capacitance is 7.7-fold larger (Fig. 8) due to the additional transistors and differential structure. Thus, as shown in Fig. 9, the CERO power is higher than that of CSRO above 1 MHz, where dynamic power dominates over short-circuit current.

To address the higher energy consumption of the CERO at high frequencies, we therefore propose an extension to the CERO using a hybrid scheme referred to as the hCERO. The hCERO approach selectively employs one of two oscillator topologies by changing switch configuration, thereby achieving improved energy efficiency at high frequencies at the cost of additional complexity and area. Fig. 10(a) shows a delay cell for the hCERO. Five transistors ($M_{S1} - M_{S5}$) are added to the basic CERO delay cell. By connecting all the switches in the CERO mode [Fig. 10(b)], this oscillator becomes equivalent

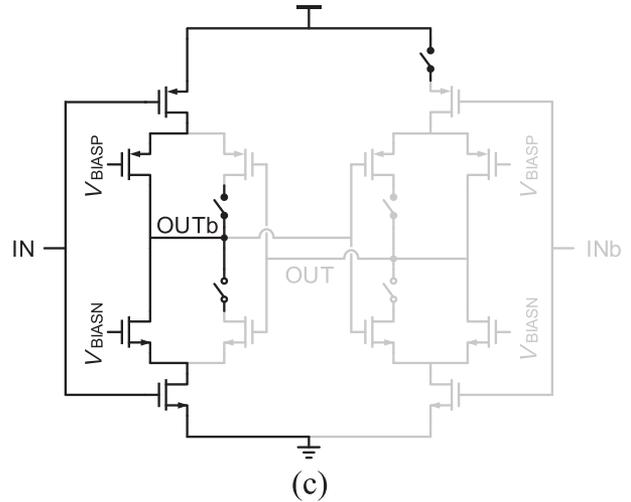
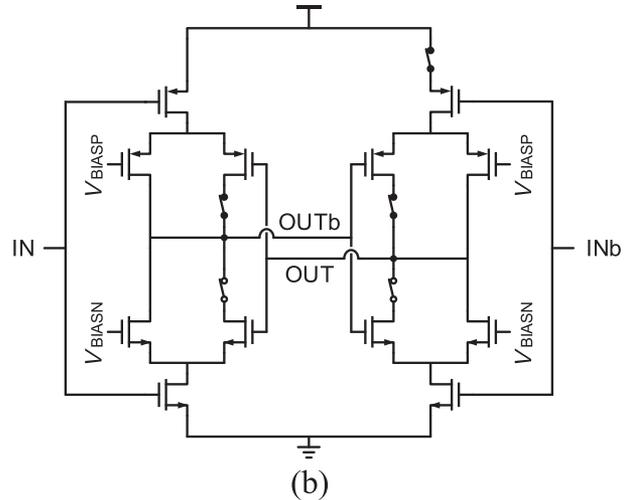
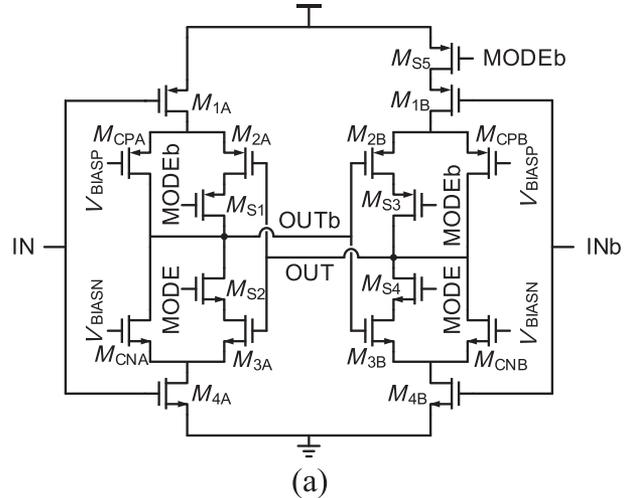


Fig. 10. Proposed extension to the CERO (hCERO). (a) Circuit diagram of a delay cell. (b) CERO mode. (c) CSRO mode.

to the CERO. In contrast, by disconnecting the switches in the CSRO mode [Fig. 10(c)], the circuit operates like CSRO. Half of a delay cell is disabled by a power gating switch (M_{S5}), and back-to-back inverters are disassembled by disconnecting M_{S1} and M_{S2} . The remaining active parts are the input and current control transistors, which provide CSRO functionality.

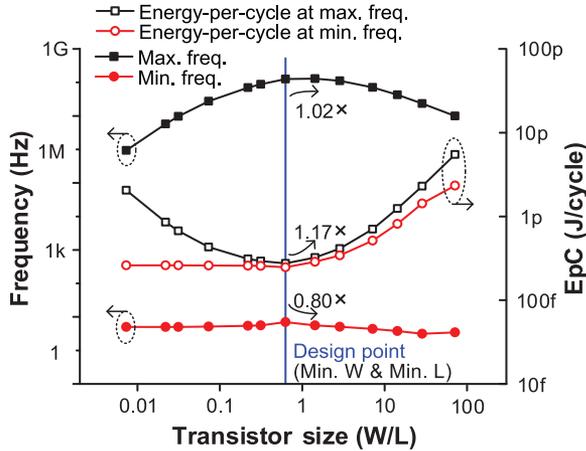


Fig. 11. Simulated frequency and EpC of CERO across current control transistor sizes.

In the CSRO mode, the hCERO switches a $5.8 \times$ lower load capacitance than the CERO (Fig. 8) due to the single-ended scheme. Due to the reduced switching capacitance, the hCERO in the CSRO mode is more efficient than the CERO above 1 MHz, where the impact of short-circuit current is not significant (shown in Fig. 9). The frequency breakpoint to switch between modes can be set when the oscillator is designed and placed in a simple lookup table.

C. Circuit Design

The oscillator maximum and minimum output frequencies depend on the size of the current control transistors. At the same time, additional switching capacitance reduces energy efficiency. Minimum width and length devices offer near-ideal maximum frequency with minimal EpC, as shown in Fig. 11. Note that using a $2 \times$ larger transistor offers only a 2% increase in the maximum frequency at the expense of 17% in energy efficiency. Thus, the current control transistors are designed with the minimum width and length size. Furthermore, to reduce leakage current and switching capacitance, transistors for the inputs, back-to-back inverters, and mode switches are also implemented with the minimum size in both the CERO and the hCERO.

In the proposed oscillator, bias voltages are needed to set the voltage-controlled currents and hence the frequency. Fig. 12 shows the output frequency and generated bias current across the bias voltages. Of the frequency range in the log domain, 87% is covered by ≤ 0.8 V bias voltage since transistors operate in the weak-inversion region ($V_{th} \approx 0.7$ V).

Fig. 13 shows a simple bias voltage generator based on a voltage divider. The voltage divider uses stacked diode-connected transistors to generate different voltages that are used for bias voltages. One of the taps is connected to the gates of the current control transistors through a transmission gate-based multiplexer. In this design, same-sized transistors are used for the voltage division to minimize device mismatch.

Fig. 14 shows the bias voltage steps for different numbers of diode stacks and the frequency change per step at a bias voltage of ~ 0.35 V. The supply voltage and number of diode

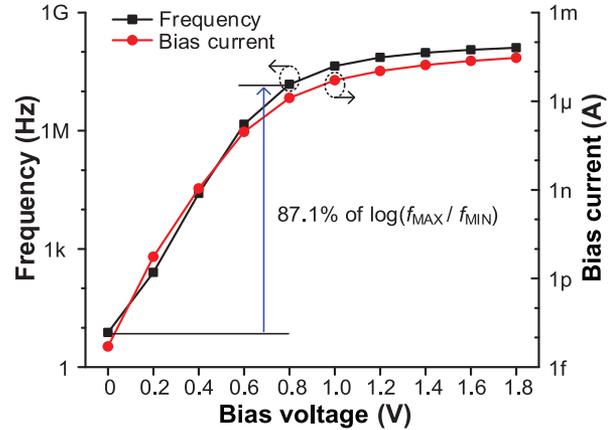


Fig. 12. Simulated frequency and bias current of CERO across bias voltages.

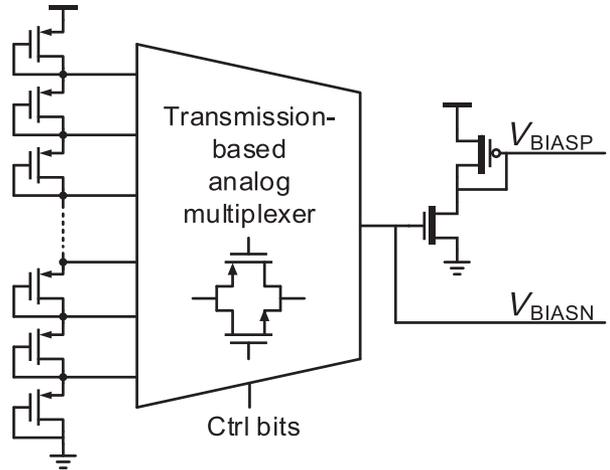


Fig. 13. Voltage divider-based bias voltage generator.

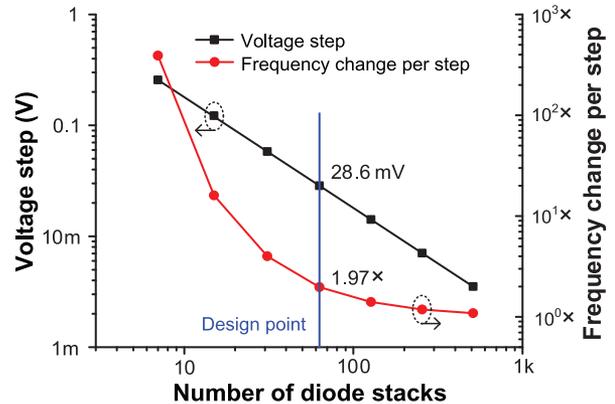


Fig. 14. Simulated voltage step and frequency change per step of voltage divider-based bias voltage generator across numbers of diode stacks.

stacks determine the bias voltage step size. Considering an analog multiplexer implementation, 63 diode-connected transistors are used for the voltage divider, which offers a 28.6 mV voltage step and $1.97 \times$ frequency change per step. The bias voltage generator is designed with high V_{th} transistors sized at $0.5/0.185 \mu\text{m}$ (W/L) and consumes 1.7 pW. With this low-power bias generator, the total power scales down with the

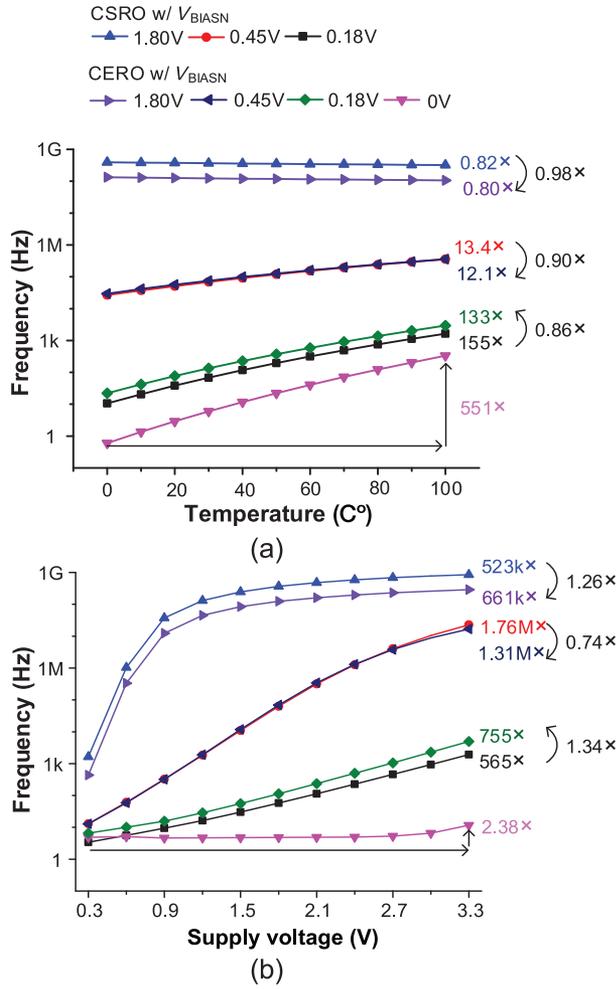


Fig. 15. Simulated frequency variation on CSRO and CERO using a voltage divider-based bias voltage generator by (a) temperature variation (1.8 V supply voltage and TT corner) and (b) supply voltage variation (27 °C and TT corner).

frequency to 32 Hz, while maintaining an EpC between 0.27 and 0.33 pJ/cycle in simulation.

The voltage divider-based bias voltage generator achieves power scalability at low frequencies due to its extremely low power, but it results in significant variation in the output clock frequency in the face of temperature variation ($551\times$ change across 0°C – 100°C at a bias voltage of 0 V) and supply voltage change ($1.31\text{ M}\times$ across 0.3–3.3 V at $\frac{1}{4}V_{\text{dd}}$ bias voltage), as shown in Fig. 15. However, compared to CSRO with the same bias voltage generator, the frequency of the CERO demonstrates a similar sensitivity to temperature ($<0.98\times$) and supply voltage variation ($<1.34\times$). Three bias voltages are selected to set the output frequency to different levels. A voltage of 0 V is only used for the CERO, since the CSRO does not work without bias current.

Fig. 16 shows the output frequency and EpC from different corner simulations. The output frequency of the CERO [Fig. 16(a)] is sensitive to global process variation and can be changed by $171\times$. Compared to the CSRO, the CERO has a similar sensitivity to process variation (up to 2% ratio increase). On the other hand, the EpC of the CERO [Fig. 16(b)] is less sensitive to process variation ($0.07\times$ at $0.18\text{ V }V_{\text{BIASN}}$) than

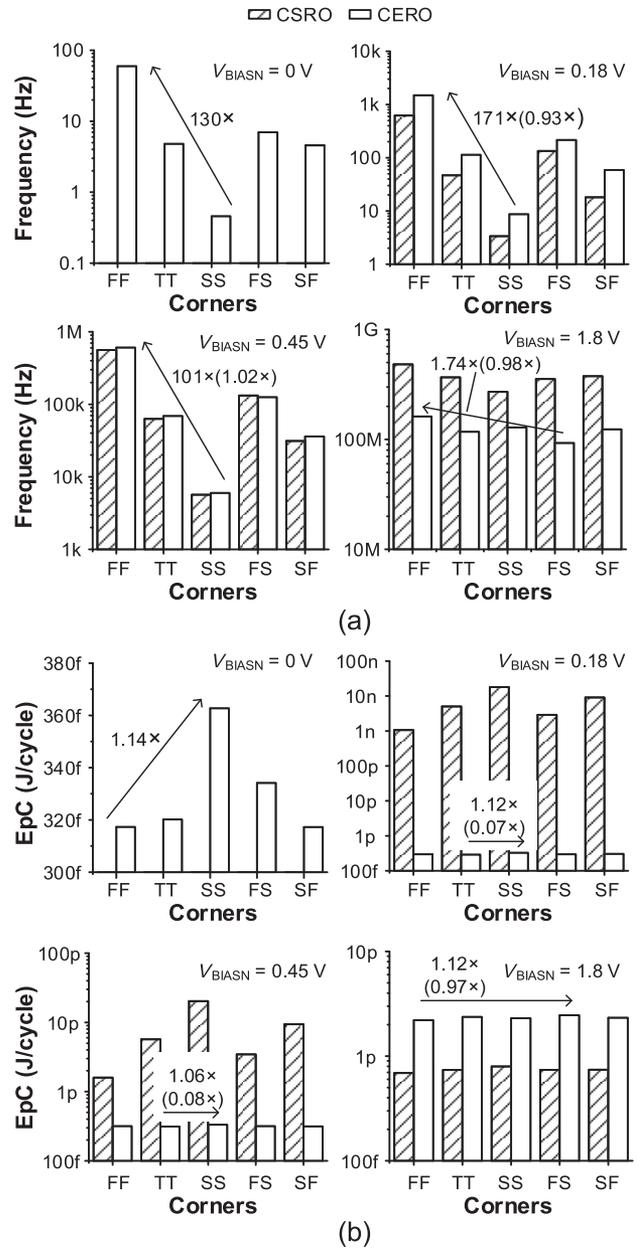


Fig. 16. Corner simulations of CSRO and CERO (27 °C and 1.8 V supply voltage). (a) Oscillator frequency. (b) EpC [(): [Max./Min.] of CERO/[Max./Min.] of CSRO].

the EpC of the CSRO due to the characteristics of a constant EpC. Although the output frequency changes, the EpC is maintained because the power consumption is proportional to the frequency. In addition, the CERO achieves a lower EpC than the CSRO at 0.18 and 0.45 V V_{BIASN} by avoiding the short-circuit current through the output buffer; however, its EpC is higher at 1.8 V V_{BIASN} due to more switching capacitance.

Fig. 17 shows the Monte Carlo simulation results with 1 k samples for each data point, including global process and local mismatch variation. The CSRO and CERO have the same size transistors. As shown in Fig. 17(a), the relative variations of the oscillator frequency (σ/μ) are similar for these two types of oscillators, with a higher σ/μ at lower bias voltage due

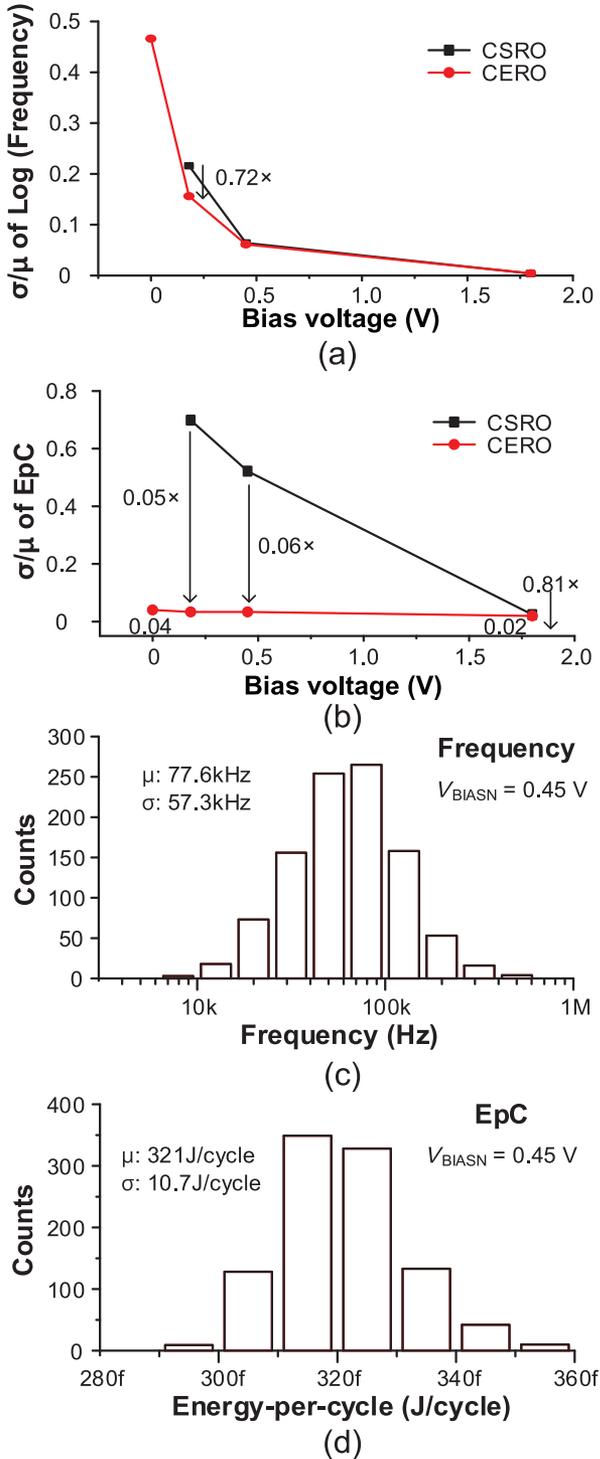


Fig. 17. Monte Carlo simulations of CSRO and CERO (27°C and 1.8 V supply voltage). (a) σ/μ of oscillator frequency. (b) σ/μ of EpC. (c) Histogram of oscillator frequency at 0.45 V V_{BIASN} . (d) Histogram of EpC at 0.45 V V_{BIASN} .

to the deeper weak-inversion operating region of the transistors. Here, the logarithmic value of frequency is used, since its spread is closer to a normal distribution [Fig. 17(c)] than that of the raw value. The variation can be similar in the CERO and the CSRO since they have similar dominant variation sources in the slow frequency range, the current-starving transistors in the CSRO (M_{X1} and M_{X4} in Fig. 2) and current-controlling

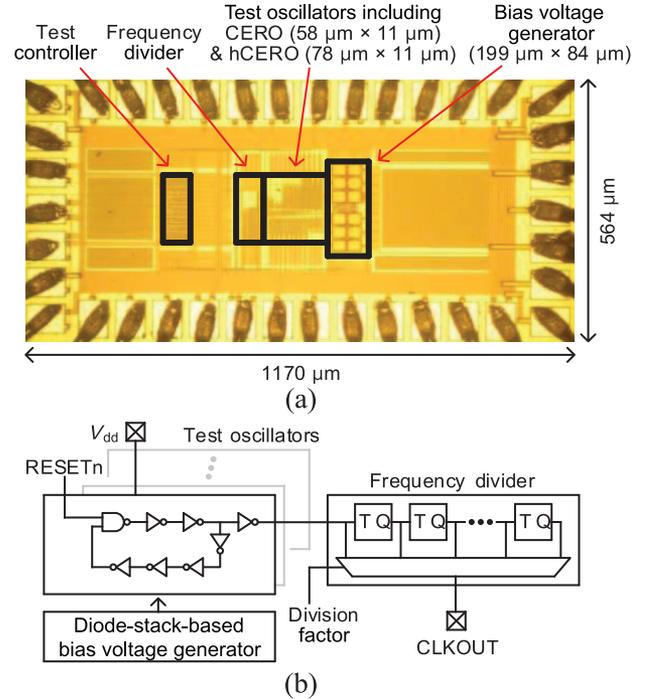


Fig. 18. Test chip for oscillators. (a) Die photograph. (b) Test structure.

transistors in the CERO (M_{CPA} , M_{CPB} , M_{CNA} , and M_{CNB}). The CERO exhibits slightly less frequency variation than the CSRO ($0.72 \times$ at 0.18 V V_{BIASN}), since the differential structure mitigates the impact of the variation. As shown in Fig. 17(b), the CERO has significantly less EpC variation than the CSRO due to the constant EpC across the oscillator frequencies. Fig. 17(c) and (d) shows the distribution of the frequency and EpC at 0.45 V V_{BIASN} as examples.

Compared to the CSRO, the CERO shows a similar sensitivity of the output frequency to temperature, supply voltage, process variation, and device mismatch. The frequency variation can be tolerated by a closed-loop design. For example, as seen in Fig. 1, the output voltage of a switched-capacitor DC–DC converter is compared to the desired reference voltage, and the clock frequency is updated to maintain the proper output voltage [10]. As will be seen later, the closed loop is implemented with off-chip equipment for a prototype switched-capacitor DC–DC converter, and the control bits of the multiplexer in the bias voltage generator are adjusted to find the desired oscillator frequency.

IV. MEASUREMENT RESULTS

Prototype oscillators are fabricated in a 0.18 μm CMOS technology, including a seven-stage conventional CSRO and the proposed ring oscillators (CERO and hCERO) with inverter buffers for comparison (Fig. 18). A diode stack with PMOS transistors and a 64-input analog multiplexer using transmission gates are implemented to provide bias voltages for the oscillators. The oscillator outputs are connected to a frequency divider to allow for direct observation through a pad. The output frequency is manually changed by reconfiguring the control bits of the bias voltage generator shown in Fig. 13.

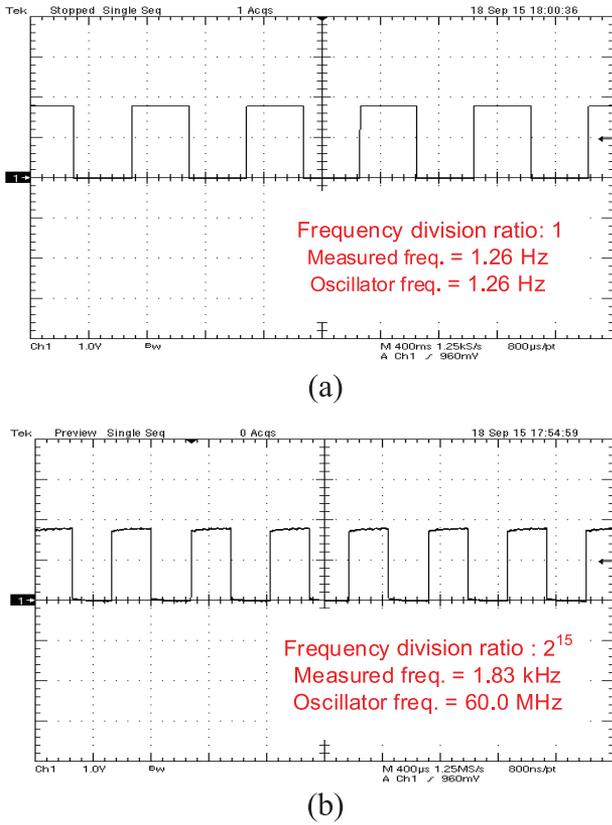


Fig. 19. Measured waveforms from CERO. (a) Slowest output frequency with 0 V V_{BIASN} . (b) Fastest output frequency with 1.8 V V_{BIASN} .

Fig. 19 shows the measured transient waveforms of the CERO. In Fig. 19(a), the minimum output frequency of 1.26 Hz is measured. In Fig. 19(b), the maximum frequency of 1.83 kHz is measured with the frequency divisions of 2^{15} , and the oscillator frequency is 60.0 MHz.

Fig. 20 shows the measured power and EpC of the CSRO and the CERO. In Fig. 20(a), the CERO shows linearly scaled power consumption from 1.2 Hz to 60 MHz ($f_{MAX}/f_{MIN} = 5 \times 10^7$). In contrast, the CSRO power consumption has a floor at 144 nW due to short-circuit current through the buffer. In addition, it cannot effectively scale below 300 kHz, thereby excluding ultra-low frequency applications. This results in a much worse EpC for the CSRO at lower frequencies, as seen in Fig. 20(b). In contrast, the CERO shows a constant EpC of 0.8 pJ/cycle from 21 Hz to 60 MHz, which is enabled by the rapid transition through the voltage region causing short-circuit current. Below 300 kHz, the CERO requires less EpC than the CSRO, since the large short-circuit current through the buffer in the CSRO becomes dominant over dynamic energy. The difference between the simulated EpC (0.3 pJ/cycle, Fig. 16) and measured EpC (0.8 pJ/cycle, Fig. 20) results from the wire and coupling capacitance (91% increase, post-parasitic extraction) and higher I_{LEAK1} or I_{LEAK4} (Fig. 4) in fabricated devices compared with SPICE models.

Fig. 21 shows the measured bias voltage profile of the CERO for a wide frequency generation. Most of the frequency range is covered at bias voltages less than the threshold voltage (~ 0.7 V) of the devices that control charging (or discharging)

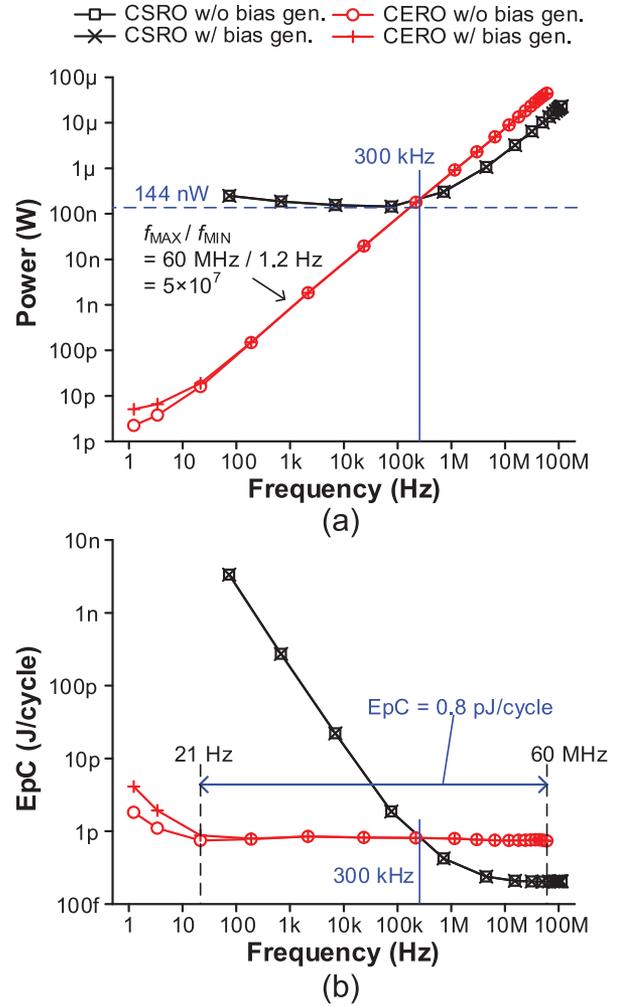


Fig. 20. Measured power and EpC of CSRO and CERO. (a) Power. (b) EpC.

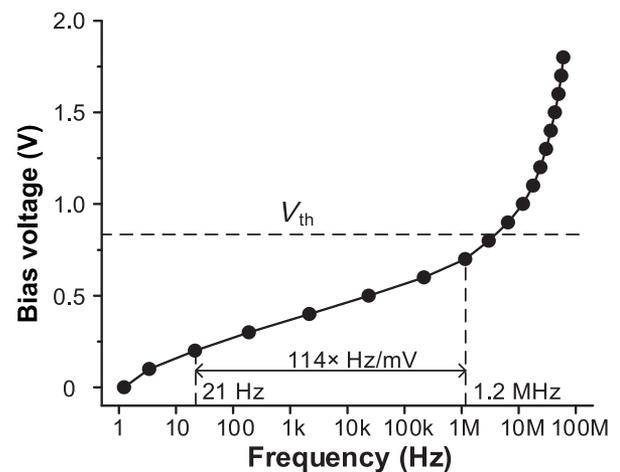


Fig. 21. Measured bias voltage profile of CERO across frequencies.

current. The high drain current sensitivity on gate voltage in the subthreshold region results in $1.14 \times \text{Hz/mV}$ of frequency sensitivity on the gate voltage from 21 Hz to 1.2 MHz. Thus, this range should be well covered with fine steps by the bias voltage generator.

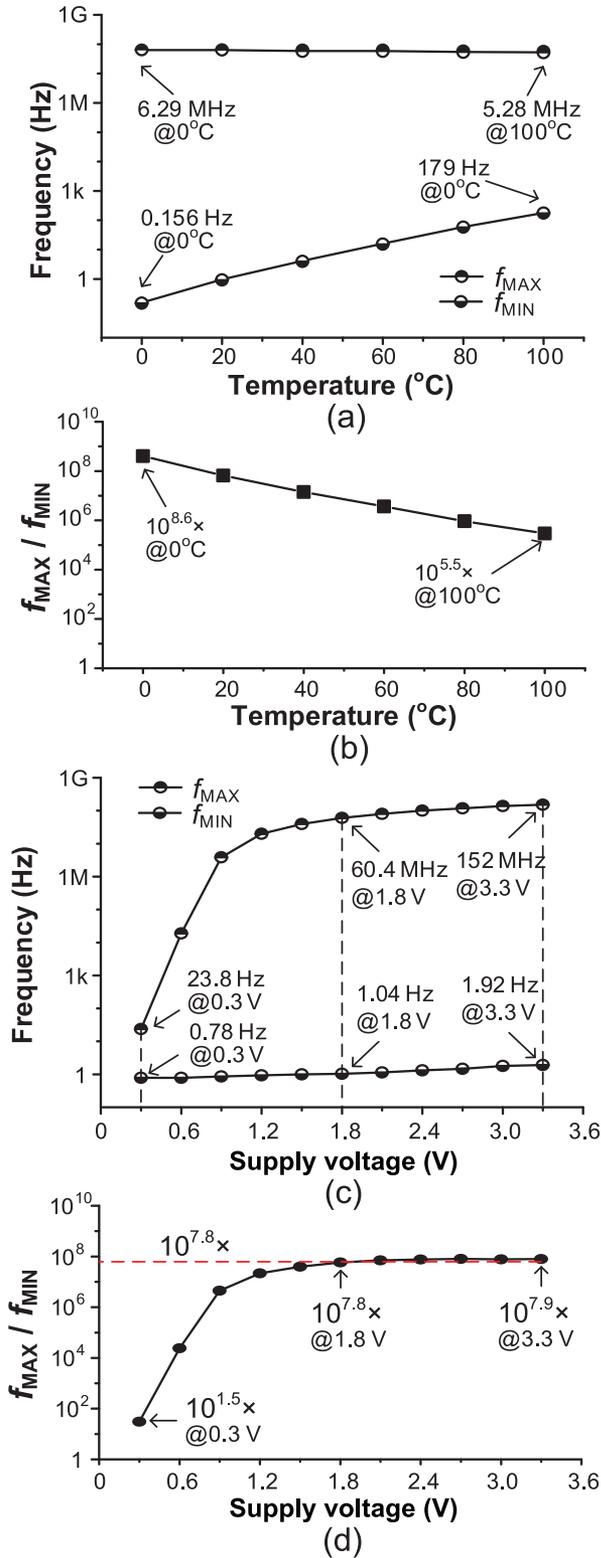


Fig. 22. Measured frequency range of CERO. (a) f_{MAX} and f_{MIN} across temperatures (1.8 V supply voltage). (b) f_{MAX}/f_{MIN} across temperatures. (c) f_{MAX} and f_{MIN} across supply voltages (ambient temperature). (d) f_{MAX}/f_{MIN} across supply voltages.

Fig. 22 shows the measured maximum and minimum oscillator frequencies across temperatures or supply voltages. As shown in Fig. 22(a), the minimum frequency significantly

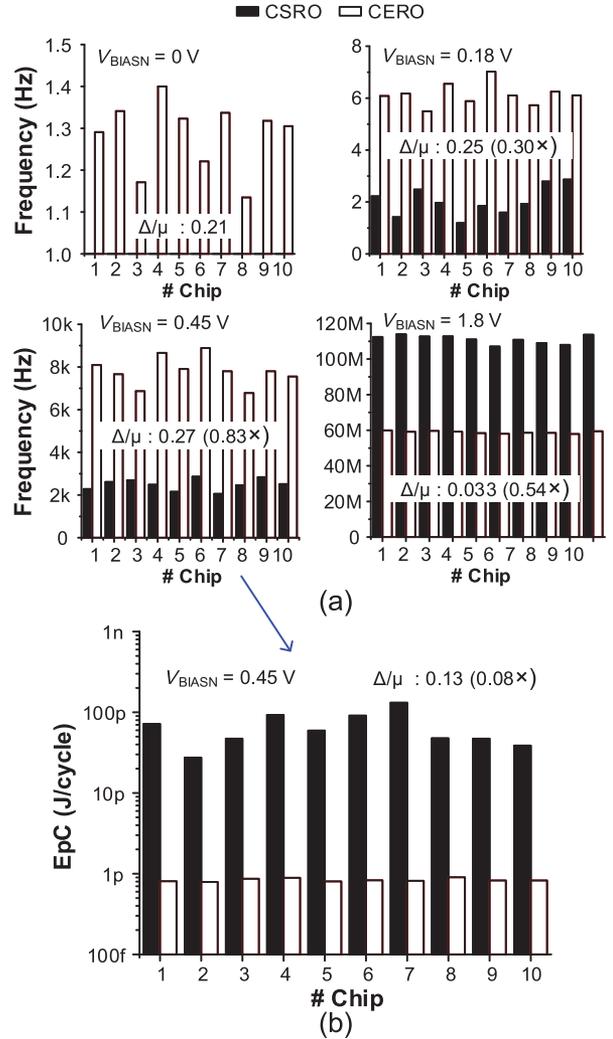
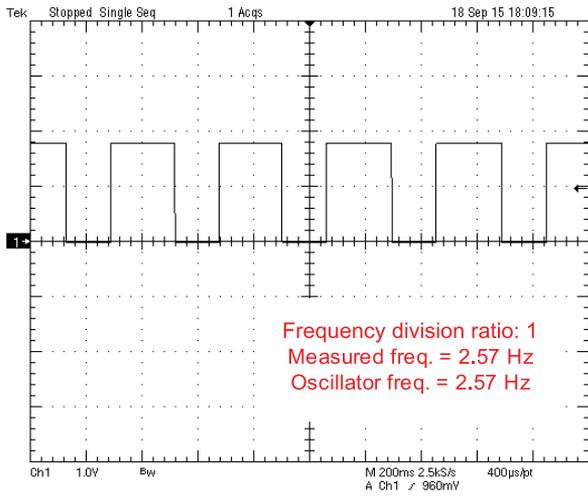


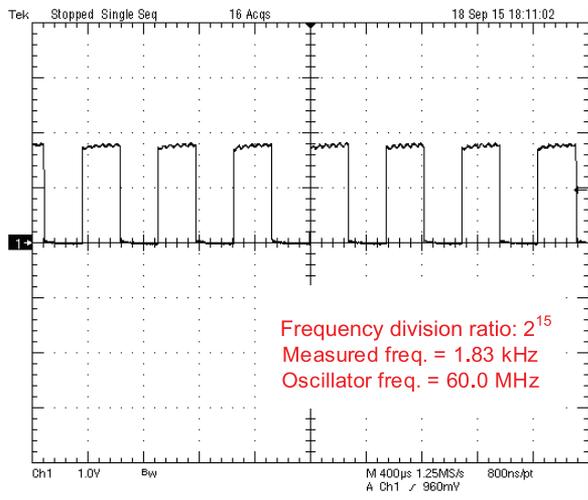
Fig. 23. Measured CSRO and CERO from 10 chips (ambient temperature and 1.8 V supply voltage). (a) Oscillator frequency. (b) EpC [Δ : Max.-Min., (): Δ of CERO/ Δ of CSRO].

changes (1147 \times) over the temperature range due to sub-threshold operation compared with the maximum frequency. This behavior results in a reduction in the frequency range (f_{MAX}/f_{MIN}) at higher temperatures, as shown in Fig. 22(b). In Fig. 22(c), the CERO operates down to 0.3 V, whereas the maximum supply voltage is limited by the process technology. For supply voltages above V_{th} , the maximum frequency becomes less sensitive to changes in the supply voltage, since the transistors begin to work in the strong-inversion region. As shown in Fig. 22(d), the frequency range increases from $10^{1.5}$ to $10^{7.8}$ as the supply voltage increases from 0.3–1.8 V, and it begins to saturate for supply voltages above 1.2 V.

Fig. 23(a) shows the measured oscillator frequencies from 10 different chips. Compared with the CSRO, the CERO has less frequency spread ($< 83\%$). Fig. 23(b) shows the measured spread of EpC at 0.45 V V_{BIASN} . The CERO has only 8% of the EpC spread observed with the CSRO due to the characteristics of a constant EpC as shown in the corner and Monte Carlo simulation results (Figs. 16 and 17).



(a)



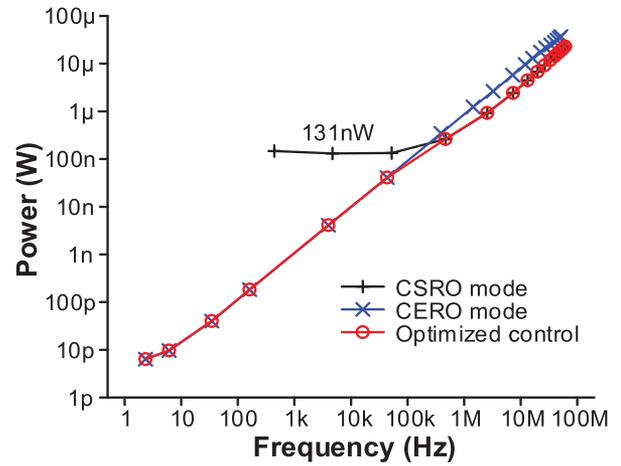
(b)

Fig. 24. Measured waveforms from hCERO. (a) Slowest output frequency with 0 V V_{BIASN} in CERO mode. (b) Fastest output frequency with 1.8 V V_{BIASN} in CSRO mode.

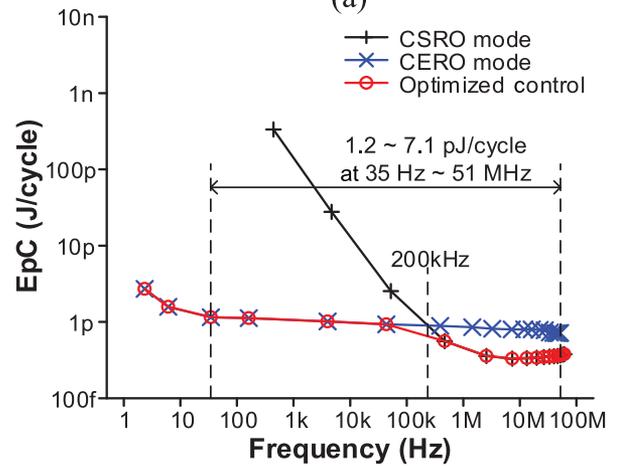
Fig. 24 shows the measured transient waveforms of hCERO. In Fig. 24(a), the minimum output frequency of 2.57 Hz is measured without frequency division in the CERO mode. In Fig. 24(b), the maximum frequency of 1.83 kHz is measured with frequency divisions of 2^{15} in the CSRO mode. Thus, the oscillator frequency is 60.0 MHz.

Fig. 25 shows the measured power and EpC of the hCERO in the two different modes. Similar to the CERO, the hCERO in the CERO mode maintains an EpC of 0.7–1.2 pJ/cycle over the frequency range 35 Hz–51 MHz. Although the power reaches a minimum at 131 nW below 53 kHz, the CSRO mode is more efficient than the CERO mode above 200 kHz. Hence, the hCERO mode switches at 200 kHz to achieve lower EpC values.

Fig. 26 shows the measured EpC of the CSRO, CERO, and optimized hCERO. Below 80 kHz, the hCERO has a higher EpC than the CERO by up to 38% (180 Hz). This finding results from $1.3\times$ increased switching capacitance from additional transistors that control the mode change (Fig. 8). Above



(a)



(b)

Fig. 25. Measured performance of hCERO across frequencies. (a) Power. (b) EpC.

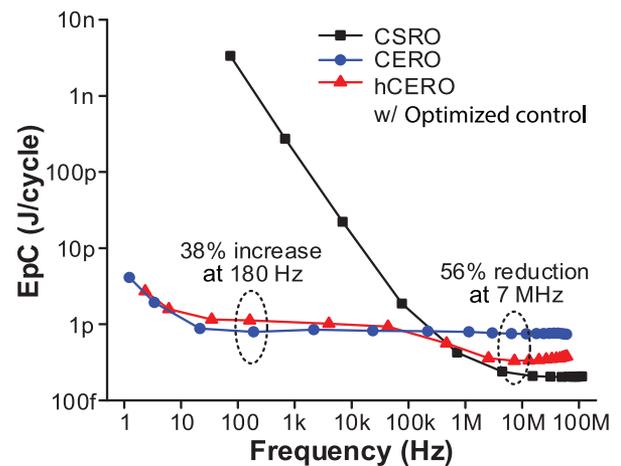


Fig. 26. Measured EpC of CSRO, CERO, and hCERO.

80 kHz, the hCERO uses up to 56% less (7 MHz) EpC than the CERO. This is achieved by disabling half of the circuits in the delay cells, which reduces switching capacitance by $5.8\times$. However, although the hCERO operates in a similar manner as

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO OTHER PRIOR WORKS

	This work		CSRO	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]
	CERO	hCERO									
Process (nm)	180		350	350	180	800	180	600	180	130	
V_{dd} (V)	1.8		3.3	3.3	2	5	3.3	3.0	1.8	1.2	
f_{MAX} (Hz)	60 M	61 M	113 M	256 M	1.1 G	807 M	407 M	368.9 M	366 M	6.9 G	10 M
f_{MIN} (Hz)	1.2	2.3	74	4.8	4 k	20 M	13	40	40	75 M	1.75 k
$\log(f_{MAX} / f_{MIN})$	7.7	7.4	6.2	7.7	5.4	1.6	7.5	7.0	7.0	2.0	3.8
Power @ f_{MAX} (W)	44 μ	23 μ	23 μ	1.76 m	N/A	N/A	29.2 m	30.05 m	70 μ	9.32 m	3.6 μ
Power @ f_{MIN} (W)	5.1 p	6.4 p	247 n	N/A	N/A	N/A	N/A	N/A	70 μ	70 μ	1 n
EpC @ f_{MAX} (J/cycle)	0.73 p	0.38 p	0.20 p	6.88 p	N/A	N/A	71.7 p	81.5 p	0.19 p	1.35 p	0.36 p
EpC @ f_{MIN} (J/cycle)	4.25 p	2.78 p	3.34 n	N/A	N/A	N/A	N/A	N/A	1.75 μ	0.93 p	0.57 p
Comments	Silicon measurement						Spice simulation				

the CSRO, it is slightly less efficient than the CSRO at high frequencies due to the $1.3\times$ capacitance penalty.

Table I shows the performance summary of the proposed oscillators and prior wide range frequency ring oscillators. The CERO, along with [17], shows the widest range of frequency (> 7 orders of magnitude). However, [17] does not report energy/power at the lowest frequency, while the energy at the highest frequency is $2.8\times$ higher than hCERO considering technology scaling such as capacitance and supply voltage ($9.4\times$ without considering technology scaling). Although [23] and [24] show good performance with respect to EpC, their frequency range is not nearly as wide as the CERO or the hCERO, and their oscillators are not verified in silicon. The CERO and the hCERO demonstrate good EpC over a wide frequency range.

V. APPLICATION EXAMPLE

The proposed CERO is implemented to operate a switched-capacitor DC–DC converter fabricated in a $0.18\ \mu\text{m}$ CMOS process, as shown in Fig. 27(a). A 6:1 step-down converter is designed to deliver power from a Li thin-film battery ($\sim 3.8\ \text{V}$) to a digital system such as a processor and a memory ($0.5\text{--}0.6\ \text{V}$) for a low-power WSN.

Fig. 27(b) shows the converter block diagram including the CERO. In the tradeoff between converter switching power and the drive strength of transistors, the gate-driving voltage is set to one-third of the input voltage (V_{IN}). The converter switch drivers and the CERO operate under the same supply voltage, which is one tap of the converter (one-third V_{IN}). Thus, the converter can operate by itself after it starts delivering power with the help of a startup oscillator that runs directly from the battery.

Fig. 28 shows the measured waveforms of the oscillator and DC–DC converter. In Fig. 28(a), $50\ \text{nA}$ is loaded at the output of the DC–DC converter as default due to the input impedance

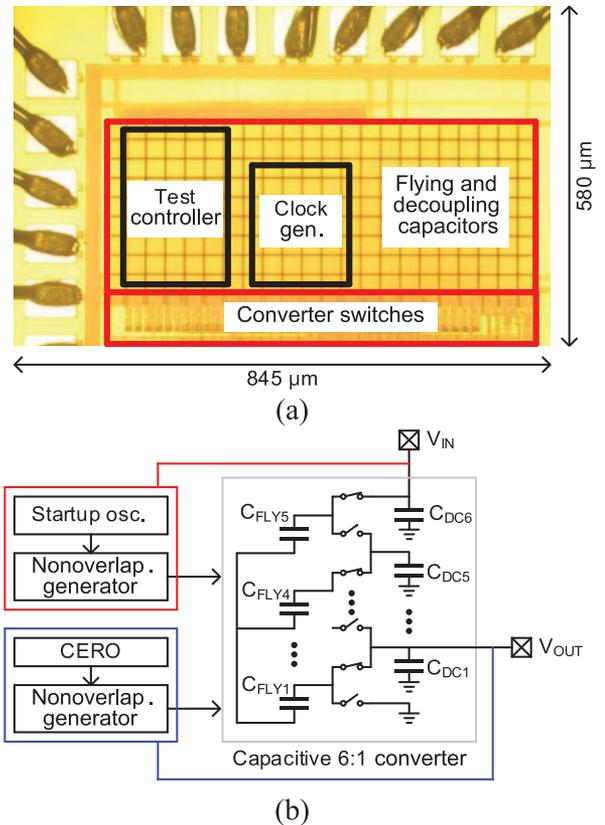
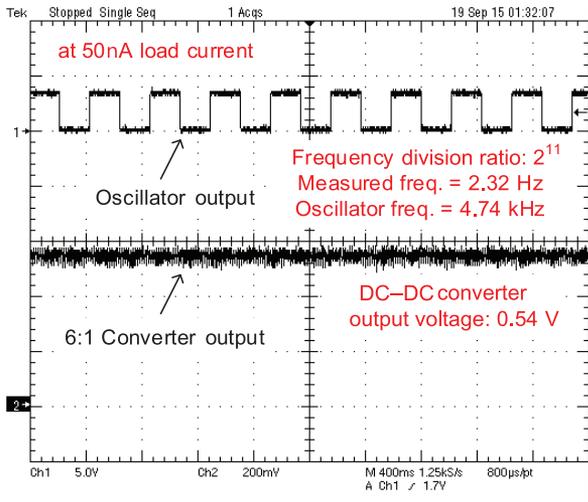


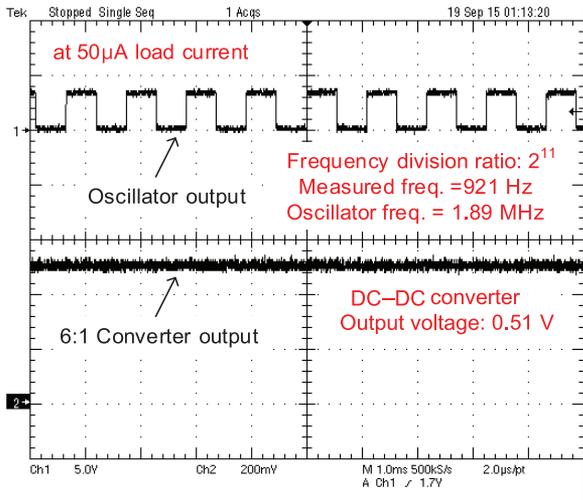
Fig. 27. Test chip for a capacitive step-down converter. (a) Die photograph. (b) Converter diagram.

of the oscilloscope ($\sim 10\ \text{M}\Omega$). In Fig. 28(b), $50\ \mu\text{A}$ is pulled down from the output by an off-chip resistor ($\sim 10\ \text{k}\Omega$). The input voltage is $3.8\ \text{V}$.

Fig. 29 shows the measured input power, converter efficiency, and clock frequency across load powers. The output voltage is



(a)

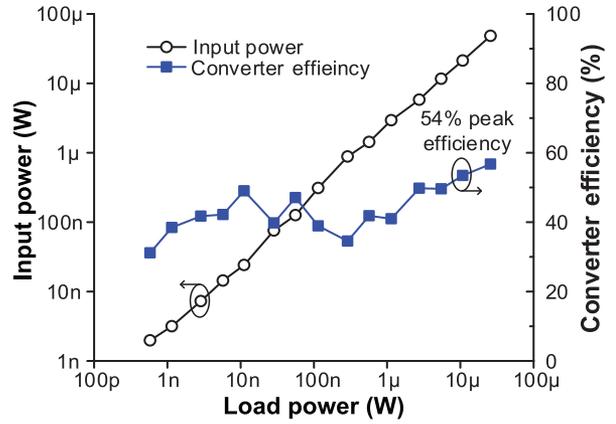


(b)

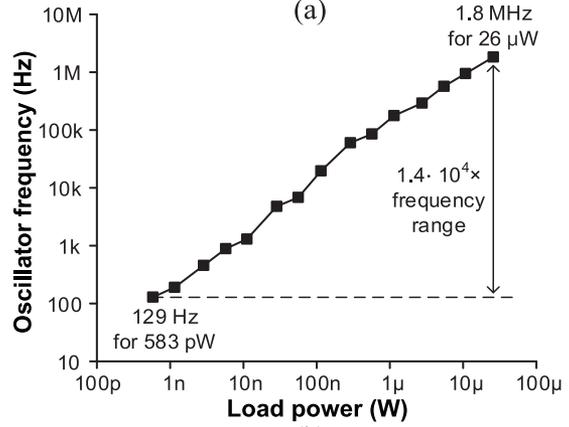
Fig. 28. Measured waveforms from oscillator and DC-DC converter. (a) 50 nA load current. (b) 50 μ A load current.

monitored by a voltage meter (Keithley 2400), and LABVIEW automatically lowers the oscillator frequency by changing the control bits of the bias voltage generator until the output voltage decreases below 80% (0.5 V) of the zero-load output voltage. The converter can support a wide load power range from 583 pW to 26 μ W and achieves a peak converter efficiency of 54%. As the load power decreases, the converter transfers less charge through the switched capacitor network. Hence, the switching speed can be slower, leading to lower input power with less switching and oscillator power. However, this is only true when the oscillator power scales with the frequency.

Fig. 30 shows the converter efficiency using either the CSRO or the CERO. The efficiency of the converter using the CSRO is calculated based on the oscillator measurement. Below 5.7 nW load power, the converter with the CERO is more efficient than the CSRO-based converter due to the power scalability of the CERO. The CERO-based converter efficiency is improved by 11%–56% for 583 pW–2.9 nW load power compared with that of the CSRO-based converter.



(a)



(b)

Fig. 29. Measured converter across load powers. (a) Input power and converter efficiency. (b) Operating frequency.

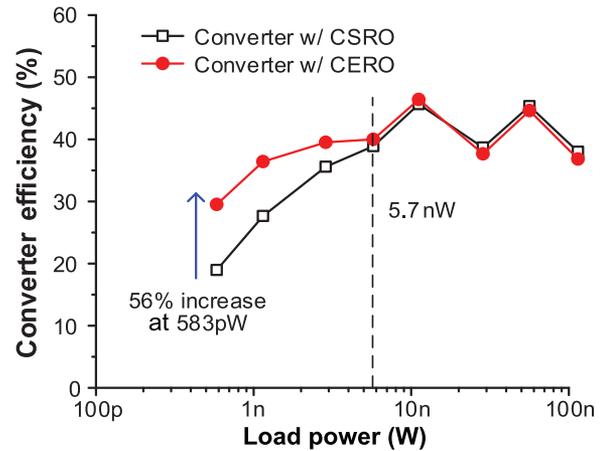


Fig. 30. Efficiency of converters using CSRO and CERO.

VI. CONCLUSION

This work demonstrates an energy-efficient oscillator for WSN applications. In a prototype chip, the proposed CERO achieves a constant 0.8 pJ/cycle over a 21 Hz–60 MHz frequency range at a supply voltage of 1.8 V. Below 300 kHz,

the CERO offers better energy efficiency than a conventional CSRO. This improved energy efficiency is enabled by the rapid transition through the voltage region between V_{thn} and $[V_{dd} - |V_{thp}|]$ and the resulting substantial reduction in short-circuit current. The current-feeding scheme with gate voltage control offers a wide frequency range of 1.2 Hz–60 MHz. In addition, an extension to the CERO is proposed using a hybrid scheme (hCERO) to achieve improved energy efficiency at high frequencies with some costs in additional complexity and area.

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