

Edge-Pursuit Comparator: An Energy-Scalable Oscillator Collapse-Based Comparator With Application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC

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Abstract—This paper presents a new energy-efficient ring oscillator collapse-based comparator, named edge-pursuit comparator (EPC). This comparator automatically adjusts the performance by changing the comparison energy according to its input difference without any control, eliminating unnecessary energy spent on coarse comparisons. Furthermore, a detailed analysis of the EPC in the phase domain shows improved energy efficiency over conventional comparators even without energy scaling, and wider resolution tuning capability with small load capacitance and area. The EPC is used in a successive-approximation-register analog-to-digital converter (SAR ADC) design, which supplements a 10 b differential coarse capacitive digital-to-analog converter (CDAC) with a 5 b common-mode CDAC. This offers an additional 5 b of resolution with common mode to differential gain tuning that improves linearity by reducing the effect of switch parasitic capacitance. A test chip fabricated in 40 nm CMOS shows 74.12 dB signal-to-noise and distortion ratio and 173.4 dB Schreier Figure-of-Merit. With the full ADC consuming 1.17 μ W, the comparator consumes 104 nW, which is only 8.9% of the full ADC power, proving the comparator's energy efficiency.

Index Terms—Common-mode CDAC, edge-pursuit comparator (EPC), high-resolution ADC, noise analysis, oscillator collapse, phase domain, SAR ADC.

I. INTRODUCTION

COMPARATORS are widely used in many applications such as voltage regulation, brown-out detection, and analog-to-digital conversion. In some of these applications, the performance of the entire circuit directly relies on the

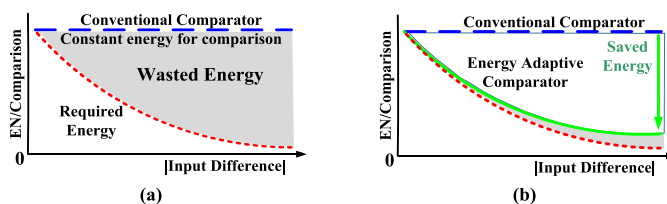


Fig. 1. Required energy for comparison versus input difference. (a) Conventional comparators wasting most energy for large input difference. (b) Energy scaling saved wasted energy for comparison.

comparator's performance as the comparator plays a key role. A high-resolution successive-approximation-register (SAR) analog-to-digital converter (ADC) is a good example, which needs an especially low-noise comparison to distinguish voltages that are very close for fine bit decisions requiring a large amount of energy that takes a significant portion of the total conversion energy. However, as depicted in Fig. 1(a), while the actual energy requirement sharply decreases as the input signal difference becomes larger, conventional clocked comparators [1]–[3] usually consume nearly constant energy for each comparison since they are designed according to the most accurate and power-hungry comparison. Therefore, in these kinds of applications, adjusting the energy for comparison according to the input difference level can greatly help in reducing the total comparison energy [Fig. 1(b)] as well as the overall energy consumption. For this reason, some prior works on SAR ADCs have presented techniques for comparator energy scaling [4]–[10], including dual ADC architectures that use two comparators for coarse and fine comparisons [4], [5], multiple repetitive comparisons for noise-critical bits [5]–[7], and time-domain comparators whose noise level can be modulated by changing the length of the delay lines [8]. However, these structures reduce the simplicity of the SAR structure by introducing overheads for extra control, increasing design and control complexity. They also have a limited number of energy scaling steps and a limited noise tuning range, making it difficult to benefit much from comparator energy scaling. In addition, some prior techniques require preprogrammed scaling by prediction, introducing additional inefficiencies from prediction misses.

This paper presents a ring oscillator collapse-based comparator, referred to as an *edge-pursuit comparator* (EPC).

Manuscript received August 14, 2016; revised October 8, 2016; accepted November 10, 2016. Date of publication January 16, 2017; date of current version March 23, 2017. This work was supported by the TSMC University Shuttle Program for chip fabrication and Analog Devices. This paper was approved by Guest Editor Brian Ginsburg.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2631299

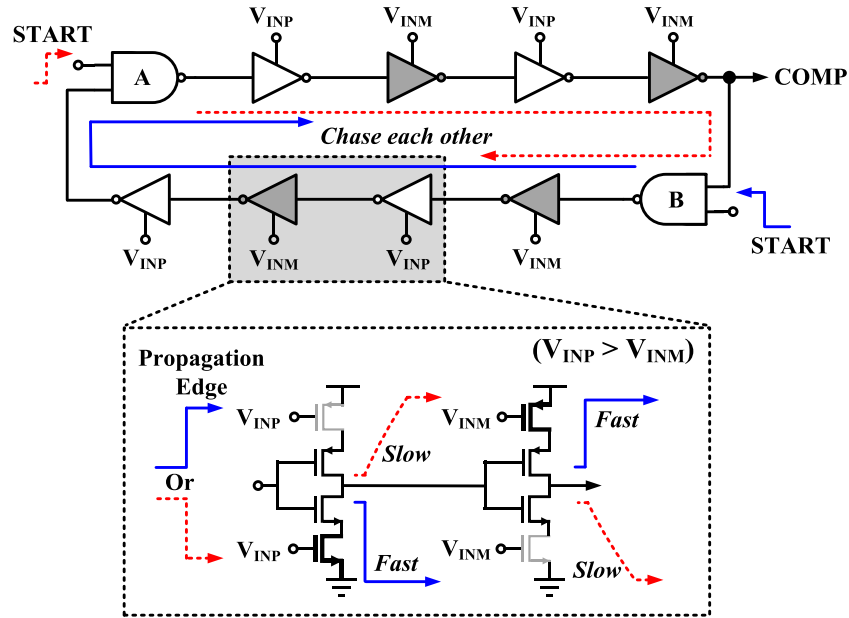


Fig. 2. Structure of the EPC.

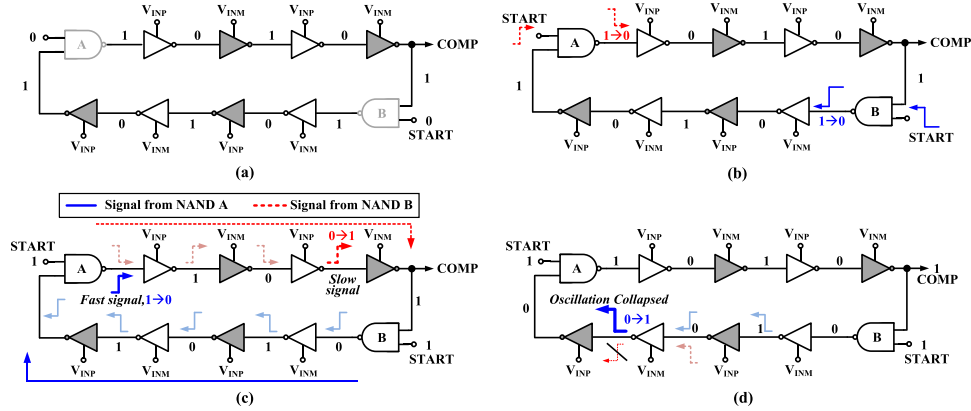


Fig. 3. Operation of the EPC. (a) Reset state. (b) Comparison start. (c) Edge propagation. (d) Comparison end.

The EPC automatically scales comparison energy according to its input difference without external control, tailoring comparison energy to each conversion. Wide-range energy scaling allows for saving a significant amount of energy for coarse comparisons. Phase-domain operation running for many cycles over the ring oscillator enables high-resolution operation with a small load capacitance and area.

Section II presents the structure of the EPC and describes its operation. Section III analyzes the operation of the EPC in detail with noise, deriving equations on expected performance and energy efficiency. In Section IV, some important characteristics of the EPC are discussed and its energy efficiency is compared with conventional comparators. Section V presents an application of the EPC to a 15 b SAR ADC with dual capacitive digital-to-analog converter (CDAC) structure. Section VI presents the measured results, and Section VII concludes this paper.

II. STRUCTURE AND OPERATION OF THE EDGE-PURSUIT COMPARATOR

Fig. 2 shows the structure of the EPC [9], which is composed of two NAND gates and inverter delay cells. The design

is inspired by a physically unclonable function circuit that uses oscillator collapse to uniquely identify integrated circuits [11]. Here, the design is modified to serve as a comparator with differential inputs; the topology is shown below to be particularly well suited for use as a comparator. Initially, the comparator is in the reset state as the signal *START* is low to disconnect the oscillation path, as shown in Fig. 3(a). The comparator initiates a comparison when the signal *START* goes high simultaneously at both NAND gates [Fig. 3(b)]. This injects two propagating edges into the oscillator, which travel around the comparator [Fig. 3(c)] until one overtakes the other, collapsing the oscillation [Fig. 3(d)]. Differential input signals (V_{INP} and V_{INM}) are alternatively applied to both the top and bottom current-limiting transistors of the delay cells, modulating the pull-up and pull-down edge-propagation delays. The propagation delay of these two edges is controlled by mutually exclusive current-limiting transistors such that increasing V_{INP} causes one edge to propagate faster and the other to become slower (and vice versa for V_{INM}). After one propagating edge overtakes the other edge, the oscillation collapses and the stage outputs settle to either V_{DD} or GND , dictated by which edge was slower and hence overtaken [Fig. 4(a)]. The

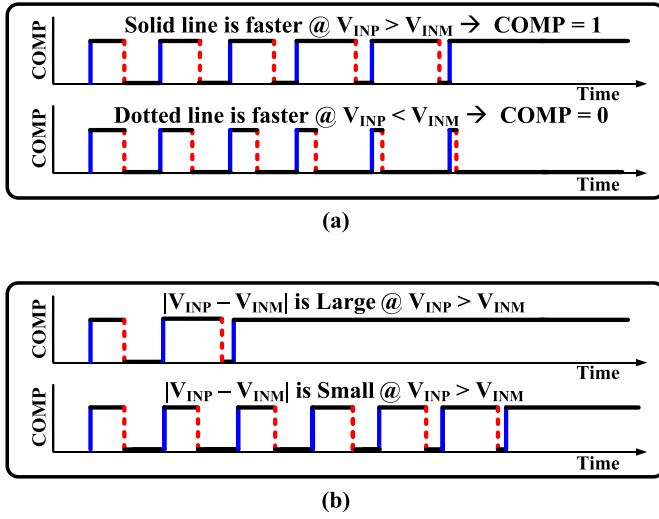


Fig. 4. Output of the EPC versus time during comparison. Output waveform changes according to (a) polarity of the $|V_{INP} - V_{INM}|$ and (b) amount of the input signal difference.

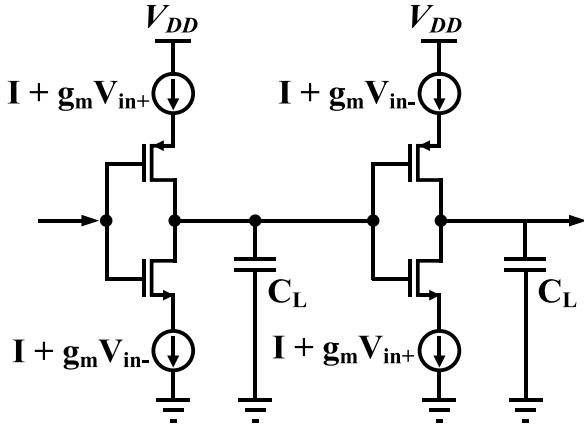


Fig. 5. Simplified delay cell model for noise estimation.

comparator output $COMP$ is sampled from an internal stage that goes high when $V_{INP} > V_{INM}$ and low otherwise. When the voltage difference between V_{INM} and V_{INP} is small, the two injected edges have similar propagation delays and the number of cycles required to make a decision automatically increases [Fig. 4(b)]. This filters out high-frequency noise, as the design performs noise averaging over a longer period of time. On the other hand, for large voltage differences, the oscillation inherently collapses quickly, limiting dynamic energy consumption for coarse comparisons. In this manner, the comparator naturally adjusts its energy dissipation without external control, and realizes both high accuracy and low power operation.

III. ANALYSIS OF EDGE-PURSUIT COMPARATOR PERFORMANCE

During a comparison, the EPC operates similarly to a ring oscillator. After it is triggered, two injected edges propagate with different speeds driven by different transistors, whose phase difference drifts until it shifts by $-\pi$ or π compared

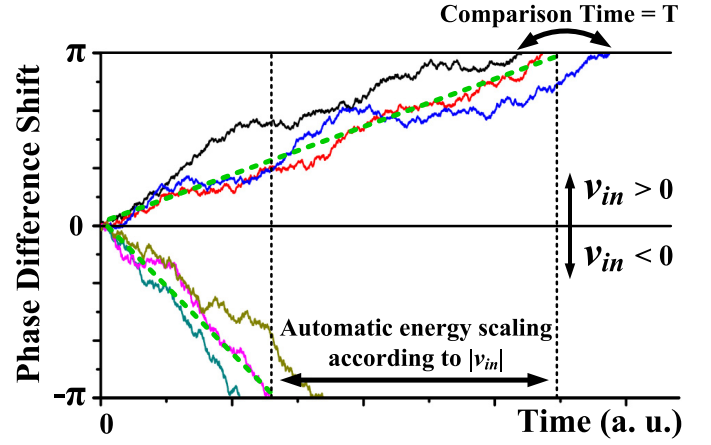


Fig. 6. Operation of EPC in phase domain.

with when the propagation started. Therefore, comparator noise can be estimated by analyzing the phase difference in the time or phase domain instead of voltage or current. To simplify the noise analysis, we reduce the circuit to be analyzed to the one shown in Fig. 5. The NAND gates with the comparator clock are skipped as their propagation delay and jitter noise are much smaller than the other stages. Each current-limiting transistor is modeled as a noisy current source. Assuming that the parasitic device capacitances are much smaller than the stage load capacitance C_L , the noise from transistors in the middle of the stack can be neglected, allowing these transistors to be modeled as simple noiseless switches that flip at $\sim V_{DD}/2$.

A. Operational Analysis in Phase Domain

We analyze the EPC behavior in the phase domain, with the basic concept illustrated in Fig. 6. According to Abidi's analysis of ring oscillator noise in [12], the comparator period jitter variance is

$$\sigma_{\tau}^2 = \frac{kT}{If_0} \left(\frac{2}{V_{ov}} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right) \quad (1)$$

where τ is the oscillation period, σ_{τ}^2 is the variance of the period jitter, f_0 is the oscillation frequency, and V_{ov} is the overdrive voltage of the current-limiting transistors. Assuming that the period jitter is uncorrelated between the two propagating edges, the variance of the phase difference shift at a period is

$$\sigma_{\Delta\phi}^2 \cong 2 \times (2\pi)^2 \frac{\sigma_{\tau}^2}{\tau^2} = 8\pi^2 f_0 \frac{kT}{I} \left(\frac{2}{V_{ov}} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right). \quad (2)$$

In addition to noise, the phase difference shifts as the input voltage difference gives rise to a current difference for the two propagating edges. The average period difference between the two edges $\Delta\tau$ is

$$\Delta\tau \cong \frac{\Delta I}{I} \tau = v_{in} \frac{g_m}{If_0} = \frac{v_{in}}{V_{ov}} \frac{2}{f_0} \quad (3)$$

where v_{in} is the input differential voltage and g_m is the transconductance of the current-limiting transistors.

Therefore, the average phase difference shift at a period $\mu_{\Delta\phi}$ is

$$\mu_{\Delta\phi} \cong 2\pi \times \frac{\Delta\tau}{\tau} = 4\pi \frac{v_{in}}{V_{ov}}. \quad (4)$$

Note that in this convention, a positive v_{in} causes the phase difference to drift toward the boundary at π . Therefore, an oscillation finishing with the phase difference at π means that the comparison result is “high,” and otherwise (finishing at $-\pi$) means “low.”

For easier formulation of the phase shift during a comparison, we assume that the phase difference shift $\Phi(t)$ is a continuous-time random process with independent increments in nonoverlapping time intervals, similar to 1-D Brownian motion with drift. Then, the probability density function of $\phi(t)$

$$f(t, \phi) \equiv f_{\Phi(t)}(\phi), \quad t \geq 0, \quad -\pi \leq \phi \leq \pi \quad (5)$$

satisfies the Fokker–Planck equation [13]

$$\partial_t f(t, \phi) = -M \partial_\phi f(t, \phi) + \frac{\Sigma}{2} \partial_\phi^2 f(t, \phi) \quad (6)$$

where M and Σ are the “drift” and “diffusion” coefficients of this random process, defined as

$$M \equiv \frac{\mu_{\Delta\phi}}{\tau} = 4\pi f_0 \frac{v_{in}}{V_{ov}} \quad (7)$$

$$\Sigma \equiv \frac{\sigma_{\Delta\phi}^2}{\tau} = 8\pi^2 f_0^2 \frac{kT}{I} \left(\frac{2}{V_{ov}} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right). \quad (8)$$

From the initial condition of the comparator, this system has a boundary condition

$$f(0, \phi) = \delta(\phi). \quad (9)$$

In addition, another boundary condition at the phase shift boundaries is given by

$$f(t, \pi) = f(t, -\pi) = 0 \quad (10)$$

because a trial of this process is excluded from the probability density once its value reaches a boundary.

The solution of this system is

$$f(t, \phi) = \frac{1}{\pi} e^{\frac{M}{\Sigma} \phi} \sum_{n=1}^{\infty} e^{-\lambda(n)t} \cos(k(n)\phi) \quad (11)$$

where the coefficients $k(n)$ and $\lambda(n)$ are defined as

$$k(n) = n - \frac{1}{2}, \quad n \in N \quad (12)$$

$$\lambda(n) = \frac{M^2}{2\Sigma} + \frac{\Sigma}{2} \times k(n)^2. \quad (13)$$

B. Comparison Time and Energy

Let T be a random variable for the comparison time and $f(t)$ be a function representing the probability of the comparator oscillating at time t . $f(t)$ is derived by integrating $f(t, \phi)$ in (11) along the ϕ -axis

$$\begin{aligned} f(t) &\equiv P[T > t] = P[-\pi < f_{\Phi(t)}(\phi) < \pi] \\ &= \int_{-\pi}^{\pi} f(t, \phi) d\phi = \frac{1}{\pi} \Sigma \cos h \left(\frac{M}{\Sigma} \pi \right) \\ &\quad \times \sum_{n=1}^{\infty} (-1)^{n+1} \frac{k(n)}{\lambda(n)} e^{-\lambda(n)t}. \end{aligned} \quad (14)$$

By differentiating this with respect to t , we obtain the probability density function of T , $f_T(t)$, as

$$\begin{aligned} f_T(t) &= \frac{d}{dt} P[T \leq t] = -f'(t) = \frac{1}{\pi} \Sigma \cos h \left(\frac{M}{\Sigma} \pi \right) \\ &\quad \times \sum_{n=1}^{\infty} (-1)^{n+1} k(n) e^{-\lambda(n)t}. \end{aligned} \quad (15)$$

The average comparison time $E[T]$ is

$$E[T] = \int_0^{\infty} t f_T(t) dt = \frac{\pi \tanh \left(\frac{M}{\Sigma} \pi \right)}{M} = \frac{\pi^2}{\Sigma} S \left(\frac{M}{\Sigma} \right) \quad (16)$$

where the scaling factor S , which is dependent on the ratio M/Σ , is defined as

$$S(k) \equiv \frac{\tanh h(k\pi)}{k\pi}. \quad (17)$$

The function $S(k)$ is an even function with its maximum at $(0, 1)$. Its value decreases as $|k|$ becomes larger, characterizing the automatic energy scaling behavior of this comparator. When $M = 0$, i.e., $v_{in} = 0$, the average comparison time peaks at π^2/Σ .

The energy for a comparison is easily calculated from the comparison time. Because each edge draws current I from the supply voltage V_{DD} on average as it propagates, the comparator consumes an average power of

$$P = 2IV_{DD}. \quad (18)$$

Therefore, the average energy consumption per comparison is

$$E = P \times E[T] = 2IV_{DD} \frac{\pi^2}{\Sigma} S \left(\frac{M}{\Sigma} \right). \quad (19)$$

C. Input Referred Noise

Let $g(t, \phi)$ be a function on the region $t \geq 0$, $-\pi \leq \phi \leq \pi$ whose value represents the probability for the comparator to finish its oscillation with a final phase difference shift of π , meaning output “high,” when the current phase difference shift is ϕ at time t . By this definition, the value of this function must be independent of time t , because its dynamic behavior is determined only by the stationary random variable $\Delta\Phi(\Delta t)$ and current phase difference ϕ . Then, $g(t, \phi) = g(\phi)$ satisfies the differential equation

$$Ag'(\phi) + \frac{B}{2} g''(\phi) = 0. \quad (20)$$

Solving (20) with two boundary conditions

$$g(\pi) = 1, \quad g(-\pi) = 0 \quad (21)$$

that are clearly given by the earlier definition of g , we obtain

$$g(\phi) = \frac{e^{\frac{2M}{\Sigma}\pi} - e^{\frac{-2M}{\Sigma}\phi}}{e^{\frac{2M}{\Sigma}\pi} - e^{\frac{-2M}{\Sigma}\pi}}. \quad (22)$$

Let $h(v_{in}) \equiv g(0)$ be a function representing the probability of the comparison result being “high” when the input voltage is v_{in} . This function changes its value according to v_{in} as M

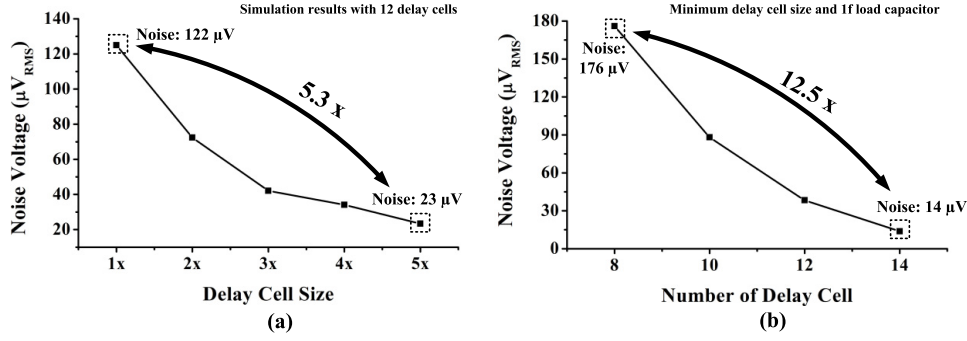


Fig. 7. Simulated input-referred noise versus (a) delay cell size and (b) number of delay cells.

depends on v_{in}

$$h(v_{in}) \equiv g(0)|_{v_{in}} = \frac{e^{\frac{2A(v_{in})}{B}\pi} - 1}{e^{\frac{2A(v_{in})}{B}\pi} - e^{-\frac{2A(v_{in})}{B}\pi}}. \quad (23)$$

The comparator's input-referred noise voltage v_n is a random variable with a probability density function $f_{v_n}(v)$ that satisfies

$$h(v_{in}) = \int_{-\infty}^{\infty} H(v_{in} + v_n) f_{v_n}(v_n) dv_n = \int_{-v_{in}}^{\infty} f_{v_n}(v_n) dv_n \quad (24)$$

where $H(v_{in})$ is the Heaviside step function that models probability of the ideal noiseless comparator output, and therefore

$$f_{v_n}(v_n) = h'(-v_n) = h'(v_n) \quad (25)$$

because h' is an even function.

Then, the comparator's input-referred noise power $\sigma_{v_n}^2$ is obtained as

$$\begin{aligned} \sigma_{v_n}^2 &= \int_{-\infty}^{\infty} v_n^2 f_{v_n}(v_n) dv_n = \int_{-\infty}^{\infty} v_n^2 h'(v_n) dv_n \\ &= \frac{\pi^2}{3} f_0^2 \left(\frac{kT}{I} \right)^2 \left(\frac{2}{V_{ov}} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right)^2 V_{ov}^2. \end{aligned} \quad (26)$$

IV. DISCUSSION ON CHARACTERISTICS OF EDGE-PURSUIT COMPARATOR

The analysis in Section III reveals some useful characteristics of the EPC compared with conventional comparators, which are discussed in this section. In addition, to evaluate the energy efficiency of the EPC and compare it with conventional clocked comparator topologies [1]–[3], energy efficiency norm values are estimated for EPC and conventional comparators and compared with each other.

A. Input Noise Tunability

From (26), the noise rms level σ_{v_n} is

$$\sigma_{v_n} = \sqrt{\sigma_{v_n}^2} = \frac{\pi}{\sqrt{3}} f_0 \frac{kT}{I} \left(\frac{2}{V_{ov}} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right) V_{ov}. \quad (27)$$

Note that the rms level of the comparator's input-referred noise is proportional to f_0/I , which is inversely proportional to the total capacitor size throughout the oscillator. Using this characteristic, one can easily tune the required input-referred noise level across a wide range for this comparator topology

during both design time and runtime. On the other hand, other comparators usually require the tuning of design factors inversely proportional to the required noise power, rather than the rms level, which renders wide-range noise tuning more difficult. Fig. 7(a) shows an example of changing the total capacitance by changing the size of each inverter cell, and as expected, the noise rms level roughly follows the inverse of the total capacitance.

Another example in Fig. 7(b) tries to change the total capacitance by changing the number of delay cells in the comparator. However, the simulated results show that the noise changes more sensitively than expected, which is due to positive feedback on the phase difference shift. The phase difference shift changes the time that each stage output stays at 0 and V_{DD} , during which the internal nodes of each delay cell are reset. If this time for reset becomes too short, the nodes in the delay cell cannot be completely reset, accelerating the phase difference shift in the present direction. As shown in the graph, this positive feedback more affects the comparator with a small number of stages because the time for reset is shorter. This mechanism is similar to the regeneration of the output signal in conventional regenerative comparators, but this phase regeneration does not consume much energy, whereas voltage regeneration in conventional comparators consumes a fixed amount of dynamic energy. For this reason, the energy efficiency of the EPC is maintained even for designs with a small number of stages. This positive feedback mechanism further increases the tunable noise range, showing a 12.5x noise level change only by changing the number of stages from 8 to 14, while conventional comparators require more than 100x design parameter tuning for a similar noise level change.

B. Automatic Energy Scaling

According to (19), the EPC's energy consumption depends on the energy scaling factor $S(M/\Sigma)$. To estimate how much energy is actually saved in usual applications, we obtain the relationship between M/Σ and v_{in} from (7) and (27)

$$\frac{M}{\Sigma} = \frac{1}{\sqrt{12}} \frac{v_{in}}{\sigma_{v_n}}. \quad (28)$$

Taking this equation together with the graph of the scaling factor S in Fig. 8 into account, the energy scaling factor remains around 1 when v_{in} is within the noisy region, but if v_{in} goes outside the noisy region, it decreases fast toward 0 in a

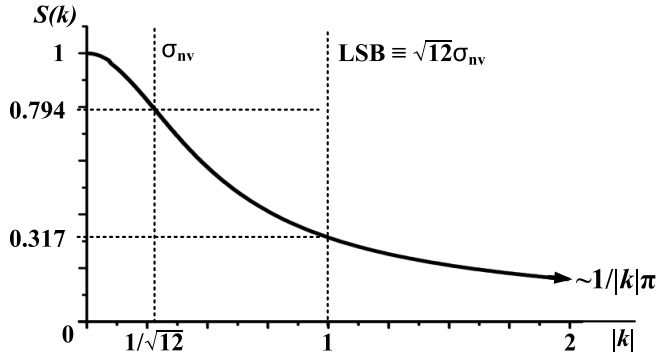
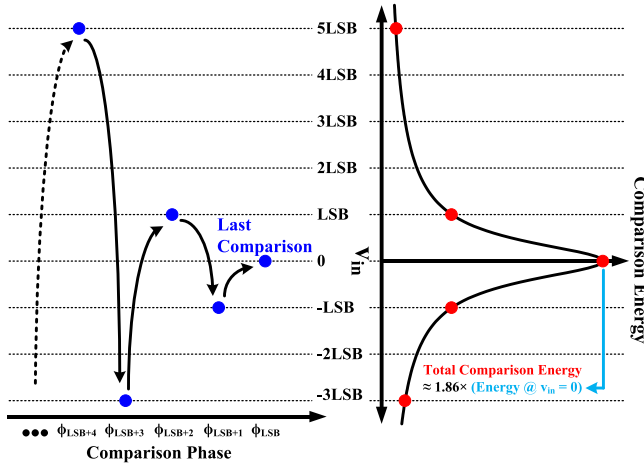
Fig. 8. EPC's scaling factor $S(k)$.

Fig. 9. Comparisons during SAR ADC conversion in the energy worst case.

hyperbolic manner. Therefore, the comparator can save almost all its energy in most voltage ranges, except for a small noisy region that is usually within the μVs – mVs range.

For example, assuming an application of the EPC in a SAR ADC where the comparator is designed to have the same noise level as the quantization noise, a comparison with $v_{in} = \text{LSB} = \sqrt{12}\sigma_{nv}$ consumes only ~ 0.317 times the energy of the comparison with $v_{in} = 0$. Even assuming the worst case of consuming the maximum comparison energy, where the comparison occurs alternately below and above 0 to finally finish with the comparison exactly at $v_{in} = 0$ as shown in Fig. 9, the calculated total energy for all comparisons ($v_{in} = (0\text{LSB}, -1\text{LSB}, +1\text{LSB}, -3\text{LSB}, +5\text{LSB} \dots)$) during a single ADC conversion is only ~ 1.86 times the energy of a single comparison with $v_{in} = 0$.

C. Energy Versus Noise Efficiency

To evaluate the EPC's energy efficiency and compare it with other comparators, we shall define a norm for comparison

$$N \equiv E \times \frac{\sigma_{v_n}^2}{V_{DD}^2} \quad (29)$$

which means the energy consumption per SNR assuming maximum signal power is V_{DD}^2 . From (8), (19), and (26), we

get the norm value for the EPC

$$N_{\text{EPC}} = \frac{\pi^2}{6} S \left(\frac{M}{\Sigma} \right) kT \frac{(V_{DD}(\gamma_N + \gamma_P) + V_{ov})V_{ov}}{V_{DD}^2}. \quad (30)$$

Assuming $\gamma_N = \gamma_P = \gamma$ and $V_{DD}(\gamma_N + \gamma_P) \gg V_{ov}$, (30) simplifies to

$$N_{\text{EPC}} \cong \frac{\pi^2}{3} S \left(\frac{M}{\Sigma} \right) kT \gamma \frac{V_{ov}}{V_{DD}} \quad (31)$$

which has the dimension of energy in the form of kT multiplied by some design factors.

From Nuzzo's analysis [14] on a single-stage regenerated comparator [2] illustrated in Fig. 10(a), its input-referred voltage noise power $\sigma_{v_n}^2$ is derived as

$$\sigma_{v_n}^2 = \sigma_{M_1}^2 + \sigma_{S_1}^2 + \sigma_{M_{3-5}}^2 + \sigma_{S_3}^2. \quad (32)$$

Assuming that the comparator's noise is optimized enough so that $\sigma_{M_1}^2$ becomes dominant, (32) is simplified to

$$\sigma_{v_n \text{ SS}}^2 \cong \sigma_{M_1}^2 = \frac{2kT\gamma}{C_X} \frac{V_{ov}}{V_{th}} \quad (33)$$

where V_{th} and V_{ov} are V_{Tn3} and $V_{ov1,1}$ in the original equation in [14], which means the threshold voltage of M_3 and overdrive voltage of M_1 during comparison phase 1 defined in [14], respectively.

During a comparison, this comparator discharges X_1 and X_2 from V_{DD} to 0. Either node between the two output nodes is also fully discharged. The other output node is discharged down to around half of V_{DD} where the currents through M_{3-4} and M_{5-6} are balanced. Assuming that most of the energy for comparison is used in recharging these nodes, this comparator consumes energy

$$E_{\text{SS}} \cong (2C_X + 1.5C_O) V_{DD}^2 \quad (34)$$

per comparison. Using (29), this comparator's performance norm is

$$N_{\text{SS}} = E_{\text{SS}} \times \frac{\sigma_{v_n \text{ SS}}^2}{V_{DD}^2} \cong 4kT\gamma \left(1 + \frac{3}{4} \frac{C_O}{C_X} \right) \frac{V_{ov}}{V_{th}} \quad (35)$$

and following the assumption $C_O \cong C_X$ in [14], it is further simplified to

$$N_{\text{SS}} \cong 7kT\gamma \frac{V_{ov}}{V_{th}}. \quad (36)$$

From Elzakker's analysis [3] on a two-stage comparator illustrated in Fig. 10(b), its input-referred voltage noise power $\sigma_{v_n}^2$ is derived as

$$\sigma_{v_n \text{ TS}}^2 = 4kT \frac{1}{V_{th} C_F} \frac{I}{g_m} = \frac{2kT\gamma}{C_F} \frac{V_{ov}}{V_{th}} \quad (37)$$

by substituting g_m with $2I/V_{ov}$, and restoring the omitted γ by the assumption $\gamma = 1$ in [3]. During a comparison, the drain nodes of the two input transistors are discharged from V_{DD} to 0, each of which is connected to a large capacitor C_F . Therefore, the energy to replenish these capacitors dominates the total energy consumption, which is

$$E_{\text{TS}} \cong 2C_F V_{DD}^2 \quad (38)$$

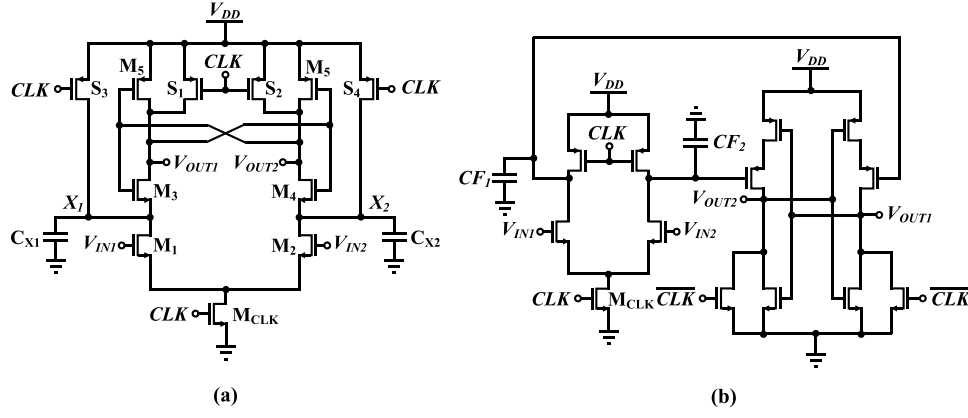


Fig. 10. Conventional dynamic comparators. (a) Single-stage [2], [14]. (b) Two-stage [3].

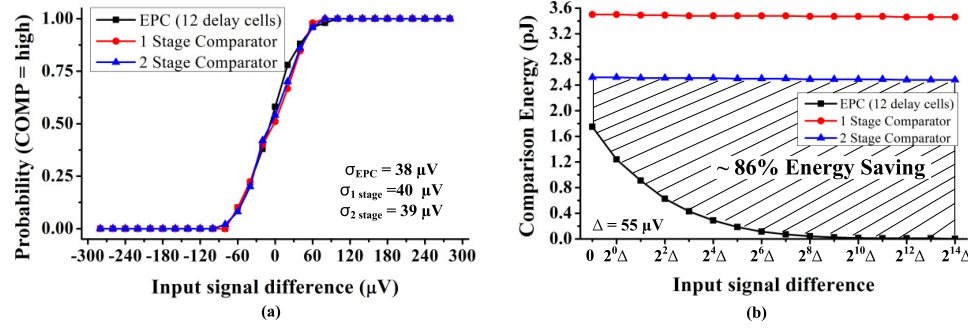


Fig. 11. Comparison of simulated comparator performances among EPC and conventional one-stage [2], [14] and two-stage [3] comparators. (a) Probability for output “high,” inferring input-referred noise. (b) Comparison energy versus input signal difference.

per comparison. Therefore, the comparator’s performance norm is

$$N_{TS} = E_{TS} \times \frac{\sigma_{v_{in}}^2}{V_{DD}^2} = 4kT\gamma \frac{V_{ov}}{V_{th}}. \quad (39)$$

All comparators’ performance norms estimated in (31), (36), and (39) share the same dimension and similar form factored by $kT\gamma$. Ratios among those norms are

$$N_{EPC} : N_{SS} : N_{TS} = S \left(\frac{A}{B} \right) \frac{\pi^2/3}{V_{DD}} : \frac{7}{V_{th}} : \frac{4}{V_{th}} \quad (40)$$

showing that the EPC has relatively smaller norms than the other two, even when $v_{in} = 0$ and $S = 1$ where the EPC does not benefit from the scaling factor S at all. This efficiency gain comes from the following:

- 1) saving energy used for output regeneration (versus a single-stage comparator only), by 4/7;
- 2) increased voltage integration swing from V_{th} to $2V_{th}/V_{DD}$, by V_{DD} ;
- 3) EPC’s bidirectional operation similar to [15], where both pull-up and pull-down currents are used for phase integration, by 1/2;
- 4) fixed phase difference shift threshold for an output decision that prevents a decision with insufficient signal integration, by $\pi^2/12$.

In addition to the above, the EPC can further reduce the average comparison energy due to automatic energy scaling. For example, the EPC consumes only around 1.86x energy per single SAR ADC conversion as discussed in Section IV-B,

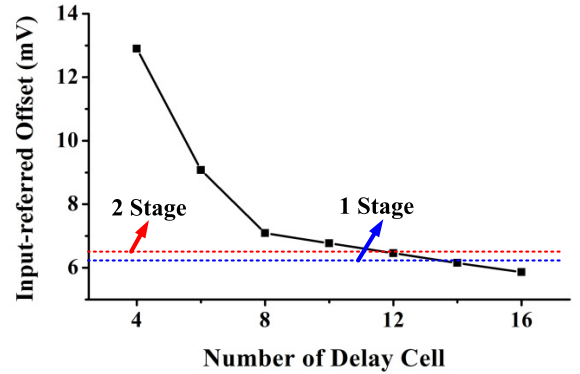


Fig. 12. Simulated input-referred offset voltage versus number of delay cells.

which is comparable with the energy level for only a single comparison of other comparators.

Fig. 11 shows the simulation results of the three comparators compared. With similar levels of input-referred noise [Fig. 11(a)], the EPC shows large energy savings from automatic energy scaling, while the other two comparators show nearly constant energy consumption. Fig. 11(b) shows the simulation results when the V_{ov} is similar among all comparator types considered. The simulation results follow the trend of (40).

D. Offset

The mismatch of the MOSFET causes an input-referred offset voltage, V_{OS} , and it makes a small delay difference, Δt_d , of each delay cell. Since mismatch factors among every delay cell are uncorrelated, the standard deviation of accumulated

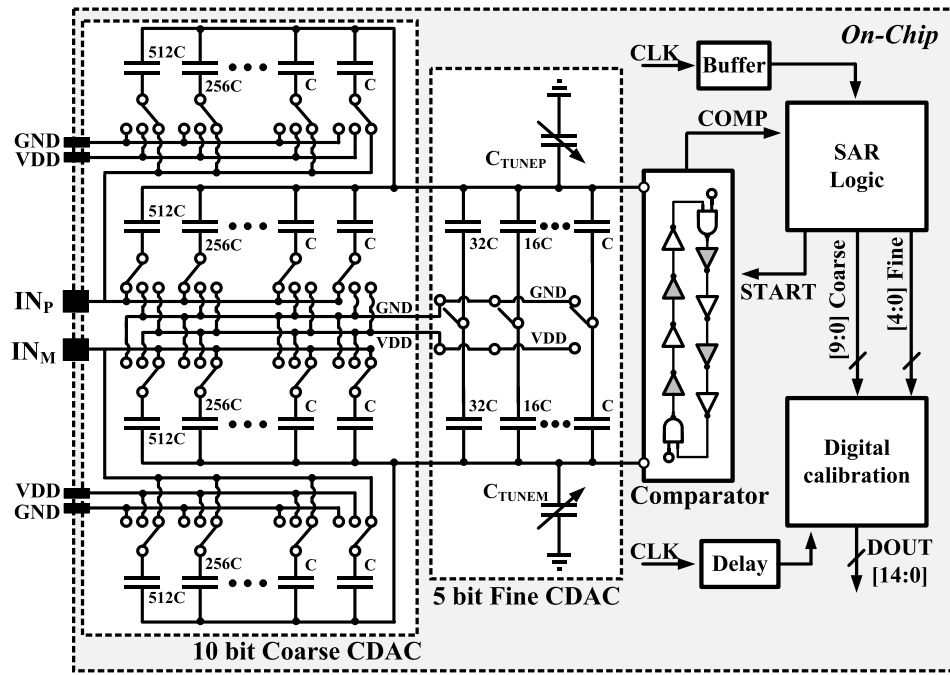


Fig. 13. 15 b SAR ADC architecture with EPC and dual CDAC for high resolution.

delay difference when the edge runs a lap of N -stage delay cells is $\sqrt{N} \cdot \Delta t_d$. According to [8], the voltage to time gain of the N -stage delay cell is $N \cdot \Delta t_d / V_{OS}$, and thus the input-referred offset voltage of the N -stage delay cells, V_{OS_N} , is

$$V_{OS_N} = \frac{1}{\sqrt{N}} \cdot V_{OS}. \quad (41)$$

Therefore, the input-referred offset voltage is dependent only on the number of delay cells. Fig. 12 shows that the Monte Carlo simulation result and the offset voltage are reduced when the number of delay cells is increased.

V. SAR ADC WITH EDGE-PURSUIT COMPARATOR

The EPC was applied to a 15 b high-resolution synchronous SAR ADC that is composed of a CDAC and digital logic as shown in Fig. 13. The EPC uses 16 delay cells, and the number of delay cells is decided by the simulation result that includes the parasitic capacitance. The input-referred noise voltage is under $15 \mu\text{V}$. The EPC has a meta-stability issue because the comparison time is automatically changed according to the input voltage difference. The performance and the comparison time of the EPC are maximized in meta-stability condition. For this reason, the sampling rate of the ADC should be decided by considering the comparison time when the input voltage difference is very small. Fig. 14 shows that the transient noise simulation result when the input voltage difference is 0, 0.5, and 1 LSB, respectively. The maximum comparison time at the 0.5 LSB input voltage difference is smaller than $3 \mu\text{s}$, and thus the sampling rate of the ADC is decided to 20 kS/s. There are some cases that the comparison time is larger than $3.3 \mu\text{s}$ when the input voltage difference is zero; however, the probability is very low and the large code is not caused when the input voltage difference is under the 0.5 LSB.

The CDAC of the SAR ADC consists of the 10 b coarse CDAC, the 5 b fine CDAC, and the 9 b common-mode to

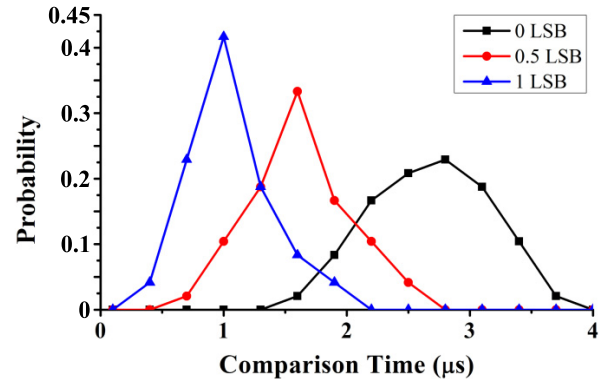


Fig. 14. Simulated probability distribution function of the comparison time at $\Delta V_{IN} = 0, 0.5$, and 1 LSB .

differential gain tuning CDAC. The unit capacitance of the coarse and fine CDACs is 16 fF , and the unit capacitance of the tuning CDAC is 4 fF . The total capacitance value of each plus and minus CDAC is about 16 pF to get an under $15 \mu\text{V}$ kT/C noise. The 10 b differential CDAC is implemented using a split capacitor array [16] to reduce the switching power. The 5 b fine CDAC shares top plates with the CDAC (V_{INP} , V_{INM}) and has the same unit capacitor size as the coarse CDAC. An intentional difference between tuning the capacitors C_{TUNEP} and C_{TUNEM} induces a small differential voltage change as the shared bottom plates of the fine CDAC change, allowing high resolution without significantly increasing the overall CDAC capacitance.

Differing from a conventional bridge-capacitor technique [17], [18], the 5 b fine CDAC has shared bottom plates for each pair of capacitors. Fig. 15 shows the detailed operation of the bottom node switching. First, all bottom nodes of the fine CDAC are reset to GND during the sampling phase. After finishing the 10 b MSB decision using a differential

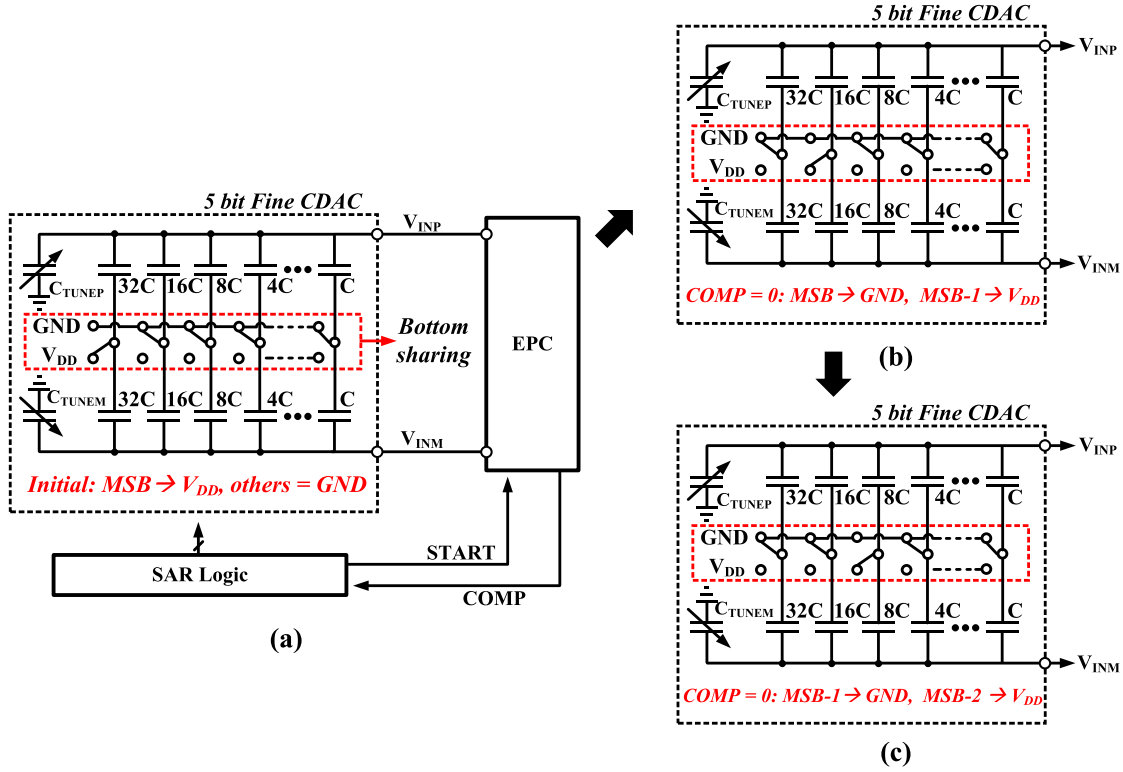


Fig. 15. Operation of 5 b find CDAC during fine-bit decision. (a) Initial state. (b) After a comparison with "COMP = 0." (c) After another comparison with "COMP = 0."

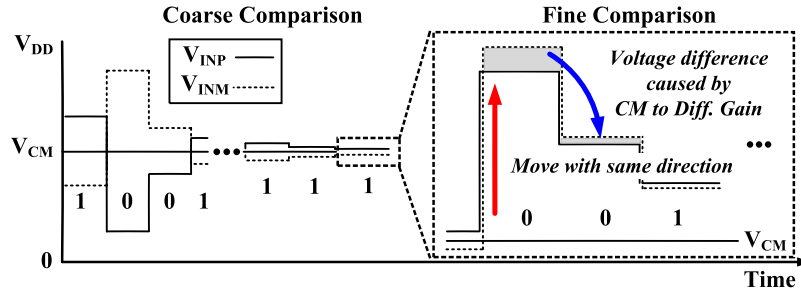


Fig. 16. Operation principle of the fine-bit CDAC generating small voltage change.

CDAC, the shared bottom node of the fine DAC's MSB is set to V_{DD} [Fig. 15(a)]. It changes the differential input voltage into the comparator by half an LSB of the coarse DAC (Fig. 16, upward arrow) to form a middle point for the 11th b decision. After the comparison, the voltage of the MSB bottom node is set according to the comparison result (0 in the example in Figs. 15 and 16), and the bottom node of the second MSB is switched to V_{DD} for the 12th b decision [Fig. 15(b)]. In this manner, the fine CDAC switches its shared bottom nodes in the same way as a usual single-ended SAR ADC [Fig. 15(c)]. Because the bottom node switching injects the same charge into both CDAC top output nodes, switching a capacitor shifts only the common-mode voltage of the two output nodes and does not impact the SAR as long as the two CDACs are completely matched. However, by creating a small imbalance between the total capacitance to ground of the two CDAC output nodes, this common-mode shift will also translate into a small differential voltage difference [Fig. 16]. This common-mode charge injection to differential voltage

gain is fine-tuned using the two tuning capacitors C_{TUNEP} and C_{TUNEM} [Fig. 13].

As depicted in Fig. 17, both the bridge-capacitor technique and common-mode CDAC technique use tuning capacitor arrays to control the fine-to-coarse CDAC gain. Tuning switches in these capacitor arrays have parasitic capacitances whose values vary as the corresponding top voltage changes, possibly injecting harmonic voltage distortion in the sampled signal. Compared with the bridge-capacitor technique, the common-mode CDAC technique is less affected by this distortion because the top plate is shared between the coarse and fine CDAC, where voltage across the tuning capacitors always stays near the input common-mode voltage whenever a fine comparison is performed [Fig. 17(b)]. On the other hand, the top plate voltage of the fine CDAC does not converge to the same level in the bridge-capacitor technique, so the value of the parasitic capacitor can vary more. Hence, the proposed top-plate shared fine CDAC structure shows improved linearity over the bridge-capacitor technique by

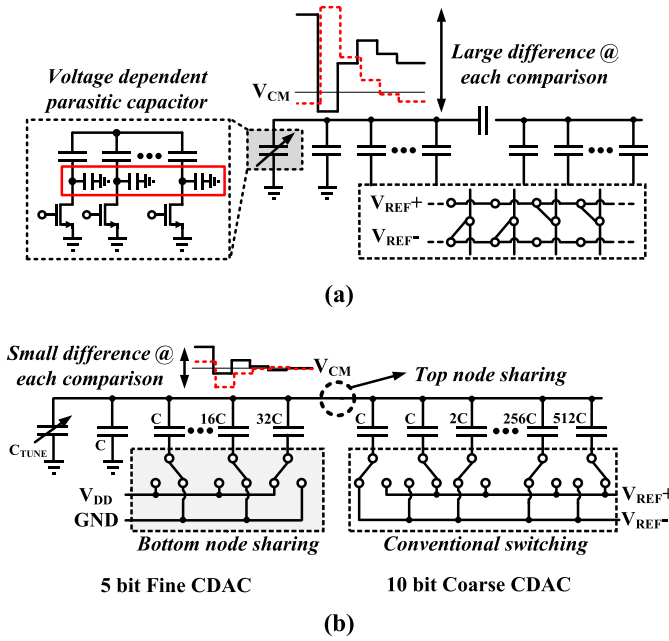


Fig. 17. Comparison between techniques for high-resolution CDAC. (a) Bridge-capacitor scheme [17], [18]. (b) Presented common-mode switching CDAC.

reducing the nonlinearity introduced by the nonlinear parasitic capacitance of the switches controlling C_{TUNEP} and C_{TUNEM} .

The 5 b CDAC with common-mode shifting shares its top node, and thus a mismatch of the fine CDAC can cause more error than the bridge-capacitor technique. However, the mismatch error can be calibrated using several techniques like a redundancy capacitor. On the other hand, it is very hard to reduce the nonlinearity from the voltage-dependent capacitor of switches.

The common-mode rejection ratio (CMRR) is also important design factor for the fine comparison. The maximum common-mode voltage changing at the fine comparison is about 30 mV, and it can change the noise and delay from the current-limiting MOSFETs. However, the common-mode change of about 30 mV is small, and thus the input-referred offset voltage is linear in this small common-mode change when we checked the simulation result. The 9 b tuning capacitor makes the common mode to differential gain in the fine comparison, and the differential gain is also linear in every comparison. For this reason, the input-referred offset voltage can be controlled by changing the tuning capacitor value and it can cancel the CMRR effect of the EPC.

VI. MEASURED RESULTS

The ADC with the EPC was fabricated in a 40 nm CMOS process with a total area of 0.315 mm^2 [Fig. 18]. Shown as a white dot in the middle, the EPC has a very small area of $54 \mu\text{m}^2$, considering its low noise level. The EPC is not located at the center between the CDACs because there are many digital signal lines at the center. Therefore, we move the EPC down to prevent the noise. The different distance between the plus/minus CDAC and comparator leads to different parasitic capacitances of the CDAC top node, but this capacitance value is much smaller than the unit

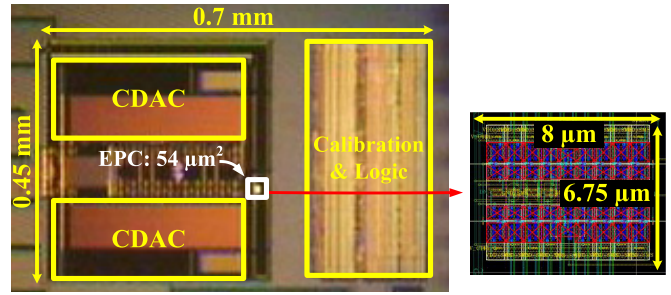


Fig. 18. Die photograph of 15 b SAR ADC with EPC.

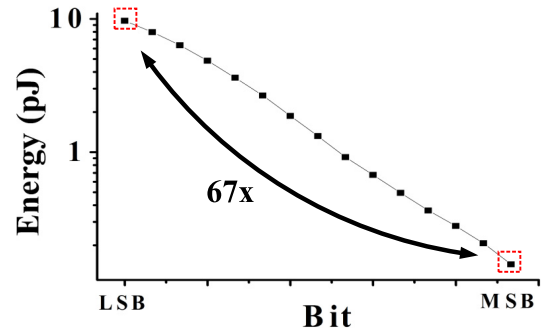


Fig. 19. Measured average comparison energy of the EPC versus SAR ADC bit position.

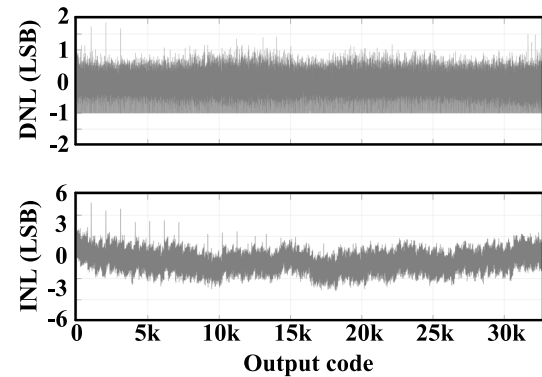


Fig. 20. Measured DNL and INL.

capacitance and the sampling rate of the ADC is slow. Fig. 19 shows the measured average comparison energy for each bit position. The comparison energy for the MSB and LSB bit position differs more than 67 times, proving its wide-range automatic energy scaling. The measured ADC results show a maximum differential non-linearity (DNL)/integral non-linearity (INL) of 1.9/5.2 LSB and a minimum DNL/INL is $-1/-3.2$ (Fig. 20). Tuning capacitor values of the C_{TUNEP} and C_{TUNEM} are decided approximately by checking the output code of the ADC when the very slow and small amplitude is applied and is optimized to get a best DNL and INL. However, the tuning capacitor cannot remove the missing code perfectly and it limits the effective number of bit (ENOB) to 12 b. Spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are 95.1 and 74.12 dB respectively at the Nyquist frequency (Fig. 21), which corresponds to 12.02 b ENOB. Fig. 22 shows the measured frequency spectrum when the input frequency is 0.999 [Fig. 22(a)] and 9.999 kHz [Fig. 22(b)]. The measured frequency spectrum shows that spurs increase when the input

TABLE I
ADC PERFORMANCE SUMMARY AND COMPARISON

	This work	Tai, ISSCC 2014 [4]	Harpe, ISSCC 2014 [7]	Lim, ISSCC 2015 [19]	Liu, ISSCC 2016 [5]	Lee, JSSC 2011 [8]	Bannon, VLSIC 2014 [20]
Technology	40 nm	40 nm	65 nm	65 nm	28 nm	180 nm	180 nm
Architecture	SAR	SAR	SAR	Pipelined-SAR	Pipelined-SAR	SAR	Pipelined-SAR
Resolution (bits)	15	10	12 14	13	12	10	18
Sampling rate, F_s (kS/s)	20	200	32	50000	100000	100	5000
Input voltage range (Differential)	1.8 V_{pk-pk}	Not reported	Not reported	2.4 V_{pk-pk}	1.8 V_{pk-pk}	1.2 V_{pk-pk}	10 V_{pk-pk}
Area (mm^2)	0.315	0.0065*	0.18	0.0544*	0.0047*	0.125	5.74
SFDR	95.1	76.25	78.4 78.5	84.6	75.4	67	Not reported
SNDR	74.12	55.63	67.8 69.7	70.9	64.43	57.7	98.6
ENOB ($(SNDR-1.76)/6.02$)	12.02	8.95	10.97 11.29	11.5	10.39	9.3	16.09
INL_{max} (LSB)	5.2	0.45	0.82 3.50	0.96	0.82	0.8	0.52
DNL_{max} (LSB)	1.9	0.44	0.58 1.75	0.58	0.53	0.4	0.10
Total Power (μW)	1.17	0.084	0.310 0.352	1000	350	1.3	60520
Critical Power** (μW)	0.104	0.025***	0.124 *** 0.141 ***	336***	119***	0.130***	Not reported
FOMs (dB)	173.4	176.8	174.9 176.3	174.9	176	163.6	177.7
FOM_C (dB)****	184	181.6	178.9 180.2	179.7	180.6	173.6	-

* Active area ** Power for noise critical block (comparator in SAR, amplifier in pipelined SAR)
*** Calculated value from the paper/presentation material **** $SNDR+10\log(F_s/2/(Critical\ power))$

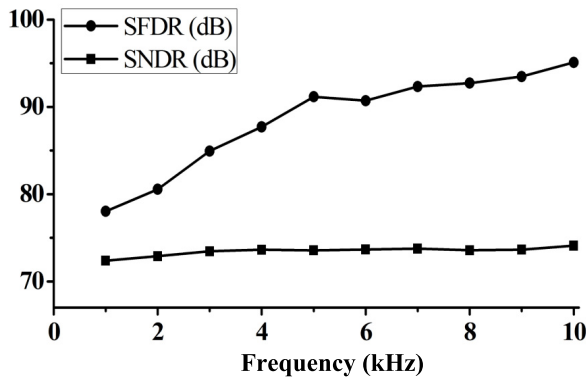


Fig. 21. Measured SNDR and SFDR versus input signal frequency.

signal frequency is reduced, because the bandpass filter has a lower harmonics suppression and a larger signal attenuation at low input frequency. Fig. 23 shows that the EPC consumes 104 nW at the Nyquist frequency, representing only 8.9% of the total ADC power of 1.17 μW .

Table I summarizes the performance of the implemented ADC with the EPC, and compares it with other similar works on SAR or pipeline-assisted SAR ADCs. To compare the EPC's efficiency with other ADCs adopting different architectures more clearly, a new figure of merit, named FOM_C , is derived from the Schreier Figure-of-Merit (FOMs). In FOM_C , the total power consumption term of the original Schreier FOMs is replaced by the power dissipation of the noise-critical blocks only, such as the comparators in SAR ADCs, amplifiers in pipelined ADCs, and integrators in delta-sigma ADCs, giving more emphasis on the energy efficiency of noise-critical

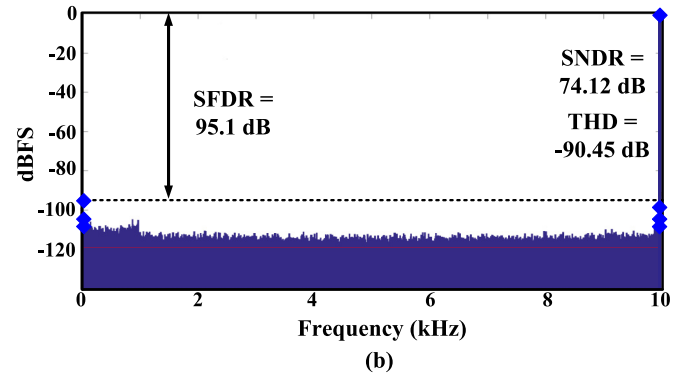
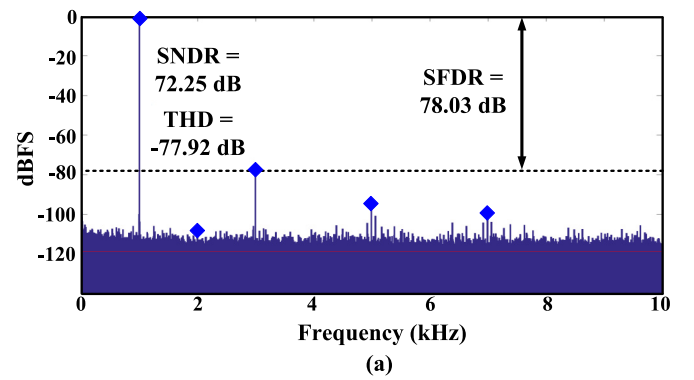


Fig. 22. Measured frequency spectrum. (a) $f_{in} = 0.999k$. (b) $f_{in} = 9.999k$.

blocks. The CDAC is also a critical noise source for the ADC; however, the performance of the SAR ADC is limited by the CDAC mismatch. Consequently, a 15 b CDAC is more than necessary specification considering the final ADC performance

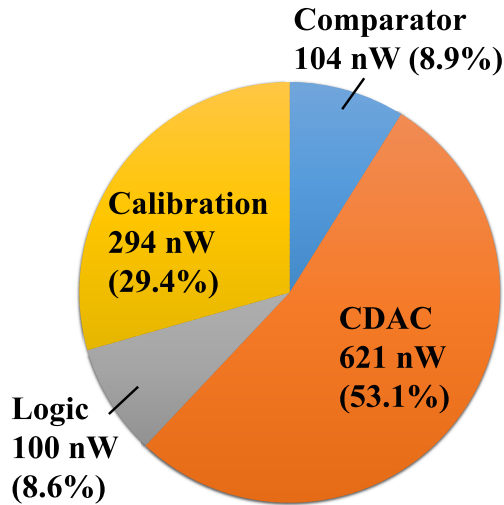


Fig. 23. Measured power consumption of the SAR ADC at Nyquist frequency.

(12 b ENOB), and therefore the CDAC power is not included in the FOM_C

$$FOM_C \equiv SNDR + 10 \log \left(\frac{F_S}{2 \times (\text{Critical Power})} \right). \quad (42)$$

While the FOMs of the ADC is 173.4 dB, the FOM_C of the EPC in this SAR ADC is calculated to be 184 dB, which compares favorably with other similar designs. This underscores the applicability of the EPC to other low-power SAR ADC topologies.

VII. CONCLUSION

This paper presents an energy-efficient comparator, named the EPC, with an automatic energy scaling capability according to the input difference. Capacitors in the oscillation path are recycled many times during phase-based operation, which allows for accurate comparisons with a small area and total capacitance. Bidirectional signal integration naturally occurs as edges propagate, offering extra efficiency gain. A 15 b SAR ADC using a small EPC of $54 \mu\text{m}^2$ shows a 74.12 dB SNDR and a 173.4 dB FOMs at the Nyquist frequency of 10 kHz. The EPC shows $67\times$ automatic energy scaling between the MSB and LSB bit decisions without any external control, saving a significant portion of the energy for the MSB decision. It also has a 184 dB FOM_C , which is the best number among the designs compared.

ACKNOWLEDGEMENT

The authors would like to thank TSMC University Shuttle Program for chip fabrication and Analog Devices and for partial financial support.

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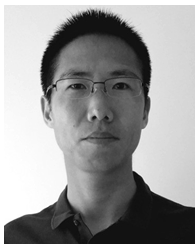


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Dr. Sylvester was a recipient of the NSF CAREER Award, the Beatrice Winner Award at ISSCC, an IBM Faculty Award, an SRC Inventor Recognition Award, and ten best paper awards and nominations. He was also a recipient of the ACM SIGDA Outstanding New Faculty Award and the University of Michigan Henry Russel Award for distinguished scholarship. He serves on the technical program committee of the IEEE International Solid-State Circuits Conference and previously served on the Executive Committee of the ACM/IEEE Design Automation Conference. He served as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS (CAD) and the IEEE TRANSACTIONS ON VLSI SYSTEMS and a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II: EXPRESS BRIEFS.

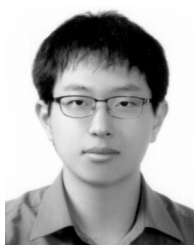


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