Synchronization of Ultra-Low Power Wireless Sensor Nodes

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***Abstract*—Radio activation in ultra-low-power wireless sensor nodes can require 5-6 orders of magnitude higher power than the sensor's average power consumption. Therefore, accurate timers that allow multiple sensor nodes to synchronize their radio communication are of critical concern for minimizing radio energy consumption. In this paper, we review ultra-low power timers and demonstrate their importance for the overall sensor node energy budget. We also propose a multistage gate-leakage-based timer with boosted charging and temperature compensation that reduces the synchronization uncertainty by 4.7× compared to the best prior gate-leakage-based timer with 660pW power consumption. Effective temperature sensitivity is reduced to 31ppm/°C.**

I. INTRODUCTION

Wireless sensor networks are a key enabler of future ubiquitous computing since they can provide countless information collection points to computing systems. Large numbers of sensors can collect abundant information needed for home automation, building monitoring, environmental monitoring or medical diagnostics through wireless networks. In a wireless sensor network, each node takes measurements with its sensors continuously or periodically. Then the measured data is processed with integrated data processing units to extract useful data or detect critical events that have to be communicated to the user. This user-interested data created by each sensor node is transferred to a gate-way sensor node or base station through wireless communication and merged with data from other sensor nodes. By processing this merged data, a bigger picture of the monitored object can be obtained which also can be used for controlling actuators if necessary.

With advances in circuit and system design, packaging and battery technologies, ultra-low power (ULP) sensor nodes with millimeter-scale volume are demonstrated recently (Figure 1). By reducing average operation power by multiple orders of magnitudes, these sensor nodes can last years with sub-mm^3 thin-film Li-ion battery or can be powered with integrated energy harvesting solar cells. Reduction in battery and silicon size enables millimeter-scale form factors and such extremely small sensor systems can potentially enable numerous new applications where small size matters, such as implantable sensors. Small silicon area also reduces the manufacturing cost per nodes, allowing cheaper sensor network expansion.

The operating power of millimeter-scale ULP sensor node is dramatically reduced by various circuit techniques

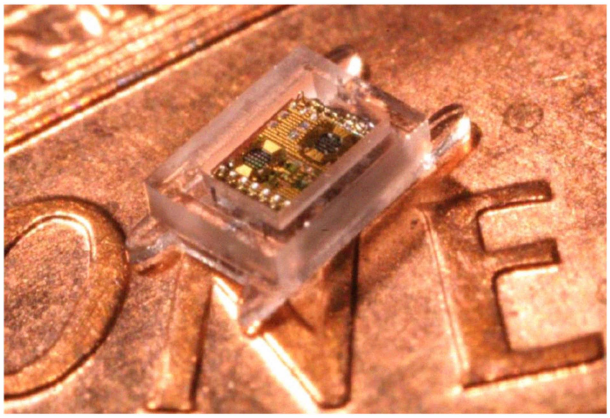

Figure 1. Recently demonstrated millimeter-scale ultra-low power sensor [1]

applied to each circuit component. Data processing processors and other logic circuits are designed to operate at energy-optimal voltage and frequency, and duty cycled to minimize leakage power. Memories are made with high threshold devices and operated with near-threshold supply voltage to reduce the leakage current. Bank-level or even word-level power gating can be implemented to further reduce the standby power. For energy-efficient power management with small load current, switch capacitor network is used to provide desired DC supply voltages. Integrated solar voltaic can be implemented to provide secondary energy source. Together with these circuit design techniques, the average operation power of millimeter-scale ULP sensor nodes is brought down to the nano-watts level. However, unlike the other sensor building blocks, power consumption of radio transceiver could not have been reduced significantly due to the physical limit of antenna efficiency and size. Therefore, average active power of the radio of a sensor node still falls in at least hundreds of micro-watt regime, which is at least 5 to 6 orders of magnitude higher than average power of the rest of sensor node components. Therefore, the radio cannot be activated continuously and has to be duty-cycled with limited energy budget.

Figure 2 shows an example scenario of a sensor node radio duty-cycling. For efficient radio duty-cycling, each sensor node has to be able to precisely determine the time to activate its radio to communicate with other nodes. In this example, the sensor nodes takes measurement every 20 minutes and exchange data hourly. Since the energy budget of ULP sensor nodes stringently limits the power consumption of the components that are always on, only

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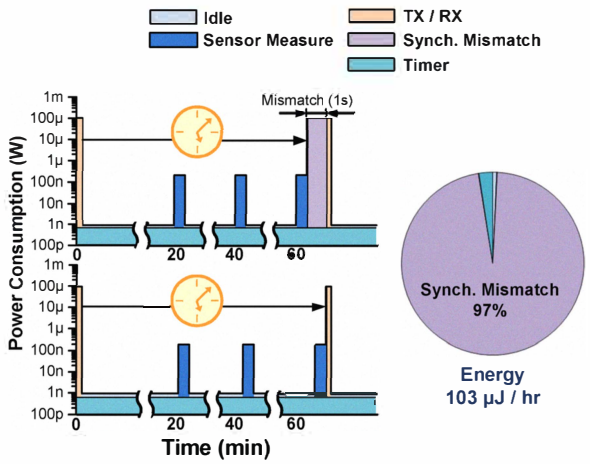

Figure 2. An example synchronization scenario of ultra-low power wireless sensor node

timers with sub-nW power consumptions can be used. Measuring 1 hour synchronization period with such timers can easily incur 1 second time error, which requires 1 second additional radio on-time to detect overlap of radio activation window of communicating sensor nodes. Due to extremely high radio power penalty, energy consumed for such overlap detection can dominate the energy budget of the sensor node as shown in Figure 2. Therefore, implementing ULP timers with acceptable accuracy for wireless sensor node synchronization is of great concern since it can significantly reduce not only the overhead for radio overlap detection but also overall energy budget of the sensor node.

In following section, two main factors that affect ULP timer accuracy are discussed. Then, state-of-the-art ULP timers that can be potentially used with ULP sensor nodes will be reviewed in Section III. Finally, recently proposed multi-stage gate-leakage-based timer with temperature compensation is presented in Section IV.

II. Timer Characterization for Sensor Node Synchronization

For precise time interval measurement, timer has to sustain consistent oscillations. However, thermal – or other source of - noises in electrical circuits cause temporal period deviation, i.e. jitter, and environmental changes such as temperature change creates period shift. Therefore, by characterizing magnitude of jitter and sensitivity to environment variation, accuracy of a timer can be characterized.

Period deviation due to the noise is often in Gaussian random and its magnitude of deviation can be characterized with RMS jitter which is defined as standard deviation of timer period. To compare the jitter of two different types of timers, normalized RMS jitter expressed in ppm is often used. However, the accuracy of a timer for measuring multi-cycle synchronization period is not well captured by these metrics since they ignore the averaging of jitter over multiple timer cycles. For example, there can be two timers with identical ppm jitter, but their accuracy for measuring one hour synchronization period can be different since the timer with shorter period will have more cycles to count, hence more averaging of jitters. Uncertainty of timers can be well characterized with Allan deviation which is defined by equation (1), where τ is the observation period and y_n is n-th fractional frequency over observation time τ. However, to portrait magnitude of synchronization timing error that ULP sensors can have, the standard deviation for measuring various synchronization periods will be presented first. Then measured Allan deviation will be presented in Section IV to compare ULP timers.

$$\sigma_y{}^2(\tau) = \frac{1}{2}\langle (y_{n+1} - y_n)^2 \rangle, \quad \sigma_y(\tau) = \sqrt{\sigma_y{}^2(\tau)} \quad (1)$$

The period of timers can be affected by the changes in environmental conditions. Battery voltage degradation or ambient temperature change can cause shift in timer period. Therefore it is important to implement timers which are insensitive to these environmental changes. By utilizing supply voltage regulation with supply-insensitive reference voltage, supply variations can be mitigated to certain extent. However, a sensor nodes can experience large amount of temperature changes and, oftentimes, sensor nodes are designed to sense these temperature deviation. For this reason, temperature sensitivities of ULP timers have to be examined as an indicator of sensitivity to environmental changes.

III. State-of-the-art Ultra-Low Power Timers

Recently, ultra-low power timers with sub-nW power consumptions are introduced for ULP sensor applications. In this section, two state-of-the-art ULP timer topologies will be discussed in detail and examined for its accuracy and temperature sensitivity.

A. *Single stage gate-leakage based timer*

An ULP timer with pW power consumption can be implemented by operating with sub-threshold supply voltage and using gate-leakage current of transistors for generating oscillation. Figure 3 shows the structure of single stage gate-leakage based timer proposed in [3]. In this timer, a load capacitor (C_L) is charged with gate-leakage current of a pair of thin-oxide PMOS and NMOS transistors (MN, MP). As the load capacitor is charged up to the high threshold voltage of sensing Schmitt trigger, the body, source and drain of MN and MP are driven to ground to discharge C_L. Repeating same procedure for discharge creates the oscillation.

Unlike the prior-art timers that use drain current for sustaining oscillations at load capacitors, single stage gate-leakage based timer can slow down the oscillation to sub-Hz with the gate current on the order of 10s of pA/µm[4]. Therefore active energy consumed for sustaining oscillation can be significantly reduced. However, the

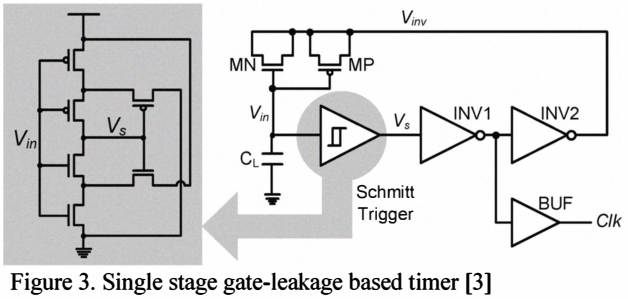

Figure 3. Single stage gate-leakage based timer [3]

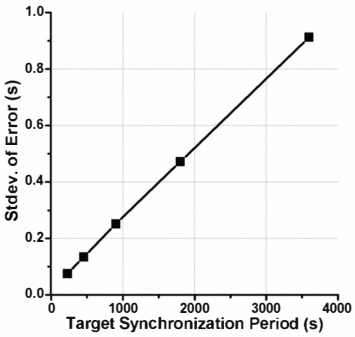

Figure 4. Synchronization period measurement error with single stage gate-leakage based timer

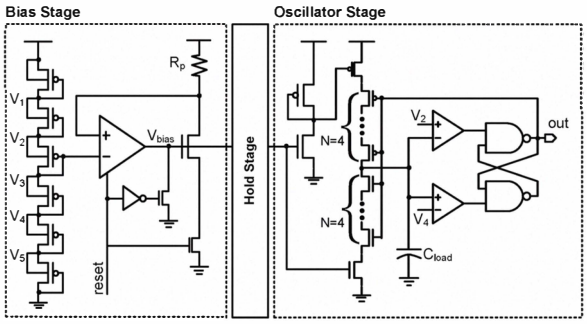

Figure 5. Structure of program-and-hold Timer [5]

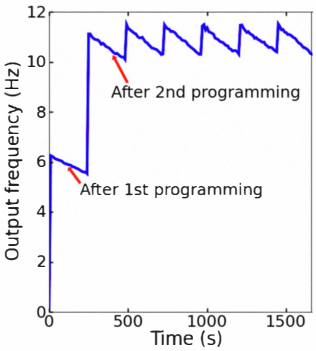

Figure 6. Period deviation of program-and-hold timer

reported RMS jitter of this timer was 1400ppm and our measurement shows that standard deviation for measuring 1 hour synchronization period was 913ms (Figure 4). This clearly indicates that synchronization cycle measurement error for each node can easily be on the order of seconds, which will cause significant radio power consumption for overlap detection as discussed in the example scenario in Section I. Therefore, this timer can only be used for shorter synchronization cycle or the timer stability has to be significantly improved for 1 hour synchronization cycle.

Utilizing gate-leakage current benefits not only from low power consumption but also from low temperature sensitivity. To build low power sub-Hz timer with drain current, sub-threshold supply voltage is often used to reduce the power consumption. However, line sensitivity of sub-threshold drain current is very high, typically can vary 2 orders of magnitude along 100 degree temperature range. Therefore, similar amount of variation in timer period is observed. Contrary, gate leakage current is less sensitive to supply voltage. The temperature sensitivity of single stage gate-leakage based timer is 0.16%/°C at 600mV and 0.6%/°C at 300mV, which translates into 16% and 60% for 100 degree range. However, the timing error due to temperature sensitivity can be significantly higher than the timing error caused by jitter. To mitigate this problem, program-and-hold timer is introduced to lower the temperature sensitivity.

B. *Program-and-hold timer*

Figure 5 shows the structure of program-and-hold timer presented in [5]. This timer consumes 150pW which is still well within the power budget for timer in ULP wireless sensor node. To lower the temperature sensitivity, temperature self-compensation is implemented. In programming mode, a bias voltage is generated with a current reference, which consists of a reference voltage (V_3) and a polysilicon resistor (R_p) with low temperature coefficient. This bias voltage is stored in hold stage and bias stage is turned off in active mode to reduce active power. The bias voltage is periodically refreshed and used for biasing oscillator stage.

With self-temperature compensation and refreshing bias voltage every 2 minutes, period deviation due to temperature was reduced down to 5% for 0-90°C operation range. However, between bias voltage refresh operations, the bias voltage stored in hold stage slowly drops as charges on storage capacitor leaks away. This change in stored bias voltage incurs bias current deviation in oscillator stage. As a result, period of program-and-hold timer periodically drifts and this drift can be as large as 10% of its period as shown in Figure 6. This means that time measurement error can be up to 10% depending on the time from last programming operation. The magnitude of this deviation can be reduced by more frequent refresh operation but this is very expensive in power since the power consumption for programming mode is very high (220nW). Therefore, despite the lower temperature sensitivity, program-and-hold timer cannot be a suitable timer for measuring synchronization cycle period.

IV. Multi-Stage Gate-Leakage-Based Timer for ULP Sensor Node Synchronization

A multi-stage gate-leakage based timer is introduced to reduce both uncertainty and temperature sensitivity significantly. This timer also oscillates with gate-leakage current to consume minimum power but various circuit techniques are used to lower uncertainty and temperature sensitivity.

A. *Lowering uncertainty*

In previous version of gate-leakage based timer, there is only one loading capacitor that is charged/discharged for oscillation. A Schmitt trigger is used to determine high and low threshold voltage at this capacitor node for switching between charging and discharging mode. It is desired to have high amplifier gain at these switching points to reduce uncertainty during this switching operation. Steeper voltage slope at the switching point also helps for same reason. At the same time, steeper voltage slope during charging is preferred since the accumulated thermal noise voltage at the capacitor node can be translated into smaller timing error with steeper voltage slope.

The structure of Multi-stage timer is shown in Figure 7. In this topology, one stage is in charging mode and the rest are in discharging mode for any given time. As the voltage of charged capacitor reaches threshold voltage of connected inverter, next stage is placed in charging mode while current stage is put in discharging mode. Since an inverter typically has higher gain than a Schmitt trigger, uncertainty due to low amp gain can be reduced. To make voltage slope much steeper, boosted charging is utilized, significantly reducing jitter. With N stage timer, capacitor in each stage experiences N-1 timer longer discharging time than charging time. As N increases, the slope at node Q[n] at the end of discharging state is lowered (from -

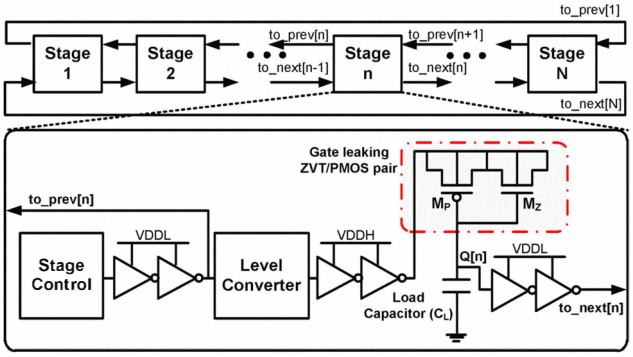

Figure 7. Multi-stage gate-leakage based timer [6]

238mV/s to 20mV/s for n from 3 to 10), which makes the initial capacitor node voltage for following charging mode less sensitive to uncertainty.

Multi-stage gate-leakage based timer shows significant uncertainty reduction over single stage timer. Figure 8 shows the standard deviation (σ) of the errors for measuring various time periods. For measuring one hour, σ was 196 ms which was 4.7× smaller than single-stage timer. Allan deviation was calculated form measured data to compare single and multi-stage gate-leakage based timer (Figure 9). For entire time range examined, multi-stage timer clearly shows large improvement over single stage timer.

B. Temperature compensation

Temperature compensation can be implemented in gate-leakage based timer by exploiting the opposite temperature dependencies of gate leakage in ZVT and PMOS during charging. By digitally tuning the size of ZVT and PMOS transistors with transistor array shown in Figure 10, the first order temperature sensitivity can be eliminated. This compensation scheme results in residual secondary order sensitivity, which has minimum temperature sensitivity at different temperature band depending on the size ratio between ZVT and PMOS transistors. Our measurement shows that optimal sizing ratio gives 3% period deviation over -20 to 60°C range, equivalent to 375ppm/°C. To further reduce temperature sensitivity, the ratio of ZVT and PMOS transistors can be dynamically tuned as temperature changes and tracking the period with switched configuration. With using 10 configurations for -20 to 60°C range, effective temperature sensitivity could be reduced down to 31ppm/°C.

V. CONCLUSION

Energy budget of ULP wireless sensor node can be dominated by radio power consumption unless accurate measuring of synchronization period is provided with reasonable power budget. Recent ULP timers with sub-nW power budget used gate-leakage current to reduce power and program-and-hold technique to reduce temperature sensitivity. However they still had high uncertainty and temperature sensitivity to be used for wireless sensor node. We proposed a multi-stage temperature compensated timer, which showed synchronization uncertainty reduction by 4.7× compared to the best prior gate-leakage-based timer. With multi-configuration temperature compensation, temperature sensitivity could be reduced down to 31ppm/°C.

ACKNOWLEDGMENT

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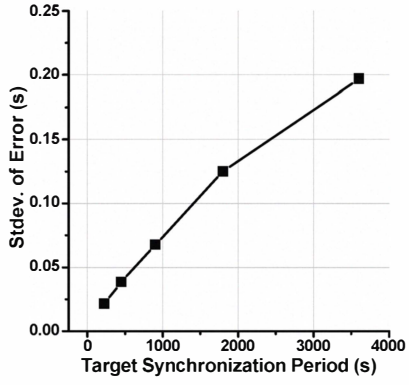

Figure 8. Synchronization period measurement error with multi-stage gate-leakage based timer

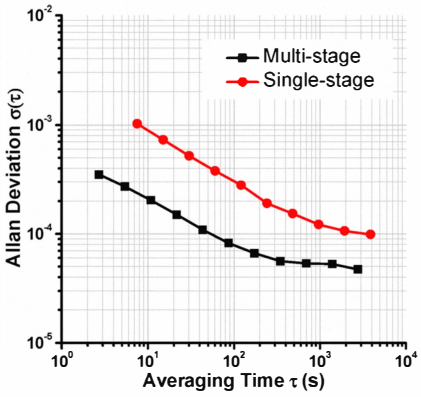

Figure 9. Allan deviation of gate-leakage based timer

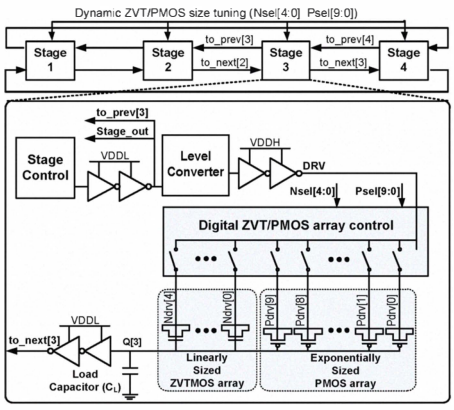

Figure 10. Temperature compensated multi-stage gate-leakage based timer