A 5.58 nW Crystal Oscillator Using Pulsed Driver for Real-Time Clocks

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Abstract—A 5.58 nW real-time clock using a crystal oscillator is presented. In this circuit, the amplifier used in a traditional circuit is replaced with pulsed drivers. The pulse is generated with precise timing using a DLL. With this approach, an extremely low oscillation amplitude of 160 mV results in low-power operation. This low-amplitude oscillation is sustained robustly using additional supply voltages: a lower supply for the final drive stage and a higher supply used for pulses that drive the final drive stage, which ensures low ON-resistance necessary for reliable operation. The different supply levels are generated on-chip by a switched capacitor network (SCN) from a single supply. The circuit has been tested at different supply voltages and temperatures. It shows a minimum power consumption of 5.58 nW and power supply sensitivity of 30.3 ppm/V over supply voltage of 0.94–1.2 V, without degrading the crystal's temperature dependency: between −20 °C and 80 °C. Moreover, its performance as a real-time clock has been verified by measurement of an Allan deviation of 1.16×10^{-8}.

Index Terms—Crystal oscillator, low power, pulsed driver, real-time clock, wireless sensor node.

I. INTRODUCTION

BELL'S law of computing classes [1] states that approximately every decade, a new computer class with lower price and volume replaces the previous class. Extending this prediction to the next decade, the next computing class is expected to have a size that is orders of magnitude smaller than today's cell phones. One of the best examples of the next computing class is the wireless sensor node. With significant computing power packed within a small volume and lower cost—thus the term *smart dust* [2]—it has the potential to change how people interact with the environment. However, many issues still remain to be solved, which have been the focus of active research to realize wireless sensor nodes and use them for continuous monitoring devices [3], [4]. Possibly, the most significant challenge rises from limited power and energy budgets.

For wireless sensor nodes, the volume that can be allocated to the battery is orders of magnitude smaller than a cell phone [2]. In some applications, the system does not have any battery and operates directly from an energy harvester [5] or is wirelessly coupled to a power source, severely limiting the power budget of the different circuit blocks. One of the key building blocks

in a sensor node system is the real-time clock, which keeps track of the wall-clock time. The power budget and accuracy requirement of a real-time clock depends on the sensor node use scenario. Under one typical scenario, shown in Fig. 1(a), a processor is activated every 20 min to take a measurement which could take 100 ms at 3 μW. Then, once every hour, the processor transmits this data to a base station, requiring ∼1 ms at 1 mW. For the remainder of the time, the whole system will be put into sleep mode where it will consume only idle power, which has been shown to have a limit as low as ∼1 nW [4]. Since the base station is supplied with power from a wired source (e.g., a wall plug), it can listen for a transmitted signal continuously. Hence, the sensor nodes do not have an extremely high timing accuracy requirement, and an on-chip timer that consumes as little as 0.66 nW with an average random error of 200 ms over an hour [6] can be used, providing for an extremely low-power system that can be highly miniaturized.

However, for some applications, sensor nodes have to communicate with each other. In such a scenario, these nodes will have synchronized timing references, and two nodes will transmit and receive data when they are notified by their timing references to do so. Unfortunately, two independently operating timing references will suffer from mismatch because of random behaviors such as jitter. This scenario is shown in Fig. 1(b). Given a silicon-based timing reference, operating in sub-nW range such as the 0.66 nW timer in [6], two nodes are expected to have a random mismatch of 200 ms in an hour due to the high-frequency instability which corresponds to 56 ppm in an hour. In this case, the RF communication module of one node will be activated earlier than the other and has to wait until the second node comes online before it can initiate communication. During this mismatch time window, the RF module consumes substantial energy, which comes to dominate the total power consumption as shown in Fig. 1(b) and increases the average power consumption to 57 nW, which is 38 times larger than the previous case.

To avoid this high energy loss during timer mismatch, each node must be equipped with a high accuracy timing source. Crystal oscillators (XO) provide a more constant frequency than silicon-based timers; however, they usually consume much higher power than an ultra-low-power sensor node system, typically in the range of μW to hundreds of nW.

To address these issues, this paper proposes a new XO topology that lowers power consumption while maintaining the crystal's frequency stability. A novel pulse charge injection scheme realized by a DLL is introduced to replace the traditional amplifier. Furthermore, extremely low oscillation amplitude of 160 mV is realized, which results in low-power
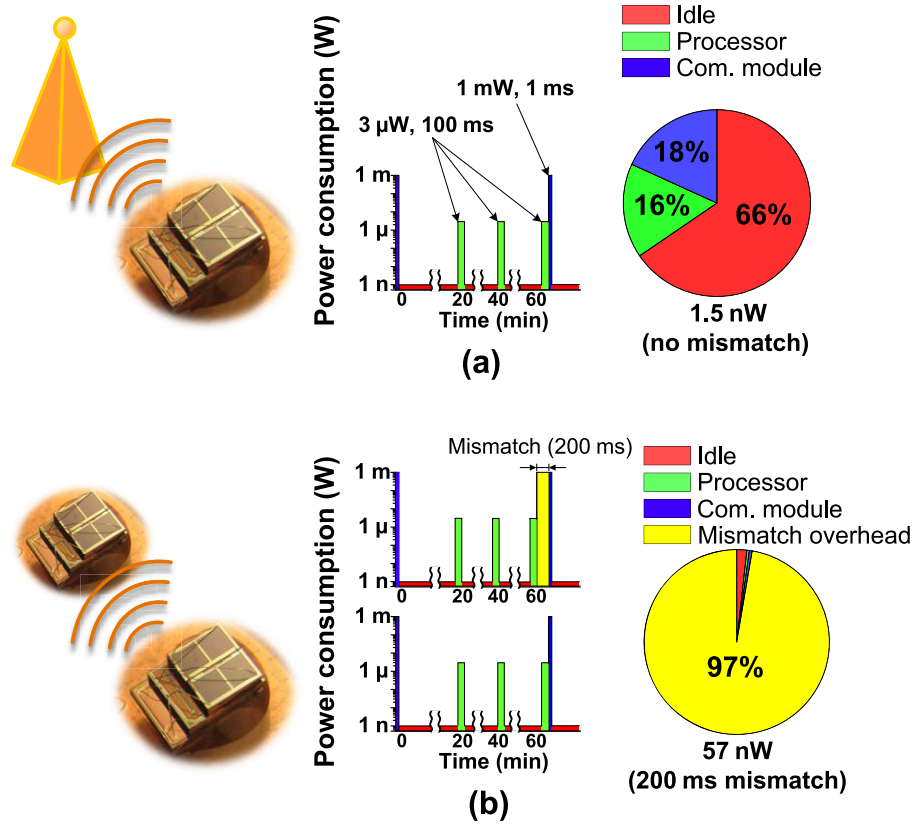
Fig. 1. Operation scenarios of WSN. (a) Node-to-base station communication. (b) Node-to-node communication with mismatch.

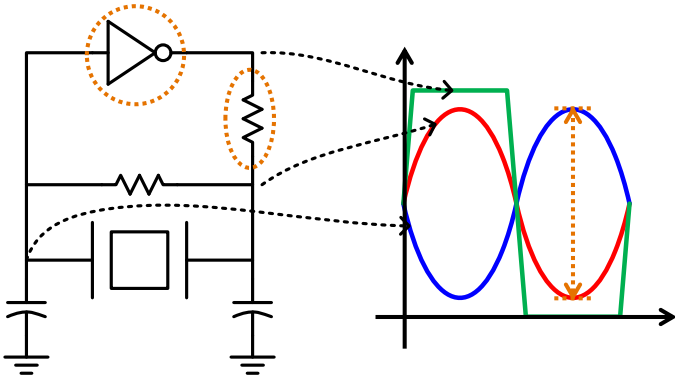Fig. 2. Conventional XO circuit and waveform.

operation. This low-amplitude oscillation is sustained robustly using two supply voltages: 1) a lower supply, which is used for the final drive stage, and 2) a higher supply, which is used to generate the pulses that drive the final drive stage. An on-chip switched capacitor network (SCN) generates multiple levels of voltage to operate different parts of the circuit for optimum power and performance.

This paper is structured as follows. Section II discusses prior works. Section III introduces the proposed topology for the XO and its operating principle. Section IV discusses the theory of the proposed XO circuit operation. Section V discusses each circuit block in detail. Section VI presents measurement results of the test chip. Finally, Section VII concludes this work.

II. PREVIOUS WORKS

To analyze the issues with a conventional XO driver topology, the basic configuration is shown in Fig. 2. An inverter in closed loop amplifies noise at its input to kick-start the oscillation. At the same time, it provides a 180° phase shift and generates lost energy each period to maintain crystal oscillation. For this configuration, inverter gain is uncontrolled. As a result, the inverter output is clipped and a square wave is generated. To avoid this, a series resistor at the output is introduced to control the drive level. A crystal driven at prohibitively high power levels—called the overdrive level—is known to suffer from reliability issues, which degrades frequency stability and sometimes leads to oscillation at higher overtone. This resistor also forms a low-pass filter with the capacitor which avoids the crystal oscillating at higher overtone frequencies. However, there are three noticeable sources of power loss in this circuit. 1) The driver itself consumes significant static power. Because its input signal is a sinusoidal wave, the driver is never completely turned OFF, which results in static current. 2) Uncontrolled gain of the inverter produces high oscillation amplitude, which leads to increased power loss by the crystal itself in each cycle. 3) The series resistor dissipates energy since the difference between square wave at the driver output and sine wave oscillation at the crystal is dissipated by this resistor. Overall, this configuration will typically consume power in hundreds of nW to a couple of μW for a 32.768 kHz crystal. While power consumption can be reduced by lowering supply voltage, there is a lower bound

Fig. 3. Overview of widely used low-power XO circuit.

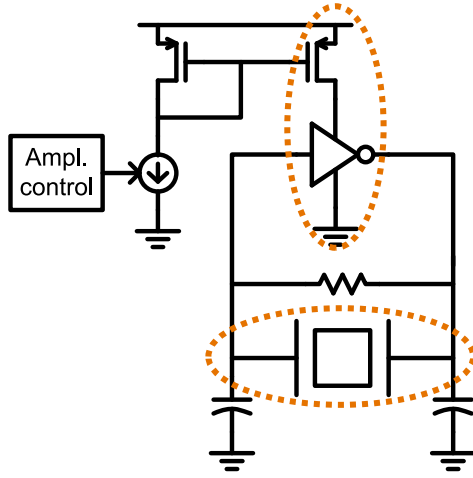Fig. 4. Preamplifier concept of the proposed circuit.

on how much the supply voltage can be reduced in this topology due to the following fundamental dependency. Smaller oscillation leads to smaller input signal to the driver. This smaller oscillation input makes the driver weaker which requires a larger driver and careful selection of design parameters to sustain the oscillation. As the oscillation drops below the threshold voltage of the inverter transistors, the drive strength increases very rapidly, restricting oscillation amplitude to higher, super threshold voltages with associated higher power levels.

To cope with this problem, a novel circuit was proposed in [7] and [8], which is shown in Fig. 3. This circuit monitors the oscillation amplitude and controls the bias current of the driver. Using an active feedback control loop, this approach can reduce driver current, which reduces oscillation amplitude and eliminates the need for a series resistor. The lowest power consumption reported using this scheme with a 32.768 kHz crystal is 27 nW from the oscillation alone, and 32 nW including the output buffer to generate a full-swing signal [9]. More recent work using this scheme is introduced in [10], which consumes 38.4 nW using a 50 kHz crystal in a 130 nm process. However, this level is still larger than the standby power consumption of the whole system in an ultra-low-power WSN application [4], [11]. The power consumption in this topology is due to the following reasons. 1) Although smaller than the conventional circuit, the driver still dissipates static bias current. 2) The topology still requires a high-supply voltage and significant power is dissipated in the current mirror transistors. 3) The closed-loop control system including the amplitude monitoring circuit which made the 27 nW oscillation power possible, consumes significant power itself. Furthermore, the oscillation amplitude is controlled by device sizing in the current mirror loop, which requires good device matching. Therefore, to accommodate process variation, the system requires significant margin in transistor size to ensure robust operation over a wide range of operating conditions, especially as the voltage amplitude reduces and transistors operate in the subthreshold region. This in turn increases the minimum oscillation voltage.
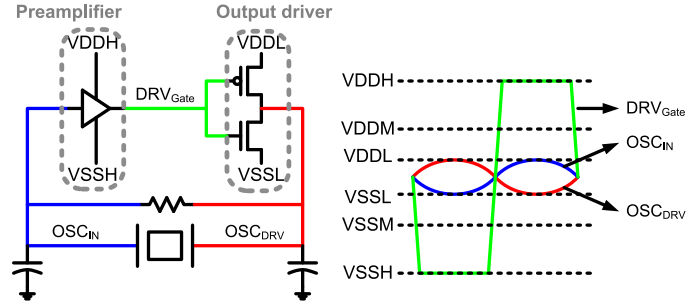
III. PROPOSED APPROACH

To further reduce the power consumption of an XO, we propose a new circuit topology which uses a preamplifier concept, which is the first of two key components for the proposed circuit. Considering again the conventional circuit with only a single inverter in Fig. 2, a preamplifier is placed before the output driver as shown in Fig. 4. A new V_{DD} (V_{DDL}) and ground (V_{SSL}) pair—which will be called low-voltage supply— smaller than the nominal V_{DD} (V_{DDH}) and ground (V_{SSH}) pair is supplied, so that oscillation amplitude is kept small. Then, a larger voltage is supplied to the preamplifier, so that the small input signal is amplified before being applied to the output driver. This provides the output driver with maximum gate-to-source voltage, minimizing ON-resistance of the transistor and supports immediate transfer of energy to the oscillation with minimum loss in the transistor. This supply voltage pair is referred to as the high-voltage supply. In this configuration, the smaller oscillation amplitude no longer weakens the driver. With the help of the higher input signal to the driver, it now has very low ON-resistance and can maintain oscillation robustly, even at very small low-voltage supply. In addition, the driving transistor now operates in the linear region instead of subthreshold region, which helps to cope with PVT variation better. In addition, the ON-resistance is less dependent on V_{DS} and hence oscillation amplitude. With boosted V_{GS}, the ON-resistance remains low even when oscillation amplitude (V_{DS}) is reduced, which is important for maintaining stable oscillation when oscillation amplitude is reduced.

This approach, however, has two remaining issues that need to be addressed. If the preamplifier is implemented using an operational amplifier with enough bandwidth, the preamplifier alone will consume a bias current larger than 10 nA at given process technology. Moreover, the amplified signal tends to make the output driver too strong, so that it again requires a series resistor to suppress higher tones. To address these issues, a pulsing scheme is implemented—the second key idea of the proposed circuit. The operational amplifier previously discussed is replaced with an inverter and a pulse generator (PG). Instead of prematurely turning ON the driver and perturbing the sinusoidal oscillation, the driver is turned ON only at each oscillation peak to regenerate energy only when it is needed. Precise timing is controlled by a DLL locked to the crystal's resonant frequency. Pulses can be generated at preferred timing with the DLL and these signals are used to separately drive

Fig. 5. Block diagram of the proposed circuit.

NMOS and PMOS drivers. For example, at oscillation maxima, the PMOS will turn ON briefly and clamp the oscillation's top voltage excursion level back to V_{DDL}. At minima, the NMOS will turn ON and clamp the bottom voltage level down to V_{SSL}.

The proposed scheme injects current when the XO node voltage is close to the low-supply voltages. Therefore, it can sustain stable oscillation without a series resistor and with a small voltage drop across the drive transistor, which reduces power dissipation of the driver. In addition, only one transistor of the driver is ON at a time while keeping V_{GS} of the other transistor reverse-biased. This removes any need for static bias current, thus significantly reducing the output driver power.

If DLL and pulse generation circuits are run in high-voltage supply, the power consumption in these circuits will become dominant and negate the benefit from lower driver power. Therefore, another voltage pair— V_{DDM} and V_{SSM}—in between high- and low-voltage supplies is introduced, which is referred to as the medium voltage supply. By keeping the medium-voltage supply at near-threshold level, power consumption of DLL and other circuits is kept low. Since the output driver still requires a high-amplitude signal at its input, level converters are implemented between the DLL/PGs and the driver stage. For converting the low-voltage crystal oscillation amplitude to the medium-voltage supply level, a body-biased inverter front end (FE) is used.

The block diagram and waveform for the resulting circuit is shown in Fig. 5. Overall, the circuit will maintain the oscillation as follows. Once the DLL is locked to the crystal's resonant frequency, the DLL generates a set of 32.768 kHz square waves with different phases. The circuit picks a pair of these square waves and produces a precise pulse with a predefined timing. Then, these pulses are applied at output driver to inject energy at oscillation peak and thereby sustain the oscillation.

As a result of the multitiered supply approach, four extra supply voltages are needed. For practical application, these

Fig. 6. Lumped model of crystal oscillator using pulsed driver.

voltages should be generated efficiently on-chip. In this circuit, an on-chip SCN is used to generate all needed voltage and the overall circuit operates from just one supply V_{DD} and ground.

IV. THEORY OF OPERATION

This section presents a more detailed explanation of the circuit operation and its behavior as a function of transistor size (ON-resistance), pulse width, and pulse location. The pulsed driver replaces an inverter in conventional circuit and provides 180° of phase shift. In fact, the output driver of the proposed circuit is identical to a regular inverter structure, although its operation is duty-cycled to achieve considerable power reduction. The crystal and load capacitance provide an additional 180° of phase shift, meeting the phase requirement for oscillation. Therefore, we will focus our discussion in this section on how energy is maintained through pulsed driver operation. Fig. 6 shows a theoretical model of a crystal oscillator using a pulsed driver. R_m, L_m, C_m, and C_p comprise the electrical model of a quartz crystal. C_{L1} and C_{L2} represent load capacitances that are assumed to be matched and equal. Note that the bias resistor that is present in Figs. 4 and 5 have been removed for simplicity since its only purpose is providing the
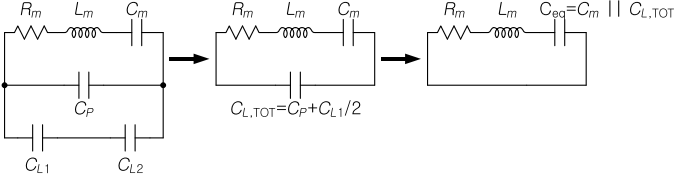
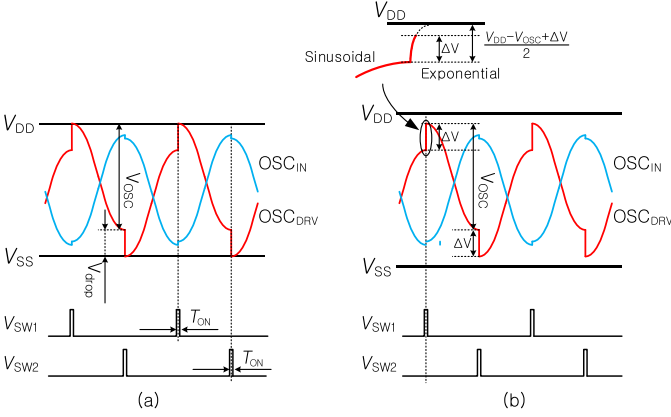Fig. 7. Simplified passive networks.

Fig. 8. Abstract waveforms of crystal oscillation. (a) Ideal switches. (b) Switches with non-zero on-resistance.

correct bias voltage at OSC_{IN}. At the oscillation peak, one of the two switches is turned ON for a duration of T_{ON}. Note that T_{ON} is centered at the peak voltage in this analysis. R_{SW} represents switch resistance. In a practical realization, the switch is implemented with a transistor, which will have a small drain-to-source voltage and will operate in the linear region, so the switch is well approximated by R_{SW}. Further, for simplicity, all voltages are measured in reference to V_{SS}.

For an initial analysis, we consider only the passive network and assume the switches are not operating (Fig. 7). The crystal is assumed to be resonating in steady state, with voltage at OSC_{IN} and OSC_{DRV}, each oscillating (180° out of phase to each other) with a peak-to-peak voltage of V_{OSC} due to this resonance. Reducing the two-load capacitors C_{L1}, C_{L2}, and C_p as $C_{L,TOT}$, we can see that the voltage across $C_{L,TOT}$ is oscillating at an amplitude of V_{OSC}. Now, we combine $C_{L,TOT}$ together with C_M as C_{eq}, which is given as

$$C_{eq} = C_m \| C_{L,TOT} = C_m \| (C_p + C_{L1}/2). \quad (1)$$

Resonance frequency F_{OSC} can then be approximated with reasonable accuracy as

$$F_{OSC} = \frac{1}{2\pi\sqrt{L_m C_{eq}}}. \quad (2)$$

At this condition, the oscillation amplitude of the voltage across capacitor C_m $V_{Cm,amp}$ is given by

$$V_{Cm,amp} = V_{OSC} \cdot \frac{C_{L,TOT}}{C_m}. \quad (3)$$

Oscillation amplitude for the current in inductor L_m $I_{Lm,amp}$ can be calculated by equating the maximum energy stored in the inductor to the maximum energy stored in the capacitor

$$I_{Lm,amp} = (V_{Cm,amp} + V_{CL,TOT,amp}) \cdot \sqrt{\frac{C_{eq}}{L_m}}$$
$$= V_{OSC} \cdot \left(1 + \frac{C_{L,TOT}}{C_m}\right) \cdot \sqrt{\frac{C_{eq}}{L_m}}. \quad (4)$$

Therefore, we can calculate average power loss from the crystal's resistive component P_{loss} and energy loss per cycle from this resistive component E_{loss} as

$$P_{loss} = 0.5 \cdot I_{Lm,amp}{}^2 \cdot R_m \quad (5)$$

$$E_{loss} = \frac{P_{loss}}{F_{OSC}} = \frac{1}{2 \cdot F_{OSC}} \cdot \frac{R_m C_{eq}}{L_m} \cdot \left(1 + \frac{C_{L,TOT}}{C_m}\right)^2$$
$$\cdot V_{OSC}{}^2 = \pi\sqrt{L_m C_{eq}} \cdot \frac{R_m \cdot C_{eq}}{L_m} \cdot \left(\frac{C_{L,TOT}}{C_{eq}}\right)^2$$
$$\cdot V_{OSC}{}^2 = \frac{\pi R_m C_{L,TOT}{}^2 V_{OSC}{}^2}{\sqrt{L_m C_{eq}}}. \quad (6)$$

In order to sustain a steady oscillation, the switches regenerate the energy lost during the oscillation, i.e., E_{loss} at a given oscillation amplitude must equal the energy delivered by the switches from the power supplies. Given an initial rail-to-rail oscillation of $V_{OSC} = V_{DD}$ and switches that are turned ON at oscillation peaks for a short duration, no energy is transferred to the passive network since there is no voltage across R_{sw}. However, on the following oscillation period, V_{OSC} will degrade by some voltage drop V_{drop}, resulting in $V_{OSC} = V_{DD} - V_{drop}$.

For an initial analysis, it is assumed that $R_{SW} = 0$ and T_{ON} is very short. When SW_1 is turned ON, it charges node OSC_{DRV} to V_{DD} instantly. Due to very narrow frequency bandwidth of $R_m - L_m - C_m$ connection, the inductor current is not perturbed significantly by this event. Therefore, current from V_{DD} flows into the capacitor network formed by C_{L1}, C_{L2}, and C_p. Seen from the switches, the equivalent input capacitance $C_{eq,sw}$ is given as

$$C_{eq,sw} = C_{L2} + (C_{L1}\|C_p). \quad (7)$$

One half cycle after this transition, SW_2 is turned ON to discharge OSC_{DRV} to V_{SS}. These switching operations cause the dc levels to shift as shown in Fig. 8(a) with minimal perturbation to the resonant behavior of the crystal (i.e., the current through L_m). Therefore, the voltage at the OSC_{DRV} node shows a dc shift of V_{drop} at each switching operation followed by a half sine wave with peak-to-peak amplitude of V_{OSC} as seen in Fig. 8(a).

These switching sequences cause a change in the energy level stored on $C_{eq,sw}$. We will refer to this change of energy in each oscillation cycle as E_{regen}. It can be calculated as follows:

$$E_{regen} = \frac{1}{2} \cdot C_{eq,sw} \cdot \left[V_{DD}{}^2 - (V_{DD} - V_{drop})^2\right]$$
$$- \frac{1}{2} \cdot C_{eq,sw} \cdot V_{drop}{}^2 = C_{eq,sw} \cdot (V_{DD} - V_{drop}) \cdot V_{drop}. \quad (8)$$

Steady state is reached when E_{regen} in (8) is equal to E_{loss} in (6), with V_{DD} in the equation replaced by $V_{OSC} = V_{DD} - V_{drop}$. For example, with $R_m = 30$ kΩ, $L_m = 10.2$ kH, $C_m = 2.3129$ fF, and $C_p = 1.5$ pF, $C_{L1} = C_{L2} = 20$ pF, $V_{DD} =$
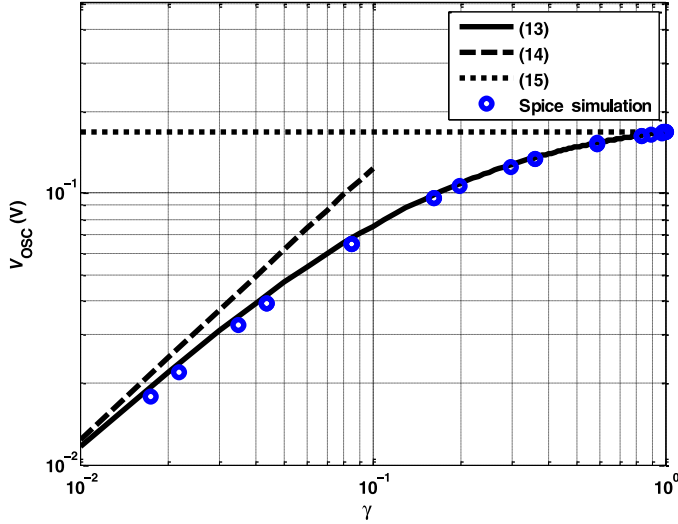
Fig. 9. Simulation and analytic solution of oscillation amplitude when $R_m = 30$ kΩ, $T_{\text{ON}} = 200$ ns, $L_m = 10.2$ kH, $C_m = 2.3129$ fF, and $C_p = 1.5$ pF, $C_{L1} = C_{L2} = 10$ pF, $V_{\text{DD}} = 180$ mV.
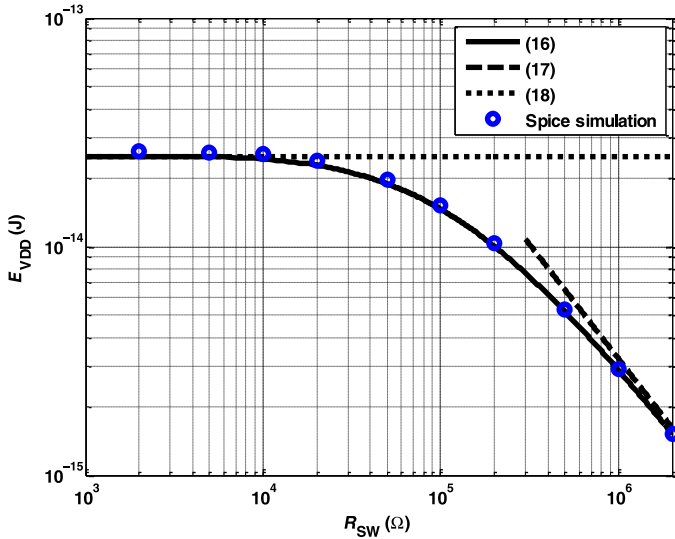
Fig. 10. Effect of R_{SW} on the energy consumption per cycle when $R_m = 30$ kΩ, $T_{\text{ON}} = 200$ ns, $L_m = 10.2$ kH, $C_m = 2.3129$ fF, and $C_p = 1.5$ pF, $C_{L1} = C_{L2} = 10$ pF, $V_{\text{DD}} = 180$ mV.

180 mV, V_{drop} and V_{OSC} are 19.3 and 160.7 mV, respectively. P_{loss} and E_{loss} are 2.17 nW and 66.3 fJ, respectively. For lower C_{L1} of 10 pF, V_{drop} decreases to 12.2 mV and P_{loss} reduces to 0.757 nW. At C_{L1} of 5 pF, V_{drop} is 8.7 mV and P_{loss} reduces to 0.299 nW.

While the inclusion of SW$_2$ effectively removes energy from the passive network, this process is essential to sustain the oscillation. With only SW$_1$ operating, the dc level of oscillation converges to V_{DD}. This makes the energy regeneration process via SW$_1$ less efficient, eventually causing the oscillation to diminish and cease completely. This would also pose a practical challenge, since the circuit would have a rising dc level of oscillation.

We now turn our attention to the energy supplied from V_{DD} ($E_{V\text{DD}}$) and regeneration efficiency ξ. Part of the supplied
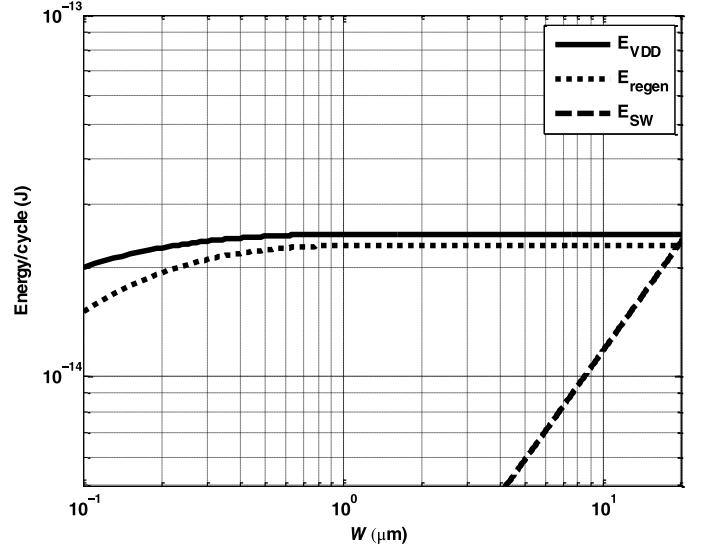
Fig. 11. Effect of W on the energy consumption per cycle when $R_m = 30$ kΩ, $T_{\text{ON}} = 200$ ns, $L_m = 10.2$ kH, $C_m = 2.3129$ fF, and $C_p = 1.5$ pF, $C_{L1} = C_{L2} = 10$ pF, $V_{\text{DD}} = 180$ mV.

energy is dissipated in R_{sw}, causing efficiency to degrade. These terms are calculated as follows:

$$
\begin{aligned}
E_{V\text{DD}} &= C_{\text{eq,sw}} \cdot V_{\text{DD}} \cdot [V_{\text{DD}} - (V_{\text{DD}} - V_{\text{drop}})] \\
&= C_{\text{eq,sw}} \cdot V_{\text{DD}} \cdot V_{\text{drop}} \tag{9}
\end{aligned}
$$

$$
\xi = \frac{E_{\text{loss}}}{E_{V\text{DD}}} = \frac{E_{\text{regen}}}{E_{V\text{DD}}} = \frac{V_{\text{DD}} - V_{\text{drop}}}{V_{\text{DD}}}. \tag{10}
$$

Note that although a larger V_{drop} leads to less E_{loss} in the crystal, it incurs more overhead in the circuit and leads to lower efficiency.

When the resistance of the switches is considered, the oscillation amplitude will be reduced as shown in Fig. 8(b). When the switches are OFF, OSC$_{\text{DRV}}$ makes a half cycle transition of V_{OSC}. Then, one of the switches is turned ON which charges or discharges the voltage by ΔV assuming the resistance of SW1 and SW2 are equal. As the inductor current is not significantly perturbed by the switching event, the capacitor network $C_{\text{eq,sw}}$ is connected to either V_{DD} or V_{SS} through the switch resistance R_{sw}. Therefore, the charging voltage ΔV can be expressed as an exponential curve as the following equation:

$$
\begin{aligned}
\Delta V &= \frac{V_{\text{DD}} - V_{\text{OSC}} + \Delta V}{2} \left(1 - e^{-\frac{T_{\text{ON}}}{R_{\text{SW}} C_{\text{eq,sw}}}} \right) \\
&= \frac{V_{\text{DD}} - V_{\text{OSC}} + \Delta V}{2} \gamma \\
\Delta V &= \frac{\gamma}{2 - \gamma} \left(V_{\text{DD}} - V_{\text{OSC}} \right) \\
&= \frac{1 - e^{-\frac{T_{\text{ON}}}{R_{\text{SW}} C_{\text{eq,sw}}}}}{1 + e^{-\frac{T_{\text{ON}}}{R_{\text{SW}} C_{\text{eq,sw}}}}} \left(V_{\text{DD}} - V_{\text{OSC}} \right) \\
&= \tanh \left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}} \right) \left(V_{\text{DD}} - V_{\text{OSC}} \right) \tag{11}
\end{aligned}
$$

where γ denotes the portion of the charged voltage. The regeneration energy per cycle E_{regen} can be found by subtracting the
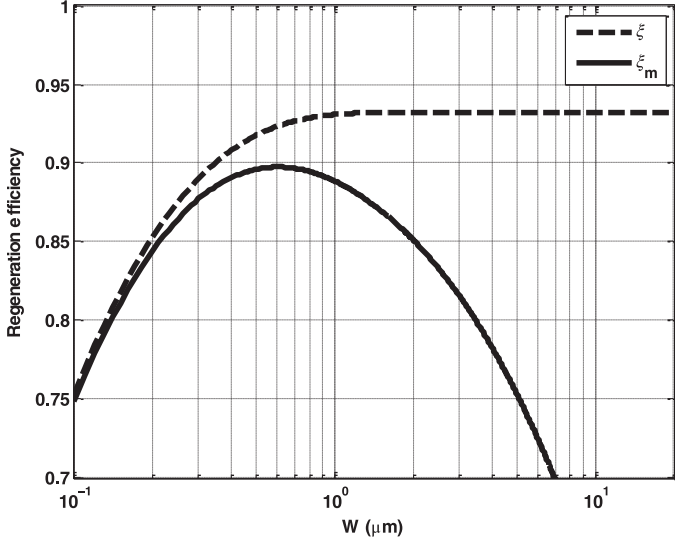
Fig. 12. Regeneration efficiency as a function of the driving transistor width.
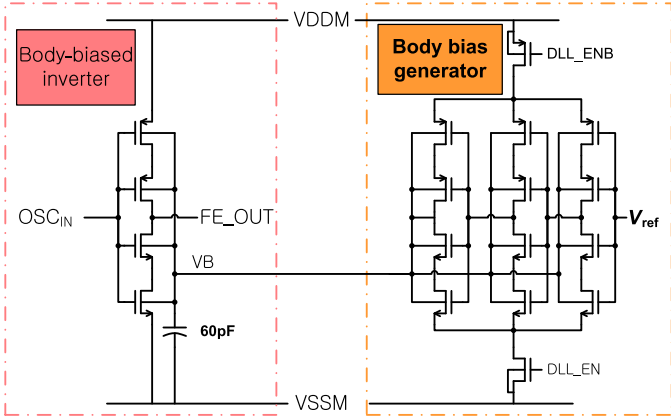

Fig. 13. FE block circuit schematic.

energy pulled from $C_{\text{eq,sw}}$ when SW2 is ON from the energy supplied when SW1 is ON as follows:

$$
\begin{aligned}
E_{\text{regen}} &= \frac{1}{2} C_{\text{eq,sw}} \left(\left(\frac{V_{\text{DD}} + V_{\text{OSC}} + \Delta V}{2} \right)^2 \right. \\
&\quad \left. - \left(\frac{V_{\text{DD}} + V_{\text{OSC}} - \Delta V}{2} \right)^2 \right) \\
&\quad - \frac{1}{2} C_{\text{eq,sw}} \left(\left(\frac{V_{\text{DD}} - V_{\text{OSC}} + \Delta V}{2} \right)^2 \right. \\
&\quad \left. - \left(\frac{V_{\text{DD}} - V_{\text{OSC}} - \Delta V}{2} \right)^2 \right) \\
&= C_{\text{eq,sw}} V_{\text{OSC}} \Delta V \\
&= \frac{\gamma}{2 - \gamma} C_{\text{eq,sw}} V_{\text{OSC}} \left(V_{\text{DD}} - V_{\text{OSC}} \right). \quad (12)
\end{aligned}
$$

Note that when $\gamma = 1$, $\Delta V = V_{\text{drop}}$ and (12) is the same as (8). E_{regen} is at the maximum of $C_{\text{eq,sw}} V_{\text{OSC}} (V_{\text{DD}} - V_{\text{OSC}})$ in this condition. As the regeneration energy is equal to the lost energy described in (6), V_{OSC} can be expressed as follows:

$$
\begin{aligned}
V_{\text{OSC}} &= \frac{\left(\frac{\gamma}{2 - \gamma} \right) C_{\text{eq,sw}}}{\frac{\pi R_m C_{L,\text{TOT}}^2}{\sqrt{L_m C_{\text{eq}}}} + \left(\frac{\gamma}{2 - \gamma} \right) C_{\text{eq,sw}}} V_{\text{DD}} \\
&= \frac{\tanh \left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}} \right) C_{\text{eq,sw}}}{\frac{\pi R_m C_{L,\text{TOT}}^2}{\sqrt{L_m C_{\text{eq}}}} + \tanh \left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}} \right) C_{\text{eq,sw}}} V_{\text{DD}}. \quad (13)
\end{aligned}
$$

Fig. 9 shows the simulated oscillation amplitude as a function of γ compares this to the analytic solution. Since $\tanh \left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}} \right)$ can be approximated as $T_{\text{ON}} / (2 R_{\text{SW}} C_{\text{eq,sw}})$ when $T_{\text{ON}} \ll R_{\text{SW}} C_{\text{eq,sw}}$, V_{OSC} can be approximated as follows:

$$
V_{\text{OSC}} \approx \frac{C_{\text{eq,sw}} \frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}}}{\frac{\pi R_m C_{L,\text{TOT}}^2}{\sqrt{L_m C_{\text{eq}}}}} V_{\text{DD}} = \frac{\sqrt{L_m C_{\text{eq}}} V_{\text{DD}}}{2 \pi R_m C_{L,\text{TOT}}^2} \cdot \frac{T_{\text{ON}}}{R_{\text{SW}} C_{\text{eq,sw}}}. \quad (14)
$$

Therefore, oscillation amplitude is inversely proportional to the switch resistance when R_{SW} is large. On the other hand, when $T_{\text{ON}} \gg R_{\text{SW}} C_{\text{eq,sw}}$, the switch resistance is small enough to maximize the amplitude, which is noted as the horizontal dotted line in Fig. 9:

$$
V_{\text{OSC,max}} = \frac{C_{\text{eq,sw}}}{\frac{\pi R_m C_{L,\text{TOT}}^2}{\sqrt{L_m C_{\text{eq}}}} + C_{\text{eq,sw}}} V_{\text{DD}}. \quad (15)
$$

The discussion to this point shows that the circuit in Fig. 6 differs from a conventional oscillator model where energy is regenerated by a transconductance amplifier. In the conventional model, regenerative current is proportional to oscillation amplitude, making it possible to model the active circuit as a negative resistance. This resistance has to overcome energy loss to maintain oscillation, thus setting a limit on the minimum transconductance the amplifier must provide. However, the oscillation amplitude in (13) shows that the circuit of Fig. 6 can theoretically maintain oscillation with any value of T_{ON}, R_{SW}, $C_{\text{eq,sw}}$, as long as $T_{\text{ON}} / (2 R_{\text{SW}} C_{\text{eq,sw}}) > 0$, which simply means that T_{ON} is positive. In the proposed circuit, regenerative current provided by switches will increase as oscillation voltage decreases. Therefore, it can eventually reach a steady-state oscillation with no theoretical limit, and cannot be modeled by a negative resistance. However, a *practical* limit in the proposed design still exists as it must be greater than the minimum oscillation amplitude that can be received as a DLL input with circuit noise present.

Continuing with original discussion, the energy provided by the supply while SW1 is ON can be calculated by multiplying V_{DD} with the charge supplied as the following equation:

$$
\begin{aligned}
E_{V\text{DD}} &= \int^{V_{\text{DD}}} i_{V\text{DD}}(t) \, dt = V_{\text{DD}} Q_{\text{DD}} \\
&= V_{\text{DD}} C_{\text{eq,sw}} \Delta V = \frac{V_{\text{DD}}}{V_{\text{OSC}}} E_{\text{regen}}. \quad (16)
\end{aligned}
$$

By combining (12), (14), and (16), $E_{V\text{DD}}$ can be expressed as the following equation when $T_{\text{ON}} \ll R_{\text{SW}} C_{\text{eq,sw}}$:
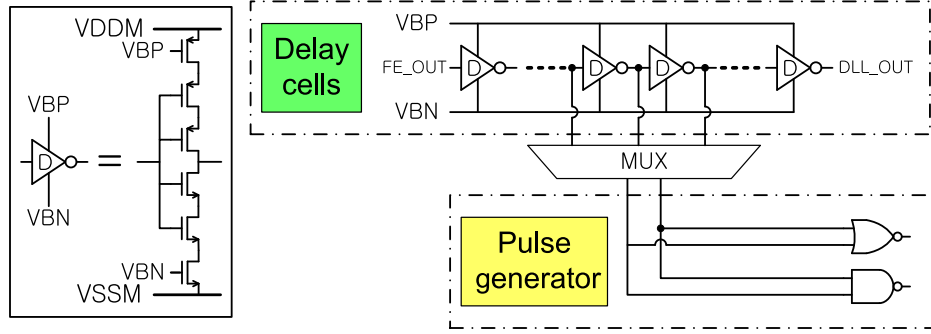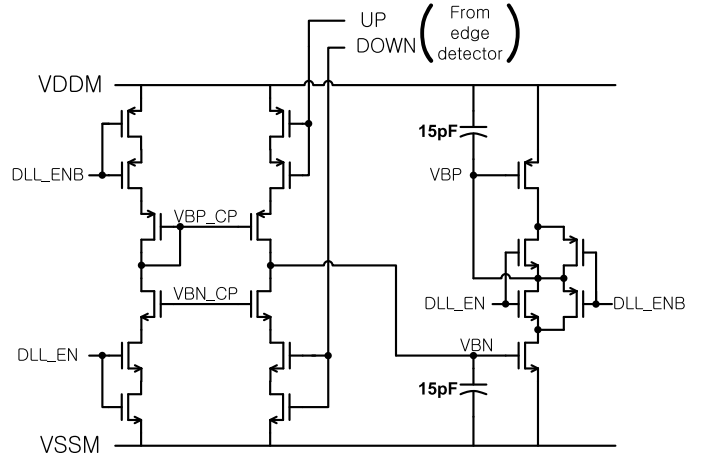
Fig. 14. DLL circuit schematic.
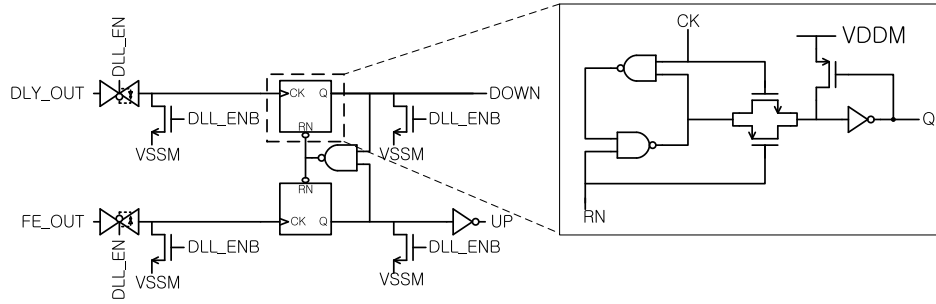
Fig. 15. Edge detector circuit schematic.

$$E_{V\text{DD}} = \frac{V_{\text{DD}}}{V_{\text{OSC}}} E_{\text{regen}} = \frac{V_{\text{DD}}}{V_{\text{OSC}}} \frac{\gamma C_{\text{eq,sw}} V_{\text{OSC}} (V_{\text{DD}} - V_{\text{OSC}})}{2 - \gamma}$$

$$\approx \tanh\left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}}\right) C_{\text{eq,sw}} V_{\text{DD}}^2 \approx \frac{T_{\text{ON}} V_{\text{DD}}^2}{2 R_{\text{SW}}}. \tag{17}$$

It can be seen that a large R_{SW} reduces the oscillation amplitude and thus, the amount of amplitude that needs to be regenerated ΔV is also reduced. On the other hand, when R_{SW} becomes small, both E_{regen} and V_{OSC} approach to their maximum, which can be derived by

$$E_{V\text{DD,max}} = \frac{V_{\text{DD}}}{V_{\text{OSC,max}}} E_{\text{regen,max}} = C_{\text{eq,sw}} V_{\text{DD}} (V_{\text{DD}} - V_{\text{OSC,max}})$$

$$= \frac{\pi R_m C_{L,\text{TOT}}^2 C_{\text{eq,sw}}}{\pi R_m C_{L,\text{TOT}}^2 + C_{\text{eq,sw}} \sqrt{L_m C_{\text{eq}}}} V_{\text{DD}}^2. \tag{18}$$

Fig. 10 shows simulated and analytic solution of E_{VDD} according to the switch resistance. Note that E_{VDD} is inversely proportional to R_{SW} when R_{SW} is large while it asymptotically approaches (18) when R_{SW} is small.

Now that we have computed both the E_{VDD} and $E_{\text{regen}} = E_{\text{loss}}$, the regeneration efficiency ξ can be found by taking the ratio between E_{regen} and E_{VDD} as follows:

$$\xi = \frac{E_{\text{regen}}}{E_{V\text{DD}}} = \frac{V_{\text{OSC}}}{V_{\text{DD}}}$$

$$= \frac{\tanh\left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}}\right) C_{\text{eq,sw}}}{\frac{\pi R_m C_{L,\text{TOT}}^2}{\sqrt{L_m C_{\text{eq}}}} + \tanh\left(\frac{T_{\text{ON}}}{2 R_{\text{SW}} C_{\text{eq,sw}}}\right) C_{\text{eq,sw}}}. \tag{19}$$

Fig. 16. Charge pump circuit schematic.

From this equation, it is clear that the maximum regeneration efficiency ξ_{max} is achieved when γ is equal to 1:

$$\xi_{\text{max}} = \frac{V_{\text{OSC,max}}}{V_{\text{DD}}} = \frac{C_{\text{eq,sw}}}{\frac{\pi R_m C_{L,\text{TOT}}^2}{\sqrt{L_m C_{\text{eq}}}} + C_{\text{eq,sw}}}. \tag{20}$$

Even though the energy consumption from V_{DD} is maximum when $\gamma = 1$, most of the energy is delivered to the crystal rather than dissipated in the switches.

However, to achieve this maximum regeneration efficiency, it is necessary that $R_{\text{SW}} \ll T_{\text{ON}}/C_{\text{eq,sw}}$. Since T_{ON} is limited to be a fraction of the oscillation period and $C_{\text{eq,sw}}$ is fixed, maximum efficiency requires R_{SW} to be reduced. However, the reduction of R_{SW} requires an increase in the size of the transistors which, in turn, increases the energy consumption for
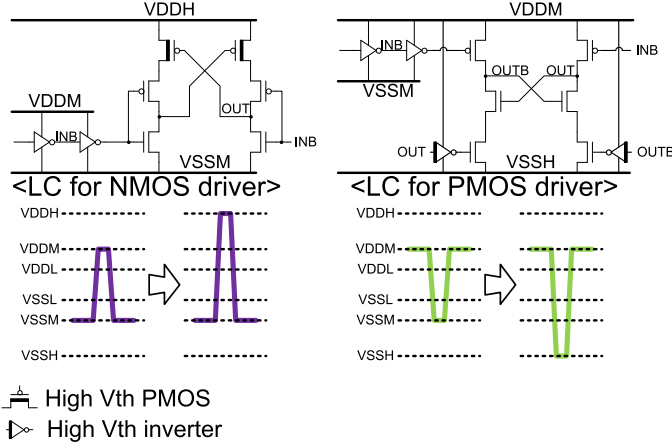
Fig. 17. Level converter circuit schematic.

switching those transistors due to their increased gate capacitance. The switches are in the linear mode when they are turned on and R_{SW} can be calculated by the following equation:

$$R_{SW} = \frac{L_n}{\mu_n C_{ox} (V_{gs} - V_{thn}) W_n} = \frac{L_p}{\mu_p C_{ox} (V_{sg} - |V_{thp}|) W_p} \tag{21}$$

where μ, C_{ox}, V_{th}, W, L, and V_{gs} are mobility, unit oxide capacitance, threshold voltage, transistor width, transistor length, and gate-to-source voltage, respectively. The gate capacitance C_{sw} is given by $C_{OX} \cdot W \cdot L$. Then, the energy consumed by the switching operation E_{SW} can be calculated by the following equation:

$$E_{SW} = (C_{swp} + C_{swn})V_{sw}^2 \tag{22}$$

where V_{SW} denotes the gate voltage swing of the transistors. Note that voltage boosting technique is used in this work, so that the V_{gs} and V_{SW} are different. More detailed information on the voltage boosting will be explained in Section V. Fig. 11 shows E_{VDD} and E_{SW} according to the transistor width when $R_m = 30 \text{ k}\Omega$, $T_{ON} = 200$ ns, $L_m = 10.2$ kH, $C_m = 2.3129$ fF, and $C_p = 1.5$ pF, $C_{L1} = C_{L2} = 10$ pF, $V_{DD} = 180$ mV, $\mu = 0.04$, $C_{ox} = 5$ fF/μm^2, $V_{gs} = 0.63$ V and $V_{sw} = 0.81$ V. As transistor width increases, R_{SW} reduces which causes E_{VDD} to approach $E_{VDD,max}$ and improves the regeneration efficiency. On the other hand, E_{SW} is proportional to W as shown in (22), which dissipates additional energy and degrades the overall regeneration efficiency. The modified regeneration efficiency ξ_m, shown in the following equation, is plotted in Fig. 12:

$$\xi_m = \frac{E_{regen}}{E_{VDD} + E_{SW}}. \tag{23}$$

Note that there exists an optimal transistor width W_{opt} that maximizes the regeneration efficiency. In this work, we numerically calculated $W_{opt} \approx 600$ nm using (12), (13), (16), (21), and (22) and the parameters given above.

Finally, it is worth briefly discussing the optimal duration of T_{ON} for completeness. Although we assumed above that it is beneficial to maintain $T_{ON} \gg R_{SW}C_{eq,sw}$, it is possible to operate the circuit with $T_{ON} < R_{SW}C_{eq,sw}$. However, if T_{ON}

is too large, the switch turns on well before the oscillation reaches its peak voltage. This induces a larger current to flow through the switch with a larger voltage across it. Therefore, the efficiency degrades as more energy is dissipated through the switches. The simulation result shows efficiency degradation as T_{ON} becomes larger than 3 μs, representing roughly 10% of the oscillation period.

V. IMPLEMENTATION DETAIL

In this section, the details of each block will be discussed. Most of the circuit operates from the medium-voltage supply, which includes the FE, DLL, and PG, and which forms the core of the system. After these circuit elements, the level converter and SCN will be explained.

Fig. 13 shows the FE block. Since the crystal oscillates as a sine wave within the low-voltage supply, the sine wave needs to be converted to square wave within medium-voltage supply for the DLL to work. Since the FE operates at a near-threshold voltage level, where the circuit is more prone to PVT variation, a simple inverter may not be able to generate a 50% duty-cycle square wave if either NMOS or PMOS is stronger than the other. However, the FE output needs to trip exactly in the middle of low-voltage supply, even with PVT variation. Therefore, a self-adaptive body-biasing technique is used for the FE [12]. The body-biased inverter will amplify the sine wave from the crystal while a separate body bias generator dynamically adjusts the body bias, so that trip voltage is set as required. However, the body-biased generator itself consumes more than a few nW of power if it runs continuously. Therefore, the body-biased voltage is held on an on-chip 60 pF capacitor and adjusted only twice every 32 cycles. If needed, the circuit configuration can be changed to recalibrate this value for 2 out of 32 cycles, 4 out of 32 cycles, 2 out of 16 cycles, or constantly. The test result in the next section was measured with fixed setting at 2 out of 32 cycles for all testing environments of voltage and temperature. The reference voltage is equal to mid-rail voltage of a medium-voltage supply pair, and it is generated on-chip using a stack of diode-connected transistors operating at low pW range. Additionally, a double-stacked inverter topology is used throughout the circuit, which helps to reduce power consumption by 46% for the FE block.

Fig. 14 shows the DLL block. Delay cells are made with current-starved inverters, double stacked to minimize any leakage. Then, a pair of outputs from the DLL is chosen by the multiplexer for the pulse generator (PG). Depending on which cells are chosen, the PG can be reconfigured to use appropriate logic gates, so that correct pulses can be sent to the drivers. The test chip in the next section was implemented without a closed-loop pulse controller. Therefore, it was tested with a fixed pulse setting having enough margin to enable reliable operation across all testing conditions. Fig. 15 shows the edge detector of the DLL. Instead of using a standard flip-flop (FF), custom cells have been designed to reduce the number of transistors from 36 in a standard cell FF to 13. Simulation results show that FF power is reduced by 55%. Similar to the body-biased generator in the FE, the edge detector will only operate periodically. This may cause concern about worse frequency
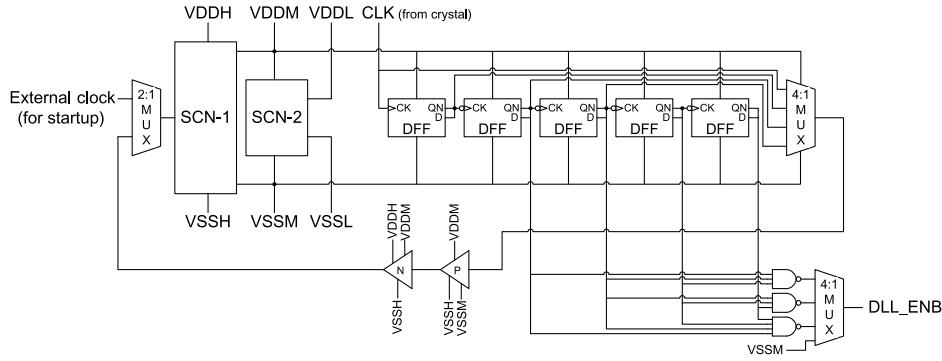
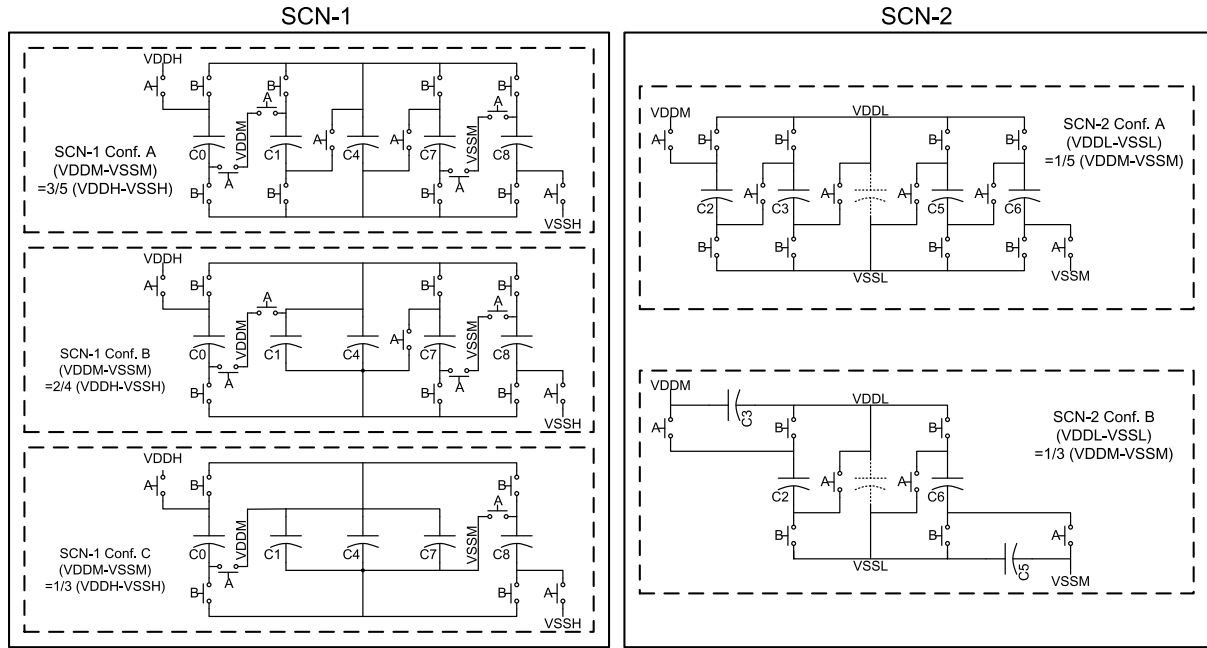Fig. 18. SCN block diagram.

Fig. 19. Detail of SCN for voltage generation. A and B refer to nonoverlapping clock pair. Dotted line represents decoupling capacitor.

stability. However, as it will be explained in the next section, the long-term stability does not show noticeable impact, due to innate frequency stability performance of the quartz crystal.

Fig. 16 shows the charge pump of the DLL. Similar to other parts shown previously, double stacking is used when needed, and the circuit operates periodically while relying on large capacitors to hold the bias voltage. Although not shown in the figure for simplicity, the bias voltage for the charge pump is also internally generated and it is assisted by on-chip capacitors.

Overall, when DLL and FE need to recalibrate their bias voltage, all the circuit parts previously explained will be activated. Measurement result confirmed that the circuit can sustain oscillation while running in this mode for only 2 out of every 32 cycles. Then, for the remaining 30 cycles, only blocks in the main signal path (FE, delay cells, and PG) operate to save power. The DLL_EN signal in Figs. 13, 15, and 16 is driven low for 30 cycles to minimize switching activity and store analog voltage on dedicated capacitors. Careful connection is required to retain analog voltage levels such as those of the cut-off transistors of the current mirror in Fig. 16. If the VBP node is connected directly to the drain of the PMOS transistor, its

voltage will leak when DLL_EN is low. In order to prevent this, additional cut-off transistors are added in between the drain and VBP node, so that it works as an ordinary current mirror for two cycles and then retains its voltage for 30 cycles.

Fig. 17 shows the level converter. The pulse generated from previous blocks is still in the medium-voltage supply. In order to have the low ON-resistance (i.e., R_{SW}), the pulse needs to be up-converted to the high-voltage supply level. Since the two pulses are sent to different types of transistors, the up-conversion requirement is different for each. For example, when the pulse for the NMOS driver is converted to high voltage, the maximum voltage is increased to V_{DDH}, whereas the minimum voltage level does not need to be changed since it is already lower than V_{SSL}. Similarly, the minimum voltage needs to be decreased to V_{SSH} for the PMOS pulse. To build a robust level converter with PVT variation tolerance, a new level converter is designed to reduce the contention between pull-up and pull-down path during transition. For the PMOS driver, a high-threshold voltage inverter acting as a delay element is inserted in the circuit to completely turn OFF the contention path during switching for more robust transition [13]. Once the level
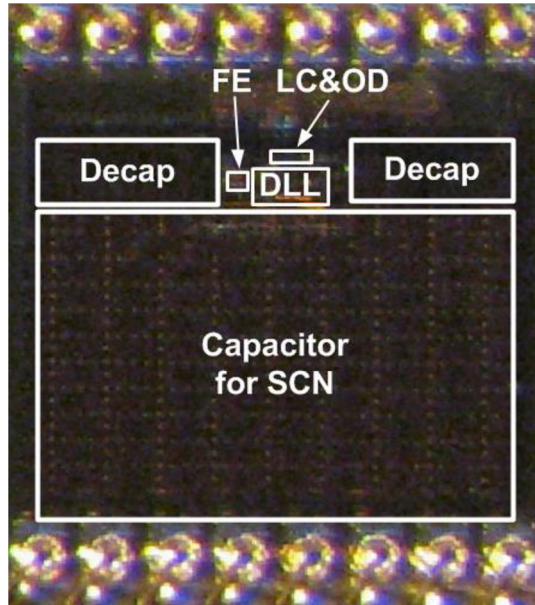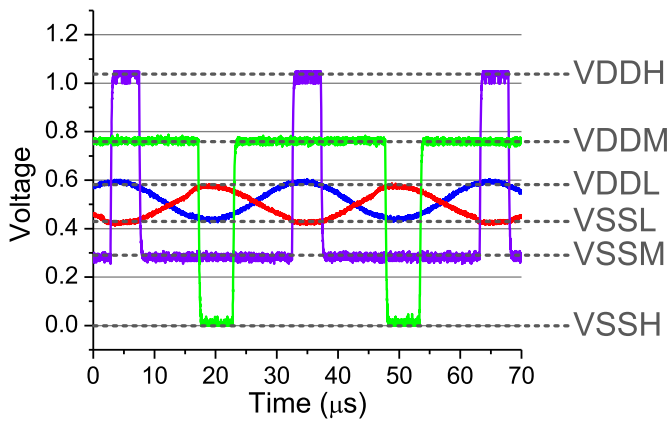
Fig. 20. Die photograph of the circuit.

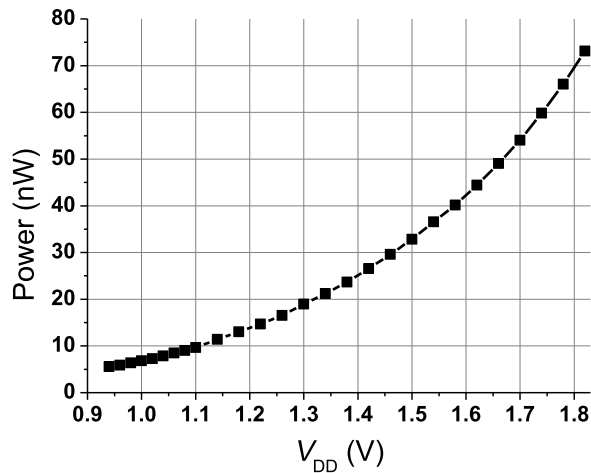Fig. 23. Measurement of normalized frequency at different pulse location.

Fig. 21. Measured waveform.
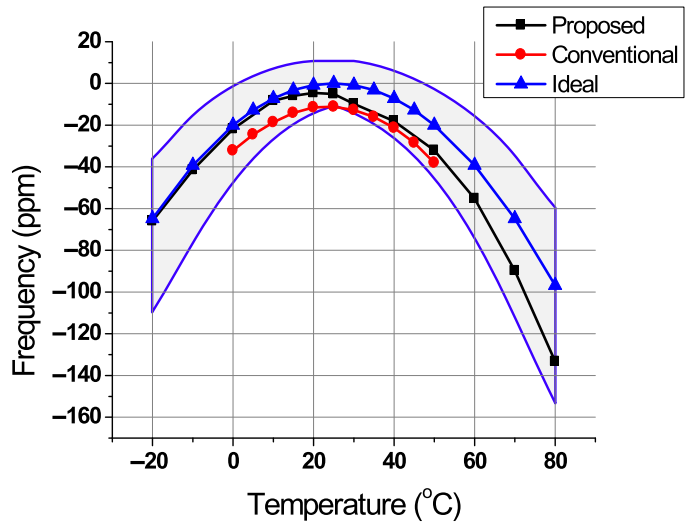
Fig. 24. Frequency at different temperature.

Fig. 22. Power at different power supply voltage.
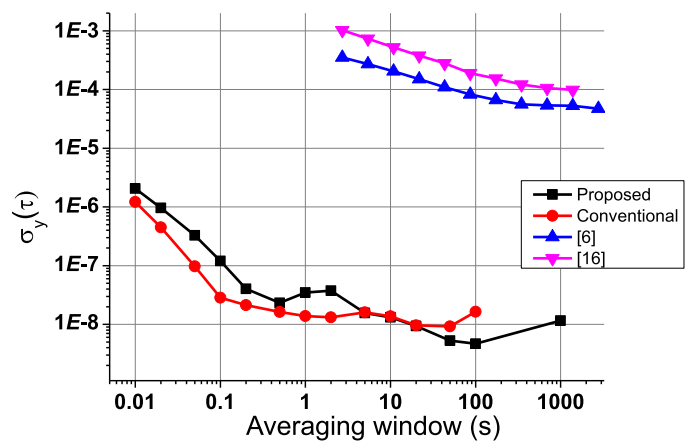
Fig. 25. Allan deviation measurement and comparison to prior ultra-low-power RTC.

conversion is done, this signal is applied to the gate terminal of output driver transistors.

As explained earlier, the circuit has its own SCN to generate the different voltage pairs required for each of the circuit blocks. A key constraint is performing this voltage generation without the conversion dominating the power consumption (i.e., maintaining high-conversion efficiency). Considering parasitic capacitance from switching components, higher SCN efficiency

is obtained using a larger switching capacitor that operates at a lower frequency, with the crystal's excellent frequency stability minimizing the effect from higher ripple in supply voltage. The SCN is operated using a 4.096 kHz signal, generated by dividing the crystal frequency by $8\times$ and level-converting to high-voltage supply level, as shown in Fig. 18. SCN-1 generates the medium-voltage supply pair from the high-voltage supply pair. Then, SCN-2 uses the medium-voltage supply to generate the low-voltage supply pair. SCN-1 and SCN-2 are designed to be reconfigurable to provide six different division ratios as shown in Fig. 19. Each capacitor is sized at 36 pF, and all supply-voltage nodes are decoupled by 100 pF capacitors. All the testing results in the following section were obtained using an SCN-1 division ratio of 2:1 (SCN-1 Conf. B) and an SCN-2 division ratio of 3:1 (SCN-2 Conf. B). The SCN consumes 0.463 nW in this configuration operating from 4.096 kHz clock signal. It requires 3.04 nW when operated from 32.768 kHz clock signal. The SCN is responsible for 80% of the chip area in the test chip introduced in the next section. This area could be reduced with slight reduction in power efficiency and using a fixed conversion ratio. This overhead can further be reduced if this circuit is implemented as part of a battery-operated sensor node system such as [4], where some voltage levels are readily available with the system's own SCN. Before the crystal starts to oscillate, the SCN requires a separate clock source during start-up to establish the needed output voltage levels. Although not implemented in the test chip, a simple ring oscillator can be used as a start-up clock to perform this task, after which it could be power gated with negligible leakage.

A triple well was used in the circuit implementation. Since the V_{SS} voltage for certain parts of the circuit is above the substrate ground level, these circuits will have negative body bias without the use of a triple well. This increases the threshold voltage of the transistors and makes it necessary to use a larger supply voltage for stable operation, resulting in increased power consumption. Hence, a triple well was used for all circuits which had a virtual ground higher than the substrate voltage to avoid unintentional biasing of the body nodes.

For the crystal to start the oscillation, the conventional inverter-based circuit is implemented in parallel to the proposed circuit. At the same time, SCN requires a separate clock signal during the start-up sequence since its clock signal during normal operation is generated from the circuit operating from the voltage generated by SCN. For this implementation, an external clock signal was provided for ease of testing. Once SCN output voltage is established and the crystal starts to oscillate using the conventional inverter based circuit, SCN clock signal is internally generated from the clock dividers. At this point, both the conventional start-up circuit and external clock signal can be safely removed and the proposed circuit can maintain the oscillation. The external clock signal can potentially be replaced by using a clock signal multiplexer and using the conventional inverter circuit's output during start-up.

VI. MEASUREMENT RESULT

The proposed circuit was fabricated in 0.18 μm CMOS technology with a triple well. Fig. 20 shows the die photograph of

TABLE I
PERFORMANCE SUMMARY

Minimum power consumption	5.58 nW
Operating temperature tested	−20ºC to 80ºC
Frequency drift within testing temperature	−4.56 ppm to 133.3 ppm
Supply voltage dependence	30.3 ppm/V
Allan deviation at 1000 s averaging window	1.16×10^{-8}

the implemented circuit. The total area is 0.3 mm. The chip was wire-bonded on a ceramic PGA package of size 37 mm × 37 mm. The chip was mounted on PCB and connected to crystal and explicit 5 pF capacitors at each node of the crystal. Authors expect the load capacitance to be in range 10–20 pF with this measurement setup. Fig. 21 shows the measured waveform and displays the pulsing scheme at each oscillation cycle. The OSC_{IN} and OSC_{OUT} voltage waveforms deviate very slightly from an ideal sinusoid due to the current injection of the output driver. As a result, these nodes voltages contain harmonics which could have impact on the jitter performance of the circuit. Based on the measured Alan deviation, this impact appears to be small or negligible although further study of this issue is needed.

The power consumption of the complete circuit, including on-chip voltage generation by the SCN, at different input power supply voltages (V_{DDH}) is shown in Fig. 22. As expected, the curve shows a quadratic dependence on voltage and a minimum power of 5.58 nW was observed at room temperature. At this point, SCN is configured to generate $V_{DDM} - V_{SSM} = 0.47$ V and $V_{DDL} - V_{SSL} = 0.16$ V. For the remainder of the test result such as the temperature sweep, an input supply voltage of $V_{DDH} = 1.08$ V was used, which had a power consumption of 9.05 nW and $V_{DDM} - V_{SSM} = 0.54$ V and $V_{DDL} - V_{SSL} = 0.18$ V when not loaded. All supply voltage pairs are centered at half the voltage of V_{DDH}, giving $V_{DDM} = 0.81$ V, $V_{DDL} = 0.63$ V, $V_{SSL} = 0.45$ V, and $V_{SSM} = 0.27$ V if unloaded. Measured frequency at this setup was 32767.83 Hz at 25 °C. This frequency is slower by 5.07 ppm from ideal frequency of 32768 Hz, but still within the normal process variation of the crystal.

The experimental results in Fig. 23 show the frequency change under different supply voltage variation and pulse location. *Normal* in Fig. 23 means the pulse was generated centered at the oscillation minima and maxima, as shown in the measured waveforms in Fig. 21. *Early* is the case when the pulses were generated before the oscillation peak, and *late* is the case when the pulses were generated after the oscillation peak. *Full* means the pulses were generated while centered at the oscillation peaks with a three times wider pulse width. The graph shows frequency change normalized to frequency with normal pulse at supply voltage of 1 V. The circuit shows 30.3 ppm/V over 0.94–1.2 V. Within 10% of the supply voltage at 1.08 V, the frequency drift is approximately 7 ppm, which is small compared to the innate temperature variation of the crystal from −20 °C to 80 °C. In comparison, the conventional circuit which has only one inverter and power consumption in μW range is 1.89 ppm/V. Fig. 23 shows that pulse location and width affect oscillation frequency by only a

TABLE II
COMPARISON TO OTHER WORKS

	[9]	[18]	[6]	[17]	[19]	[14]	This work
Technology	2 μm	2 μm	130 nm	130 nm	65 nm	28 nm	180 nm
Area (mm²)	N/A	N/A	0.015	0.019	0.015	0.0028	0.3
Original work published	1999	1994	2012	2009	2014	2014	2012
Architecture	Amplitude-regulated crystal oscillator		CMOS-based timer			Pulsed driver crystal oscillator	
Frequency (kHz)	32.768	32.768	3.7–14 Hz	11 Hz	32.768	32.768	32.768
Reported supply voltage (V)	0.71–2.6	1.1–2.2	0.65–0.75, 1.15–1.25	0.55–0.6	1.15–1.45	0.15–0.5	0.94–1.82
Tested temperature (°C)	N/A	0 to 50	−20 to 80	0 to 90	−20 to 90	−20 to 80	−20 to 80
Power consumption (nW)	27	220	0.66	0.15	190	1.89	5.58 (with SCN)
Allan deviation floor	N/A	N/A	$< 5 \times 10^{-5}$	$< 10^{-4}$	$< 4 \times 10^{-6}$	$< 10^{-8}$	$\sim 10^{-8}$

few ppm. This shows that the circuit can maintain acceptable frequency performance even if DLL performance degrades. This suggests that possible simplifications can be made to the pulse generation: trading off accuracy of the pulse position for reduced power consumption as has been exploited successfully in a more recent work [14] using a similar approach to this work [15].

Fig. 24 shows the frequency dependence on temperature. The innate frequency characteristic of the crystal itself is shown in the blue line, as specified by the crystal's datasheet [16]. The shaded region marks the specification boundary due to process variation of the crystal itself. The solid black line shows the result of the proposed circuit. The graph shows that the circuit remains well within the specification boundary. Shown in the red line is the conventional circuit result.

To use this circuit as a real-time clock in wireless sensor node, long-term frequency stability is of the utmost importance. Shown in Fig. 25 is the Allan deviation of the proposed circuit and the conventional inverter-based XO circuit. The red line shows the measurement result of the proposed circuit, and the black line is the measured result of the conventional inverter-based crystal oscillator operating at 32.768 kHz. The proposed circuit experiences Allan deviation of approximately 10^{-8} over a 1000 s time window. This translates into 36 μs of random error in an hour, which causes an average overhead of 10 pW due to timer mismatch in the scenario discussed in Section I and shown in Fig. 1. The result shows that the circuit maintains stability performance needed for a WSN. For comparison, Allan deviation measurement results for ultra-low-power silicon-based timers are shown [6], [17]. They have approximately one order of magnitude lower power consumption (0.15 nW for [17] and 0.66 nW for [6]) as the

proposed circuit (5.58 nW) but four orders of magnitude worse frequency stability performance than the proposed circuit.

Tables I and II show the performance summary, along with comparison to other crystal oscillator works [9], [14], [18] and low-power CMOS-based timers [6], [17], [19]. The proposed circuit achieves 4.84× lower minimum power than [9]. The power includes on-chip SCN and divided clock signal generation at full-supply voltage level.

VII. CONCLUSION

A new XO architecture was proposed which uses low-voltage supply to keep small oscillation amplitude and high-voltage supply for strong drivers. To the authors' best knowledge, this work is the first to use pulsed input to the driver to sustain the oscillation of the quartz crystal. Together with the pulse injection scheme realized by DLL, the power could be reduced to 5.58 nW, which is 4.84× lower than the previous work. It shows a wide-operating supply voltage of 0.94–1.82 V with supply voltage dependence of 30.3 ppm over 0.94–1.2 V. Frequency measurement from −20 °C to 80 °C shows that the circuit does not degrade the excellent frequency performance of the quartz crystal. The long-term frequency stability performance is confirmed by Allan deviation of 1.16×10^{-8} and meets the requirement for WSN application.

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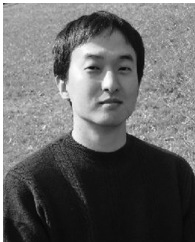
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