A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V

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***Abstract*—Sensing systems such as biomedical implants, infrastructure monitoring systems, and military surveillance units are constrained to consume only picowatts to nanowatts in standby and active mode, respectively. This tight power budget places ultra-low power demands on all building blocks in the systems. This work proposes a voltage reference for use in such ultra-low power systems, referred to as the 2T voltage reference, which has been demonstrated in silicon across three CMOS technologies. Prototype chips in 0.13 μm show a temperature coefficient of 16.9 ppm/°C (best) and line sensitivity of 0.033%/V, while consuming 2.22 pW in 1350 μm². The lowest functional V_{dd} is 0.5 V. The proposed design improves energy efficiency by 2 to 3 orders of magnitude while exhibiting better line sensitivity and temperature coefficient in less area, compared to other nanowatt voltage references. For process spread analysis, 49 dies are measured across two runs, showing the design exhibits comparable spreads in TC and output voltage to existing voltage references in the literature. Digital trimming is demonstrated, and assisted one temperature point digital trimming, guided by initial samples with two temperature point trimming, enables TC < 50 ppm/°C and ±0.35% output precision across all 25 dies. Ease of technology portability is demonstrated with silicon measurement results in 65 nm, 0.13 μm, and 0.18 μm CMOS technologies.**

***Index Terms*—Low power, process variations, ultra low power, voltage reference, 2 transistor voltage reference.**

I. Introduction

THERE is a growing interest in environmental and biomedical sensor applications today. These systems often include analog and mixed-signal modules such as linear regulators, analog-to-digital converter (ADC), and radio frequency (RF) communication blocks for self-contained functionality. Voltage references are key building blocks for these modules.

However, integrating voltage references in such sensing systems poses severe design challenges. Since sensing systems often need to consume 100 s of nanowatts or less (in modes not involving RF communication) due to limited energy sources, voltage references, as well as other modules, need to consume very little power. One example is the use of such references in voltage regulators that operate during nW or pW-level sleep modes. The area should be minimized as well, particularly for implantable biomedical applications where smaller device size translates to less invasive surgeries. These restrictions are exacerbated when multiple voltage references are integrated in a system. Additionally, these voltage references can ideally operate across a wide range of supply voltages, in particular sub-1V, since power sources such as energy scavenging units typically provide only low output voltages.

There are several approaches to designing voltage references in CMOS technology [1]–[18]. The most common method is a bandgap voltage reference using parasitic BJTs (bipolar junction transistors) [1]–[4]. To generate a temperature insensitive output voltage, bandgap references linearly combine two voltages with opposing temperature characteristics: a complementary-to-absolute-temperature (CTAT) voltage and a proportional-to-absolute-temperature (PTAT) voltage. Another method combines PTAT and CTAT *currents*, rather than voltages, to generate a temperature-independent output voltage [5]–[8]. Voltage references can also be designed by employing two devices of different threshold voltages, which can be implemented by distinct gate doping [9] or selective channel implantation [10], [11]. Alternatively, one can achieve a stable output voltage based on the finding that the weighted difference between gate-source voltages of two complementary metal-oxide silicon (CMOS) transistors is temperature insensitive [12]. Another approach uses subthreshold-biased transistors to lower minimum functional supply voltage and power consumption [13]–[15]. Finally, storing and refreshing a voltage at a floating node can be used to supply a reference voltage [16], [17].

However, these voltage references do not meet the demanding low power consumption, small design area, and low functional supply voltage requirements of miniature sensing systems. Recently published ultra-low power (ULP) designs consume as little as tens of picowatts during standby mode, and hundreds of nanowatts in active mode [19]–[22]. Therefore, voltage references in these systems should consume only a fraction of these power levels. Also, voltage references that are functional over a wide range of supply voltage, including sub-1V, are preferred as they can be used with energy harvesters, which often provide low output voltages [23]. Table I summarizes the performance characteristics of existing voltage reference designs. Only a few designs offer power consumption in the range of nanowatts, while most consume ≥ 1 μW. Additionally, most prior designs fail at supply voltages below 0.8 V. Fig. 1 illustrates the power consumption and design

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TABLE I
RECENT PUBLISHED DESIGNS OF LOW POWER VOLTAGE REFERENCES

Design	MinV_{dd}[V]	Power at Room Temp (RT)	TC [ppm/°C]	LS [%/V]	Area [mm^2]	Tech.
Annema et al. [2]	0.9	12.6µW	962	n/a	0.016	32nm
Leung et al. [5]	0.98	17.6µW	15	3.6	0.24	0.6µm
Doyle et al. [6]	0.95	10µW	17, post trim	n/a	1.09	0.5µm
Boni et al. [7]	0.85	9µW	33	4.4	n/a	0.18µm
Banba et al. [8]	2.1, 0.84(sim)	4.6µW at 2.1V	116	0.1	0.1	0.4µm FLASH
Oguey et al. [9]	2	<2µW	300 30, post-trim	n/a	n/a	CMOS
Ugajin et al. [10]	0.6	100µW at 1V	37.7	n/a	0.06	SIMOX
Leung et al. [12]	1.4	29.1µW at 3V, 100°C	36.9	0.012	0.055	0.6µm
Vita et al. [13]	0.9	36nW	10	0.27	0.045	0.35µm
Giustolisi et al. [14]	1.2	4.3µW	119	n/a	0.23	1.2µm
Annema [15]	0.85	1.02µW	57	n/a	0.063	0.35µm
Huang et al [16]	1.0	0.25µW	16.9	0.76	0.049	0.35µm
Tanaka et al. [17]	3.3	<3.3µW (standby)	372	8.3	0.044	DRAM
Kinget et al [18]	0.55	398µW	270	12.1	0.019	90nm
Kinget et al [18]	0.55	482µW	150	20.7	0.07	90nm
Magnelli et al [33]	0.45	2.6nW at 0.45V, RT 32nW at 1.8V, 80°C	165 (average over 40 dies)	0.44	0.043	0.18µm
Lee et al [34]	0.7	0.22µW	29.3 (average over 12 dies)	0.0337	0.023	0.13µm
Ivanov et al [36]	0.75	0.17µW	40 (typical)	0.005	0.07	0.13µm
B. K. Ahuja et al [37]	2.7V	2.5 µW at 5V	<1	<0.002	1.6	1.5 µm EEPROM
G. Ge et al [38]	1.8V	99µW	5-12, post trim, 61 dies	0.029	0.12	0.16µm
Annema et al [41]	1.1V	1.54µW	30	n/a	0.0025	0.16µm
This work, 2T	0.5	2.2pW at 0.5V, RT 243pW at 3.0V, 80°C	62 (average over 49 dies)	0.033	0.00135	0.13µm
This work, 2T Trimmable	0.5	29.5pW	5.3-47.4 post trim, 25 dies	0.036	0.0093	0.13µm

(Design area is not normalized to technology since many designs use non-minimum length devices for low power or other purposes.)

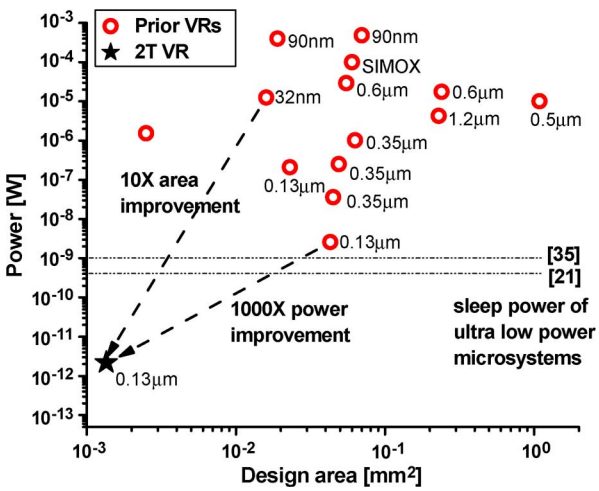

Fig. 1. Power and area comparisons of recently published voltage references.

area, which is another key metric for miniature sensors due to area/volume/cost constraints, of previously published voltage references.

Limits on power consumption, minimum functional supply voltage, and area all stem from the fact that most prior designs, including bandgap references, resort to amplifiers for error correction [1]–[11], [15], [16], [18]. Although amplifiers provide good temperature and supply voltage insensitivity, the associated power and area overhead is significant. Some recent designs avoid amplifiers [12]–[14], [17]; however they often rely on metal-oxide semiconductor field effect transistors (MOSFETs) in saturation mode, leading to significant power consumption. Both amplifiers and saturated devices require headroom, limiting supply voltage scalability. Additionally, many designs depend on the matching of integrated resistors to generate stable output voltages across temperature, which increases area in scaled processes [1]–[9], [12], [14], [15], [17], [18].

We therefore propose a voltage reference that avoids amplifiers, saturated devices, or resistors in order to meet the above requirements of power, area, and minimum functional V_{dd} [31]. Fig. 2 shows the proposed voltage reference using only two transistors, named the 2-Transistor (2T) voltage reference, which consumes as little as 2.2 pW at $V_{dd} = 0.5$ V and 25°C. This voltage reference reduces power consumption by >3 orders of magnitude compared to the previous state-of-the-art low power design [33] at typical conditions (minimum V_{dd} and room temperature). At $V_{dd} = 3$ V and 80°C, it consumes 243 pW, retaining >2 orders of magnitude power savings over existing nanopower voltage references at comparable voltage/tempera-

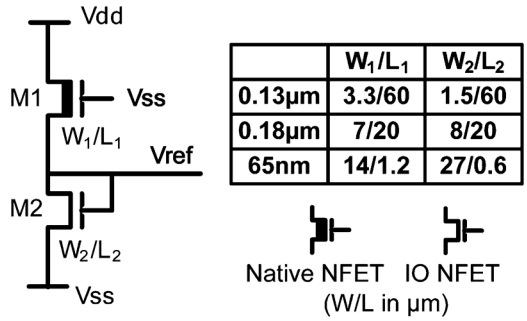

Fig. 2. Schematic of proposed 2T voltage reference.

ture points [13], [33], [34]. Due to this ultra-low power consumption, the proposed voltage reference need no duty-cycling for saving power, eliminating start-up issues. The design uses subthreshold-biased devices with distinct V_{th} levels, e.g., one regular thick oxide and one native device for achieving a stable output voltage. As a result, the number of fabrication masks is not increased.

Since semiconductor process variations lead to spreads in temperature coefficient (TC) and output voltage, we collected statistical results by measuring 49 2T voltage reference prototypes in two separate runs of 0.13 μm CMOS. These extensive measurement results provide a better understanding of the advantages and limitations of the proposed design. Measurement results indicate that the 2T voltage reference exhibits moderate spread in TC and output voltage due to die-to-die and run-to-run process variations. Such process sensitivity is typically addressed through trimming. However, trimming can be a time and cost intensive process [6]. We propose a digitally trimmable version of the 2T voltage reference to improve TC and output voltage accuracy across dies while enabling reasonable trim time and cost [32]. Measurements in 0.13 μm CMOS show that the proposed trimming enables tight distributions of TC and nominal output voltage across 25 dies. After one-temperature point digital trimming, TCs lie between 13.5 ppm/°C and 47 ppm/°C while the nominal output voltage varies by $\pm$0.35% from the mean value. The typical trimmable voltage reference consumes 29.5 pW at 0.5 V and 25°C.

We also propose several variants of the 2T voltage reference, including circuits to generate a specific output voltage, either higher or lower than its nominal value. We also demonstrate the 2T voltage reference with specific temperature dependence, PTAT or CTAT, in 0.13 μm CMOS. Technology portability is also investigated. Due the wide range of supply voltage scalability and simple topology, the proposed designs often involve only resizing of two transistors, facilitating its use as an intellectual property (IP) block across different technologies.

The remainder of this paper is organized as follows. Section II introduces the design of the proposed 2T voltage reference along with the governing equations for TC and line sensitivity (LS). Section III describes basic measurement results of the 2T voltage reference in 0.13 μm CMOS and compares to previous work. Section IV investigates the impact of process variations on the performance of the proposed 2T voltage reference with additional silicon measurement results. We also propose a assisted one temperature point trimming method, and show that it tightens the performance spread in silicon measurements. Section V introduces several variants of the 2T voltage references including measured results. Section VI demonstrates the easy portability of the 2T voltage references by providing measurement results in two additional CMOS technology nodes, while Section VII concludes the paper.

II. 2T Voltage Reference Design and Analysis

As mentioned above, the use of amplifiers and/or saturated MOSFETs is a key barrier to the scalability of power consumption and minimum functional V_{dd} in voltage references. Therefore, we seek to eliminate them while maintaining output insensitivity to temperature and supply voltage. To this end, we propose the 2T voltage reference shown in Fig. 2. Two different device types are used; in this case a native device for M1 and a thick oxide input/output (I/O) device for M2. The native device is identical to a standard MOSFET but has a near-zero V_{th}. Both devices have thick gate oxides to support a high V_{dd}. Native devices are widely available in modern foundry technologies [24], [25] and do not incur additional mask steps. One common use of native devices is to limit V_{ds} in thin oxide devices by connecting them in series, as shown in [26]. They have also been used in bandgap voltage reference circuits [8] and image sensors [27]. Although we use a native device for M1, any combination of two devices with a considerable V_{th} difference can be used for the 2T voltage reference. The required V_{th} difference is discussed later.

The output voltage V_{ref} can be modeled by (1), the well-known subthreshold current equation where μ is mobility, C_{ox} is oxide capacitance, W is transistor width, L is transistor length, m is subthreshold slope factor ($m = 1 + C_d/C_{ox}$ where C_d is depletion capacitance), V_T is thermal voltage (kT/q), V_{gs} is gate and source voltage, V_{th} is transistor threshold voltage, and V_{ds} is drain to source voltage. Setting the current through M_1 and M_2 equal leads to (2), which holds given that 1) both devices are in weak inversion, 2) V_{ds} for M_1 and M_2 is greater than 5–6 V_T, and 3) M1 follows the subthreshold current equation at V_{gs} down to $-V_{ref}$. The second condition relates to the minimum V_{ds} that ensures $<1\%$ loss of accuracy given that $1-\exp(-\chi)$ equals 0.982, 0.993, and 0.997 when χ is 4, 5, and 6, respectively. The third condition ensures that gate induced drain leakage (GIDL) is not significant at the operating point.

$$I_{sub} = \mu C_{ox}\frac{W}{L}(m-1)V_T^2\exp\left(\frac{V_{gs}-V_{th}}{mV_T}\right)\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{1}$$

$$\begin{aligned} I &= \mu_1 C_{ox1}\frac{W_1}{L_1}(m_1-1)V_T^2\exp\left(\frac{0-V_{ref}-V_{th1}}{m_1V_T}\right) \\ &= \mu_2 C_{ox2}\frac{W_2}{L_2}(m_2-1)V_T^2\exp\left(\frac{V_{ref}-V_{th2}}{m_2V_T}\right) \end{aligned} \tag{2}$$

$$V_{ref} = \frac{m_1m_2}{m_1+m_2}(V_{th2}-V_{th1}) + \frac{m_1m_2}{m_1+m_2}V_T\ln\left(\frac{\mu_1 C_{ox1}W_1L_2}{\mu_2 C_{ox2}W_2L_1}\right) \tag{3}$$

From (2), we obtain an analytical solution for V_{ref} as shown in (3), where both the first and second terms are either proportional or complementary to absolute temperature. Note that

MOSFET V_{th} is complementary to temperature [28]. By selecting the width and length of the two devices appropriately, the temperature dependence of the two terms can be set to cancel out and achieve temperature insensitivity. The design is also expected to offer good LS and power supply rejection ratio (PSRR) without the use of amplifiers or active current sources since all terms in (3) are insensitive to V_{dd} to first order. For example, $V_{th2} - V_{th1}$ is insensitive to V_{dd} when we use very long channel devices since the drain induced barrier lowering (DIBL) and other short channel effects become negligible. The use of long channel lengths also renders $m\ (= 1 + C_d/C_{ox})$ insensitive to V_{dd}, as the impact of drain potential becomes less important with longer channels. The log function also reduces the impact of the inner term $(\mu_1 C_{ox1} W_1 L_2/\mu_2 C_{ox2} W_2 L_1)$. M_1 decouples the output from the supply voltage, acting as a subthreshold cascode. We later demonstrate a version of the reference using submicron channel lengths as well.

$$\frac{dV_{\rm ref}}{dT} = 0 \rightarrow \left(\frac{W_1}{W_2}\right)_{opt} = \frac{\mu_2 C_{ox2} L_2}{\mu_1 C_{ox1} L_1} \exp\left(\frac{q}{k}(C_{Vth2} - C_{Vth1})\right) \quad (4)$$

Sizing of M_1 and M_2 in the 2T voltage reference targets the minimization of both power consumption and temperature sensitivity. The longest gate length $(L_1 = L_2 = 60\ \mu m)$ allowed by the process design rules can be used for both devices to achieve ultra-low power consumption, while shorter gate lengths can reduce area and drive lower impedance nodes at the expense of power. In simulations and silicon measurements, we confirm that the proposed voltage reference with $L = 60\ \mu m$ is able to drive transistor gate oxides. Widths ($W_1 = 3.3\ \mu m$, $W_2 = 1.5\ \mu m$) are chosen to minimize temperature sensitivity using the following procedure. First, we analytically approximate the optimal width ratio (W_1/W_2) by solving (4), namely $dV_{ref}/dT = 0$. We consider the first-order temperature dependency of V_{th} and V_T, while ignoring the temperature dependency of μ and m as well as the second-order temperature dependency of V_{th} to simplify the problem. Equation (4) shows the resulting optimal width ratio, where k is Boltzmann's constant and C_{Vth} is the first-order temperature coefficient of threshold voltages. The second-order temperature coefficient of threshold voltages is found to be more than 100× smaller than the first order coefficient, allowing it to be ignored without significant loss in accuracy. In the targeted 0.13 μm technology, the optimal width ratio is calculated as 2.17. We also perform an exhaustive simulation-based search for W_1 and W_2. As shown in Fig. 3 the carefully selected widths from simulations ($W_1 = 3.3$ and $W_2 = 1.5$), which are close to the calculated estimation, balance out the temperature-dependent terms of (3) and result in a very small residual temperature coefficient. The remaining temperature dependency from V_{th}, mobility, and subthreshold slope gives the V_{out}-vs.-temperature curve (in Fig. 7) a very shallow maximum.

A 0.8 pF output capacitor improves PSRR since coupling through the parasitic MOSFET capacitance can degrade PSRR. Simulated behavior in Fig. 4 shows that larger output capacitance improves PSRR. This output capacitor also reduces noise

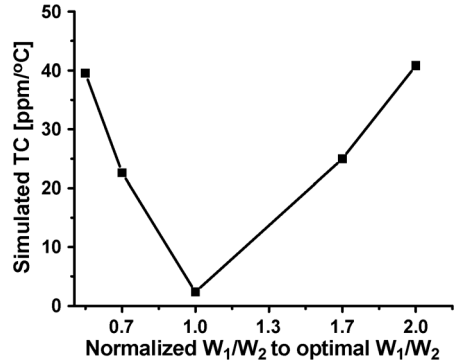

Fig. 3. Proper sizing of two transistors minimizes temperature dependency (simulated results).

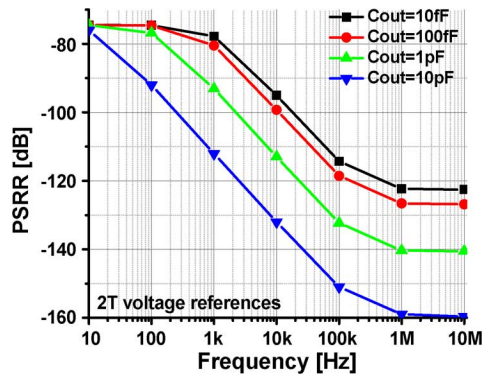

Fig. 4. A larger output capacitor provides better PSRR for 2T voltage references; schematics is shown in Fig. 2 (simulated results).

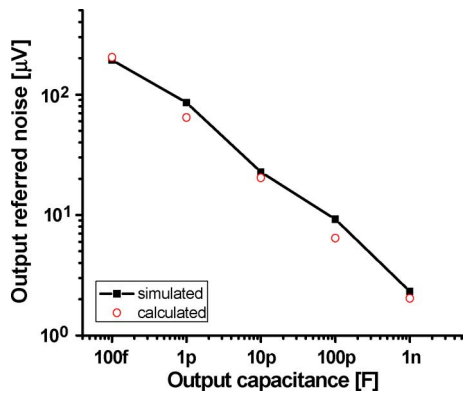

Fig. 5. Simulated output referred noise of a 2T voltage reference with different output capacitors.

on the output voltage. Since the subthreshold-biased devices exhibit large resistance, an output capacitor should be added to suppress thermal noise. The 1/f noise is less significant due to the use of large devices. Fig. 5 shows simulated results for output referred noise with different output capacitance values. The plot includes results from both SPICE simulation and RC-filter noise power $(P_{total} = kT/C)$ [29].

The minimum supply voltage of the reference is limited by whether V_{ds} of M_2 is larger than 5–6 V_T. Below this level (2) no longer holds since the final V_{ds} term in (1) cannot be neglected. The maximum supply voltage is set by reliability issues such as oxide breakdown. If necessary, diode-connected transistors

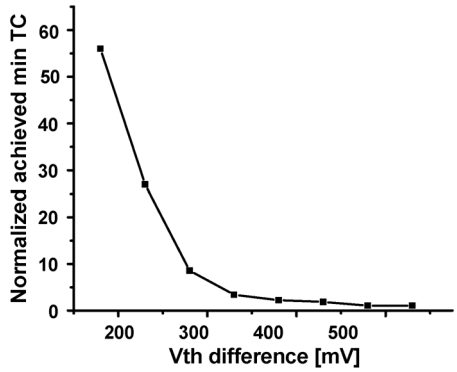

Fig. 6. Simulated required V_{th} difference to achieve a desired temperature coefficient of the 2T voltage reference.

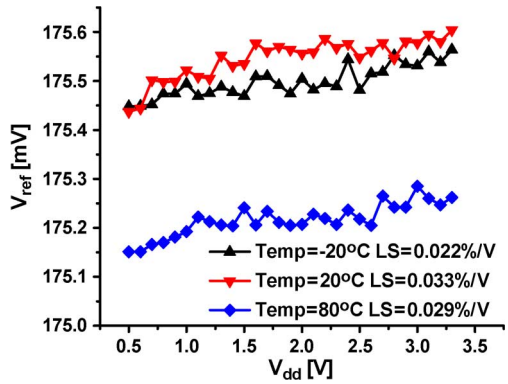

Fig. 8. Measured line sensitivity of the 2T voltage reference at three temperatures in 0.13 μm.

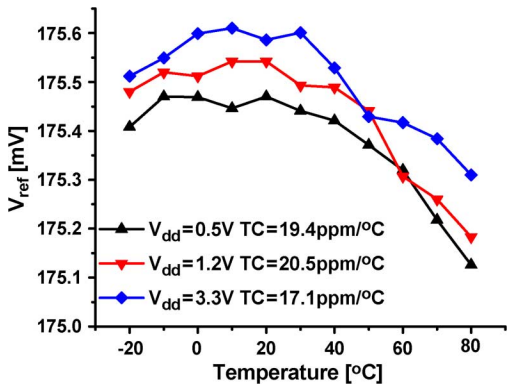

Fig. 7. Measured temperature coefficients of the 2T voltage reference at three supply voltages in 0.13 μm.

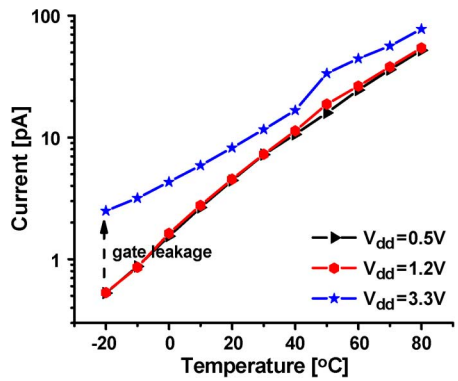

Fig. 9. Measured current consumption of the 2T voltage reference at three supply voltages in 0.13 μm.

can be added between V_{dd} and M_1 to increase the maximum allowable supply voltage.

Equation (3) implies a design constraint on the minimum difference of V_{th} between the two devices (M_1 and M_2). If we can neglect the second log term to the first order and assuming a typical subthreshold swing (90 mV/dec) for the two devices (i.e., $m_1 = m_2 = 1.5$), V_{ref} is approximately $0.75 \cdot \Delta V_{th}$ ((3)). Note that V_{ref} is equivalent to the V_{ds} of M_2, which should be larger than $\sim$5–6 V_T as shown above (to neglect the final V_{ds} term in (1)). Hence, the minimum V_{th} difference is approximately 6.6–8 V_T, or 170–200 mV at room temperature, for this type of voltage reference.

We performed SPICE simulations to confirm this analysis of the minimum required V_{th} difference. After modifying the V_{th} of M_1, we measure the degradation of temperature coefficient by sweeping device widths. Fig. 6 shows that the temperature coefficient, measured from $-20°C$ to $80°C$, degrades once the V_{th} difference becomes smaller than $\sim$250 mV. This is because the $(1-\exp(-V_{ds}/V_T))$ term in (1) cannot be ignored without a loss of accuracy. Since the maximum thermal voltage V_T in the range of $-20°C$ to $80°C$ is 33.6 mV, the simulated minimum V_{th} difference for proper operation is approximately 7.5 V_T, falling in the expected range.

III. Measurement Results in 0.13 μm CMOS

We fabricated a test chip in a standard 0.13 μm CMOS technology with no process options (thick oxide and native devices are offered in the standard process). The test chips are packaged in ceramic pin grid arrays (CPGA) [39]. Among 22 dies, the minimum TC[1] is 19.4 ppm/°C at 0.5 V with similar behavior across three different supply voltages (Fig. 7). We also fabricated a second test chip in the same technology, and a best TC of 16.9 ppm/°C is measured across these two separate runs with a total of 49 dies. In absolute terms, this equates to $\sim$ 35 μV/°C. Average TC is 62 ppm/°C with standard deviation of 41 ppm/°C across 49 dies ($\sigma/\mu = 0.66$).

Line sensitivity measurements are given in Fig. 8, showing that the output voltage changes by 0.033%/V. PSRR is measured to be -67 dB at 100 kHz. We use a 0.8 pF fingered, metal-to-metal output capacitor. Although the on-chip test circuits limit the measurement of PSRR for a wider frequency range, PSRR is expected to improve with frequency, since the 2T voltage reference acts as a low-pass RC filter, until a saturation point at high frequencies when the parasitic capacitances become pronounced. Fig. 16 confirms this intuition with measurements from the second run using an improved on-chip test setup along with simulation results. Due to the higher parasitic capacitance between the supply voltage node and the output in the trimmable version design (Fig. 12), PSRR degrades slightly.

Fig. 9 shows the current consumption for the 2T voltage reference. At 20°C and $V_{dd} = 0.5$ V, it consumes 2.22 pW. At the worst measurement conditions of 80°C and $V_{dd} = 3$ V, power

[1] $TC[\text{ppm}] = (\max(V_{ref}) - \min(V_{ref}))/V_{ref}(T = 20°C)/(80°C + 20°C) \times 10^6$

TABLE II
MEASUREMENT SUMMARY OF THE PROPOSED 2T VOLTAGE REFERENCE AND ITS VARIANTS

	2T			Trimmable	4T
Process	0.13μm CMOS	0.18μm CMOS	65nm CMOS	0.13μm CMOS	0.13μm CMOS
V_{dd}	0.5-3.0V	0.5-3.6V	0.5-2.5V	0.5-3.0V	0.5-3.0V
V_{out} (min) **V_{out} (max)**	174.9mV 178.7mV	326.8mV 330.0mV	327.2mV 333.0mV	175.2mV 176.5mV	341.5mV 348.1mV
TC (min) **TC (max)**	16.9ppm/°C 231ppm/°C	54.1ppm/°C 176.4ppm/°C	89.1ppm/°C 118.2ppm/°C	5.3ppm/°C 47.4ppm/°C	80.2ppm/°C 142.5ppm/°C
LS	0.033%/V	0.044%/V	0.33%/V	0.036%/V	0.036%/V
PSRR	-53/-62dB (100Hz/10MHz)	-49/-55dB (100Hz/10MHz)	-40/79dB (100Hz/10MHz)	-51/-64dB (100Hz/10MHz)	-58/-59dB (100Hz/100kHz)
Power **(V_{dd}, temp)**	4.4pA (0.5V,25°C) 81pA(3V,80°C)	11pA (0.5V,25°C) 139pA(3V,80°C)	0.48nA (0.5V, 20°C) 8.13nA (2.5V, 80°C)	59pA (0.5V,25°C) 847pA(3V,80°C)	21.7pA (0.5V, 25oC) 400pA (3V, 80oC)
Size	1350μm^2	1425μm^2	900μm^2	9300μm^2	3500μm^2
Comment	2 runs, 49 dies	1 run, 14 dies	1 run, 17 dies	Post-trimming 1 run, 25 dies	1 run, 30 dies

Design size includes output capacitors.

consumption is 243 pW. This picowatt power consumption is a first for voltage references to the best of our knowledge. The initial start-up time, defined as the time taken to reach stabilize within 1% of the final voltage level after power is supplied, is found to be 60 ms through simulations at room temperature with $\mathrm{L} = 60\ \mu$m and 1 ms with $\mathrm{L} = 0.36\ \mu$m.

We compare the proposed 2T voltage reference to recently published low power voltage references [2]–[10], [12]–[18], [33], [34] in Table I and Table II. Most significantly, power consumption is reduced by 1180× at room temperature with minimum operational supply voltage. At 80°C and maximum operating supply voltage (3 V) the 2T design still offers $> 130\times$ power reduction over prior art. As shown in Fig. 1, prior voltage references often exhibit comparable power consumption to full wireless sensing systems in active mode, adding significant power overhead. The proposed 2T voltage reference is feasible for use in these systems in both active and standby modes.

In addition, the 2T voltage reference can operate at supplies as low as 0.5 V since it requires no saturated devices and consequently less headroom. Although a higher supply voltage is often available from batteries or I/O pads, having a lower minimum functional supply voltage can help facilitate system design. Also, this attribute can be useful to avoid power overhead and design complexity of voltage up-conversion in systems depending on only energy scavenging units, which often generate low output voltages [23].

Even with this extremely low power consumption, the proposed design shows comparable or superior performance in many key figures of merit. For example, comparing to the lowest power voltage reference previously reported [33], the proposed design in 0.13 μm technology improves line sensitivity, PSRR, design area, and TC, while consuming two to three orders of magnitude lower power as summarized in Table I.

IV. VARIABILITY ANALYSIS AND TRIMMING

This section first investigates the impact of process variations on the voltage reference performance based on measurements across the previously mentioned 49 dies (i.e., the same parts described in Section III). We then propose a trimmable version of the 2T voltage reference to address such process variations, including measurements that demonstrate its efficacy.

A. Statistical Measurement Results

Process variation is an important consideration when designing voltage references since they require high precision in their output voltage and temperature coefficient. Although the voltage reference operates in the sub-$\mathrm{V_{th}}$ regime, where small process variations exponentially modulate subthreshold current, process variation impact on the 2T voltage reference is expected to be small due to 1) the linear effect of $\mathrm{V_{th}}$ on output voltage, and 2) the large device dimensions used, suppressing both geometric variations and $\mathrm{V_{th}}$ variation due to random dopant fluctuations.

We perform Monte-Carlo SPICE simulations to investigate the impact of process variations on output values. Transistor parameters such as $\mathrm{V_{th}}$, mobility, and subthreshold slope factor are simulated across random and global process variations. The use of the large devices successfully suppress random process variations, e.g. $\sigma/\mu(\mathrm{V_{th2}} - V_{\mathrm{th1}}) = 0.001$. Although transistor parameters vary more largely across global variations, the way each parameter is used in (3) and the correlation between two devices reduce their impact on output values. For example, $\sigma/\mu(\mathrm{V_{th2}})$ is as large as 0.2, but $\sigma/\mu(\mathrm{V_{th2}} - \mathrm{V_{th1}})$ is reduced to 0.05. Additionally, $\sigma/\mu(\mathrm{m_1 \cdot m_2/(m_1 + m_2)})$ and $\sigma/\mu(\mu_1 1/\mu_2)$ are simulated 0.014 and 0.09, respectively. In order to mitigate the impact of global variation, a careful selection of transistors is important. Since the output voltage is a strong function of $(\mathrm{V_{th2}} - \mathrm{V_{th1}})$ in (3), if the $\mathrm{V_{th}}$'s of the two devices track each other, it can reduce the impact of process variations. Compared to bandgap voltage references, the proposed voltage reference rely on less fundamental parameters, e.g. $\mathrm{V_{th}}$; hence we expect a lesser precision performance but find that our precision is still sufficient for many applications, while having significantly lower power.

To evaluate the tolerance of the 2T voltage reference to run-to-run and die-to-die process variations, we measured 49 prototype dies of the 2T voltage reference from two separate fabrication runs in 0.13 μm CMOS technology. Measured results for output voltage and temperature coefficient are plotted

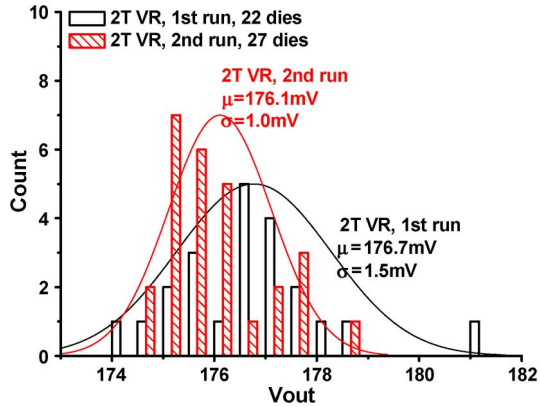

Fig. 10. Measured output voltage distribution of the 2T voltage references in two separate 0.13 μm runs.

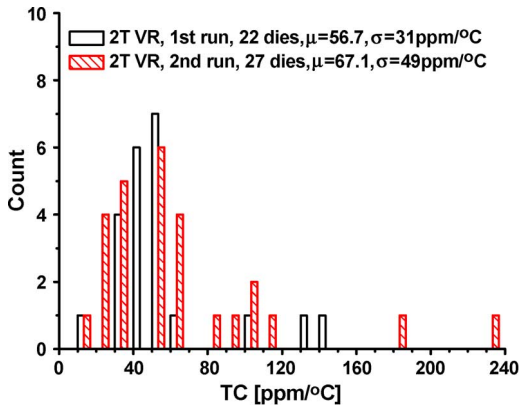

Fig. 11. Measured temperature coefficient distribution of the 2T voltage references in two separate 0.13 μm runs.

in Fig. 10 and Fig. 11, respectively. As shown in Fig. 10, the average output voltage shifted by 0.3% between the runs. Both runs show moderate spread in TC and output voltage due to die-to-die variations. Standard deviations of output voltage for each run are 1.5 mV and 1 mV, for average output voltages of 176.1 mV and 176.7 mV, respectively (cumulative $\sigma/\mu = 0.72\%$). These are reasonably tight distributions compared to past nanopower voltage references such as [33], which reported a σ/μ of 3.9% across 40 dies (two runs). Tighter distributions have been demonstrated by several bandgap references (e.g., [38]), pointing to a tradeoff between power consumption, voltage scalability and output voltage spread between these two types of designs. Temperature coefficient is more significantly impacted by variations; mean TCs from the two runs are 56 and 67 ppm/°C with standard deviations of 31 and 49 ppm/°C. These performance spreads can be further tightened using trimming, as described in the next section. However, pre-trim TC spreads are still smaller than those reported in other designs with a similar number of die measurements [33].

B. Digitally Trimmable 2T Voltage Reference

To minimize the TC and output voltage spreads, we designed a 2T voltage reference with digital trimming as shown in Fig. 12. The ratio of top-to-bottom device widths is critical to TC and

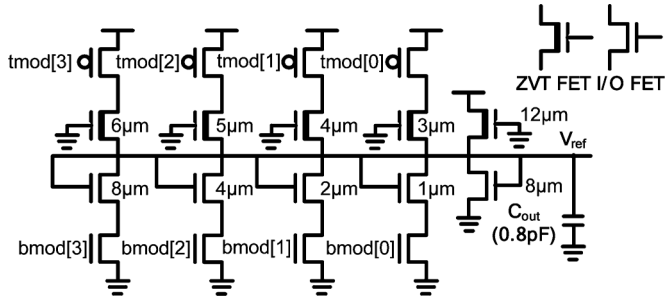

Fig. 12. Schematic of trimmable 2T voltage reference. (L = 60 μm is used.)

output voltage, as described in Section II. However, the optimal width ratio at design time may not be ideal for each manufactured chip due to process variations, making it beneficial to change the width ratio post-silicon. This voltage reference design can selectively turn the four top and four bottom devices on or off using associated switches. Bottom devices are binary-weighted for range and granularity, while top devices are sized up gradually from the minimum width constraint of native devices (3 μm). The base transistors (i.e. the transistors with no footer or header) are sized to allow sufficient granularity with the minimum width constraints. By applying control signals $bmod$ and $tmod$ to the switches, the top-to-bottom width ratio varies from 0.52 to 3.75 with 256 different settings. Control signals swing full rail, requiring no extra supply voltage. One-Time-Programmable (OTP) memories such as fuses can be used to provide the signals with minimal power overhead [30]. Once the switches are turned off, any top and bottom devices connected to them have negligible effect on the output voltage, acting as a dangling capacitor. Long transistors (L = 60 μm) are again chosen for minimizing power consumption; however L can be scaled to save area until power consumption and short channel effects become significant. Finally, a 0.8 pF output capacitor suppresses the effect of noise on output voltage.

Fig. 13 illustrates the measured TC and output voltage for different settings in the trimmable voltage reference in 0.13 μm CMOS. Fig. 13(a) shows the relationship between top and bottom device sizes to achieve minimum TC. A clear trend is observed where a specific width ratio leads to minimum TC, forming a diagonal line in the matrix. Likewise, output voltage changes at different settings and depends directly on the width ratio. This is again confirmed by the diagonal iso-V_{out} line in Fig. 13(b). Note that the width ratio leading to minimum TC also provides a consistent output voltage as sizing along the min-TC line in Fig. 13(a) provides an iso-V_{out} condition in Fig. 13(b).

C. Analysis and Minimization of Trimming Cost

Minimizing trimming time is critical to reduce testing costs, and can be achieved by reducing the number of temperature points and/or number of settings. Therefore, it is important to develop a trimming process that uses few temperature points and control settings while maintaining good post-trim performance.

One possible voltage reference design objective can be stated as: meet a specified TC constraint with minimum deviation from

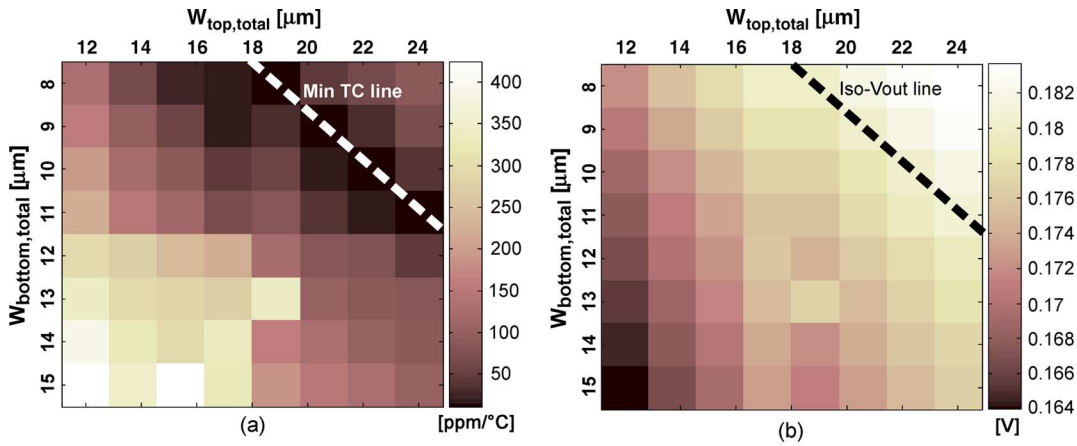

Fig. 13. Measured (a) TC and (b) output voltage dependency on trim settings.

the desired output voltage. In this experiment the goal of the trimming process is to minimize output voltage spread, which can also reduce the TC. The correlation between the output voltage and TC of a voltage reference is confirmed through SPICE simulations and silicon measurements. We target a TC of less than 50 ppm/°C and investigate single temperature point (80°C) trimming for the 25 dies to minimize time associated with trimming procedures. Since we cannot measure the TC with only one temperature point, the trimming process relies entirely on the output voltage.

The detailed trimming process is as follows. First, the output voltage of several dies is measured over various trimming settings at two temperature points (20°C, and 80°C). With this collected information, we set the target output voltage, which minimizes the spread of output voltages and TC among those initial samples. Simulation results are also used to increase confidence when estimating the target output voltage. After this initial step to set the target V_{ref}, we place the remaining dies in the temperature chamber at 80°C. Then, for each die, trimming controls are swept to find the optimal setting with output voltage closest to the target.

In order to save trimming time, all 24 dies can be tuned simultaneously to save time for thermal stabilization. If further time savings are desired, a subset of trimming combinations can be used as data is collected from earlier trimmed dies. We initially consider all possible combinations of control signals but only 16 configurations are sufficient to cover all cases based on our experiments. Finally, shorter length transistors can be used to reduce the settling time and testing cost.

After trimming, the voltage reference is tested at this chosen setting from −20 to 80°C in 10°C steps. As shown in Fig. 14, the trimming reduces the spread of TC and output voltage by 9.6× and 9.8×, respectively, compared to pre-trim results for the 25 dies. Fig. 15 gives a more detailed depiction of post-trim TCs and output voltages.

PSRR, LS, and power consumption are also measured for post-trim voltage references. Fig. 16 shows that PSRR ranges from −51 to −64 dB, which tracks simulation results well. Typical power consumption is 29.5 pW at 0.5 V, 25°C, and 2.5 nW at 3 V, 80°C. Output referred noise is investigated with SPICE simulations, as shown in Fig. 17. Together with a

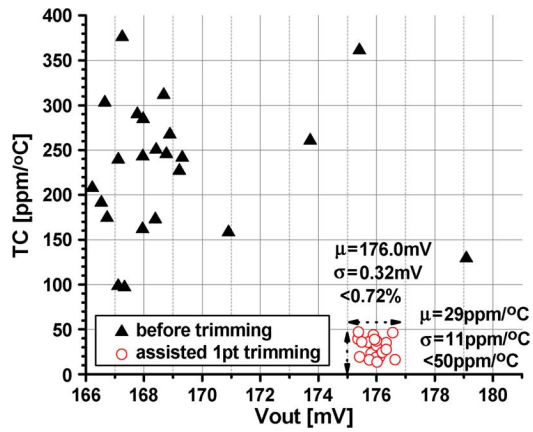

Fig. 14. Measured reductions of output voltage and temperature coefficient spreads after assisted one temperature point trimming in 0.13 μm.

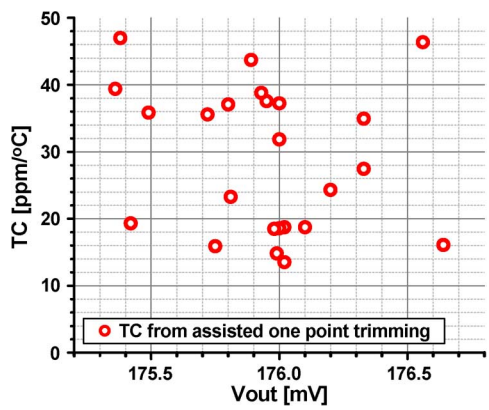

Fig. 15. Measured output voltages and temperature coefficients after assisted one temperature point trimming in 0.13 μm (zoomed in view of data at bottom right in Fig. 14).

0.8 pF output capacitor, the trimmable voltage reference effectively suppresses noise, showing 16 $\mu V/Hz^{1/2}$ with a 0.8 pF output capacitor at 100 Hz. As a reference point, [12] exhibits

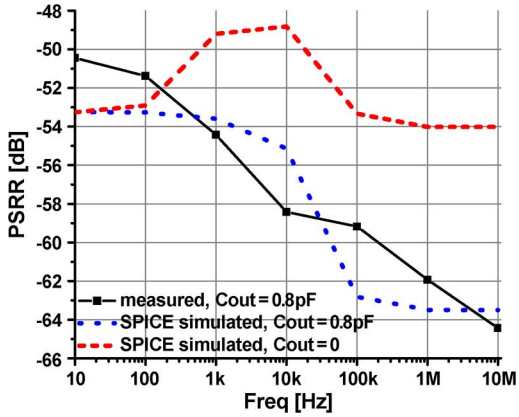

Fig. 16. Measured PSRR of post-trimmed trimmable 2T voltage reference in 0.13 μm; schematics are shown in Fig. 12.

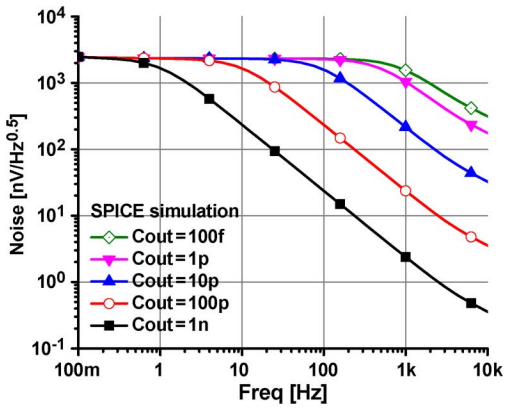

Fig. 17. Simulated output referred noise of post-trimmed 2T voltage reference (0.13 μm).

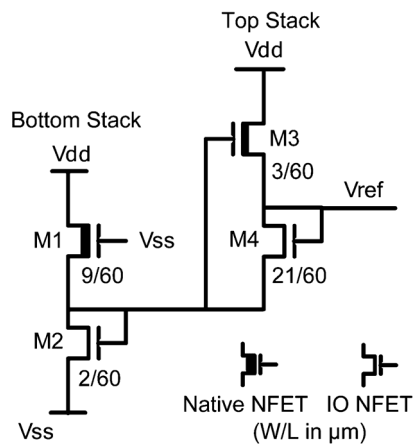

Fig. 18. Schematic of 4T voltage reference.

152 nV/Hz$^{1/2}$ with a much larger 100 nF output capacitor at 100 Hz.

V. Variants of the 2T Voltage Reference

This section describes several variants of the 2T voltage reference. The first variant is a 4T voltage reference that produces a higher output by stacking two 2T voltage references, as shown in Fig. 18. Measurement results from a prototype 4T design fabricated in 0.13 μm CMOS show a TC of 98.8 ppm/°C, LS of 0.036%/V, PSRR of -59 dB at 100 kHz, and power consumption of 10.85 pW at $V_{dd} = 0.5$ V. The design requires 3500 μm^2 including the 0.8 pF output capacitor. Measurement results of this structure are summarized in Table II and the die photo is shown in Fig. 19.

We can also generate lower output voltages by replacing the bottom device in the original 2T voltage reference (M_1 in Fig. 2) with multiple devices as shown (Fig. 20). This design has been successfully implemented in a low power microsystem [21] to provide a reference voltage to a simple linear regulator and to bias several transistor gate voltages in analog circuitry. It is also employed in power management units and clocked comparators in optical receivers for light detection, as integrated in the ultra-low power microsystem of [40].

By skewing the transistor size of the bottom and top devices (M1 and M2 in Fig. 2), we can create a CTAT or PTAT voltage reference. The temperature coefficient can be configured post-silicon using the same topology as the trimmable voltage reference in Fig. 12. We fabricated the CTAT and PTAT voltage references in 0.13 μm CMOS. In the CTAT design, the bottom transistor (M2 in Fig. 2) is 4 times larger than the top transistor (M1 in Fig. 2). The PTAT voltage reference uses a 9$\times$ larger top transistor compared to bottom transistor. The output voltages of the designs linearly increase or decrease with temperature, as shown in Fig. 21. Measured temperature coefficients for the PTAT and CTAT reference voltages are 145 ppm/°C and -550 ppm/°C, respectively.

VI. Technology Portability

Technology portability is an important metric when evaluating the usefulness of a given circuit topology. Supply voltage scalability poses a critical challenge for designing conventional bandgap voltage references in scaled technologies as they often require >1 V supply voltage to turn on BJT devices. Also, the design complexity of past voltage references hinders their technology portability, which is a concern in modest scale designs with high cost sensitivity, such as the targeted ultra-low power sensing microsystems. To demonstrate the portability of the proposed voltage reference design, we implemented 2T voltage references in 0.18 μm and 65 nm CMOS technologies to supplement the measured results from 0.13 μm CMOS in previous sections. Given the simple topology and the wide range of supply voltage scalability, porting the design only involves sizing of the two transistors.

Measurement results from 0.18 μm and 65 nm are given in Table II, showing similar performance as the 0.13 μm design. The sizing information is shown in Fig. 2. The exact performance numbers differ over technologies. Summarizing the key results, the voltage reference (best TC die) in 0.18 um CMOS shows TC of 54 ppm/°C, LS of 0.044%/V, PSRR of -49 to -55 dB, and power consumption of 5.5 pW. The 65 nm prototype exhibits TC of 89 ppm/°C, LS of 0.33%/V, PSRR of -40 to -79 dB, and power consumption of 240 pW in a compact 900 μm^2. Shorter channel lengths are intentionally used in the 65 nm design, specifically $L_1 = 1.2$ μm and $L_2 = 0.6$ μm, to demonstrate the tradeoff between area and power consumption. Line sensitivity in this case increases due to the higher short channel effects observed at these shorter channel lengths. TC

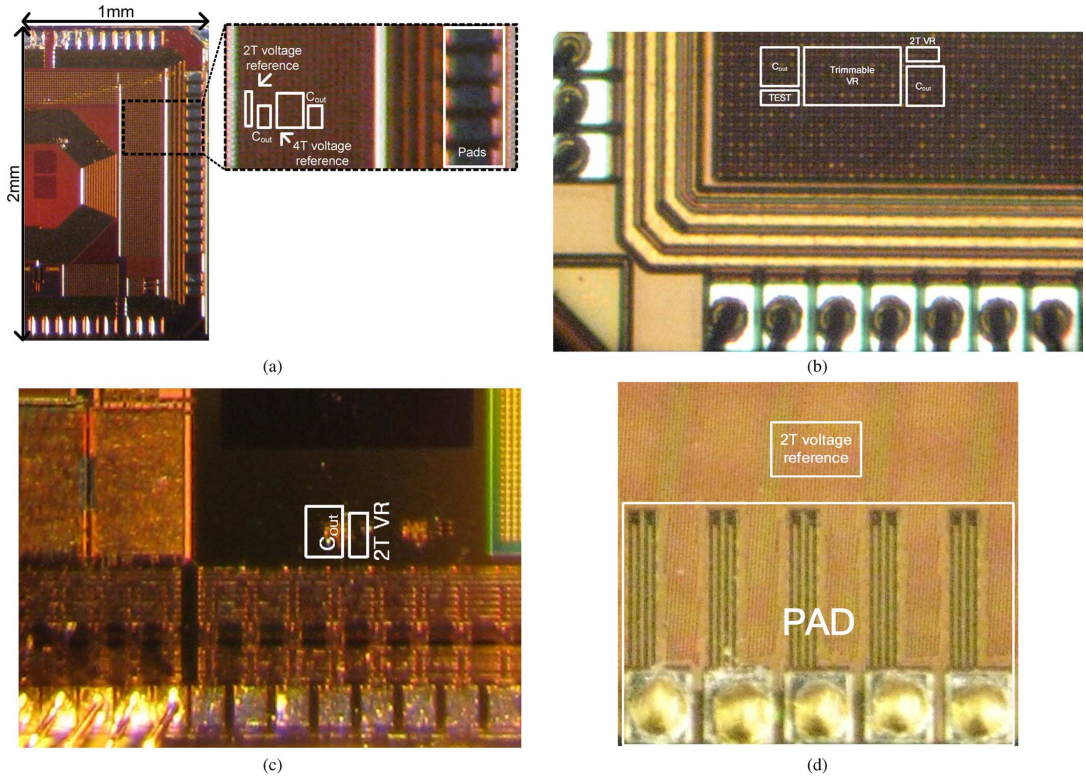

Fig. 19. Schematic of a 2T voltage reference providing lower output voltage.

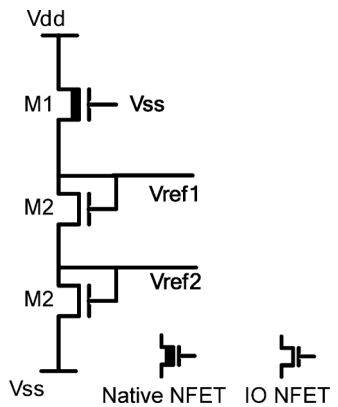

Fig. 20. Measured temperature coefficients achieved by skewing transistor sizes (0.13 μm).

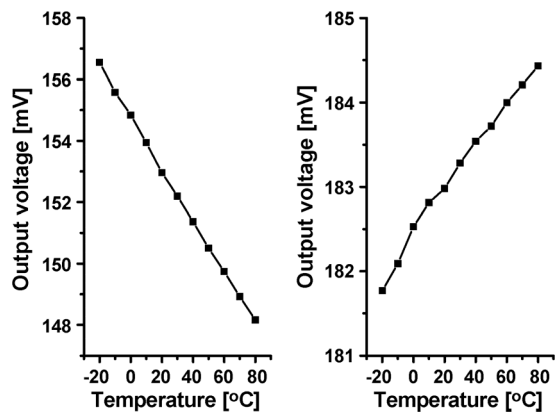

Fig. 21. Die micrographs. (a) First 0.13 μm run. (b) Second 0.13 μm run. (c) 0.18 μm run. (d) 65 nm run.

variability is expected to be larger due to the smaller transistor dimension and stronger short channel effects. From SPICE simulations, a 65 nm design using $L_1 = L_2 = 60$ μm consumes 5 pW with a 20× area overhead compared to the fabricated short channel version. Die photos for all silicon implementations described in this work are included in Fig. 21.

VII. Conclusions

This paper proposed a 2T voltage reference and several variants that offer sub-nW power consumption and operation at 0.5 V while maintaining competitive temperature coefficient, line sensitivity, and power supply rejection ratio. Single temperature point digital trimming is also demonstrated, effectively tightening the spread of temperature coefficient and output voltage. The design is shown to be highly portable across technologies with silicon results from three different CMOS technologies. Overall the design represents a 2–3 order of magnitude improvement in power consumption compared to prior state of the art and is well suited to ultra-low power sensing systems due to its low power consumption and compact footprint.

Acknowledgment

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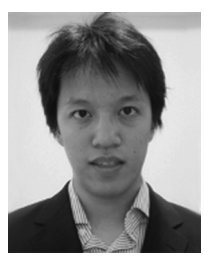

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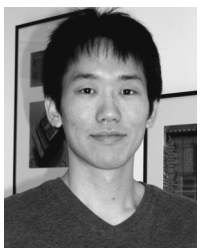

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