

A 4.7 μ W Switched-Bias MEMS Microphone Preamplifier for Ultra-Low-Power Voice Interfaces

Sechang Oh, Taekwang Jang, Kyojin D. Choo, David Blaauw, Dennis Sylvester
University of Michigan, Ann Arbor, MI

Abstract

This paper presents a switched-bias MEMS microphone preamplifier for an ultra-low-power voice interface. A switched-MOSFET periodically changes the MOSFET between strong inversion and accumulation to inherently reduce $1/f$ noise. In addition, a proposed coupling capacitor allows the microphone to benefit from a high bias voltage while the preamp can use a low VDD. The preamp achieves 7.3 μ V_{rms} input referred noise (A-weighted) with 3.4 μ A, improving NEF by 4.5 \times . Acoustic testing with the preamp and MEMS microphone shows 61.3dBA SNR at 94dB SPL.

Introduction

Voice interfaces are expected to play a dominant role in wireless sensor nodes and IoT, where conventional interfaces such as touch are limited because of small size. Recent microsystems as small as 6mm³ [1] have been reported with battery capacity of <10 μ Ah. Enabling audio interfaces in a power-constrained system requires low noise and moderate dynamic range interface circuits to achieve high far-field audio quality and clarity. One key challenge lies in the low-power microphone preamplifier implementation; this component boosts audio signal to line level and is the most noise/power sensitive block in the entire signal chain.

The human audible frequency range is 20-20kHz and microphone preamp noise is therefore severely impacted by $1/f$ noise. Chopper amplifiers, which are often used to remove $1/f$ noise, cannot be used with high impedance input sources such as MEMS microphones (with base capacitance of several pF) since the associated switching current causes high voltage output noise [2], [3]. Therefore, large input transistors must be used, increasing gate capacitance and noise gain, and thus degrading current noise efficiency (NEF=14.9) [4]. Another approach provides excitation signals for capacitive sensors to remove $1/f$ noise [5]. However, the DC capacitance canceling path to remove the carrier signal doubles noise gain and NEF. Furthermore, the excitation uses the relatively low preamp supply voltage, limiting microphone sensitivity (-35dBV/Pa) and power (2.5mW).

To overcome these limitations, we propose a low-power preamp with switched biasing and a modified coupling capacitor feedback. Together, these techniques enable the preamp to achieve 7.3 μ V_{rms} noise with 3.4 μ A, improving over previous work in the audio amplifier space by 14.7 \times in power and 4.5 \times in noise efficiency factor.

Proposed MEMS Microphone Preamplifier

Periodic on/off switching of a MOSFET between strong inversion and accumulation has been shown to reduce $1/f$ noise [6], [7]. $1/f$ noise is caused by the trapping/de-trapping process of carriers in the gate oxide. The trapping-detrapping process occurs with a wide range of time constants, including very long timeframes. By turning the device on and off, the long-term memory effect of $1/f$ noise is essentially reset and low-frequency $1/f$ noise is inherently reduced.

Fig. 1 shows the implementation of the proposed switched-bias preamp. The left or right path is alternately used according to the phase of Φ , and cascode and current source devices are shared for all phases. Here Φ is a 140kHz clock, which is set to be out of the audio band. With $\Phi=0$, current flows through the left path of the preamp, while the right pair transistors are clock gated (Figs. 2 and 3). Specifically M_{LP1-3} and M_{LN1-3} are ON and M_{LP4-6} and M_{LN4-6} are OFF so that the left input pairs ($M_{LPIN+/-}$ and $M_{LNN+/-}$) are connected to the cascode and current source devices and used for the signal amplification. Meanwhile, the right input pairs ($M_{RPIN+/-}$ and $M_{RNN+/-}$) are in the super-cutoff region by connecting M_{RN4-6} to VSS and M_{RP4-6} to VDD to enhance $1/f$ noise reduction. While $\Phi=1$, the preamp uses the right path and the left path is similarly clock gated.

The preamp is implemented with an inverter-based cascode amplifier to maximize g_m and gain at a given current. 3dB SNR is improved

by reusing the bias current in both PMOS and NMOS. CMFB is implemented with a differential difference amplifier and it uses 1/16 current of the main amplifier. Transistor sizes are chosen to optimize noise efficiency with A-weighted filtering.

Fig. 4 illustrates the overall MEMS microphone assembly consisting of MEMS sensor and ASIC on a board with a lid. The MEMS microphone consists of two parallel plates that form a pressure-sensitive capacitor. The microphone capacitance is determined by plate area and distance. Sound pressure is measured in voltage change given by $\Delta V_B = V_B/C_M \cdot \Delta C_M$ and bias voltage V_B is generally preferred to be as large as possible to achieve high sensitivity, while maintaining safe margin from its "pull-in" point. The conventional approach (Fig. 5a) uses a significant fraction of die area for C_B ($\gg C_M$) to filter out V_B noise generated from a charge pump.

In the proposed preamp (Fig. 5b), C_C couples V_B and the preamp input common mode voltage to allow the microphone to benefit from a high voltage bias without C_B while the preamp can use a low VDD for low power. Since V_B noise is low-pass filtered by R_B and C_F , a simple charge pump can be used without additional filtering. The signal gain is $-C_M/C_F$ (9.6dB) and is insensitive to C_P , C_C , and C_G , resulting in excellent linearity. Input transistor pairs are the main noise contributors of an amplifier. To minimize the noise gain of the feedback loop, large C_C with small C_P and C_G are needed. C_C is chosen as $3 \times C_M$, which is limited by the fact that C_C parasitics also contribute to C_P and C_G . C_I is a six-bit programmable capacitor array and it is tuned to C_M+C_P to maximize noise efficiency during testing. MOM capacitors are used for C_P , C_C , and C_I to avoid leakage at high voltage bias. R_B and R_F are implemented with pseudo-resistors to achieve high resistance with small area. These resistances are used to make high pass poles and must be sufficiently large that they do not impact the microphone low frequency response (<20Hz). R_F sets the input common mode voltage and cancels the preamp DC offset.

Measured Results

The microphone preamp is fabricated in 180nm CMOS and tested at 1.4V VDD. The active circuit area is 0.07mm² (Fig. 6). Fig. 7 shows measured preamp frequency response. The preamp gain is 9.6dB and high pass corner frequency is 0.4Hz. PSRR in the audio band with a 100mV_{rms} tone is >79dB and >66dB with and without the switched bias, respectively, demonstrating significant improvement from the proposed technique. Fig. 8 shows the preamp output noise spectrum. Maximum noise power reduction from switched bias occurs at 1kHz, marking a 37% reduction. The A-weighted input referred noise is 7.3 μ V_{rms}, which is a 25% reduction due to switched bias. Fig. 9 shows the preamp output offset difference with switched bias between the two paths is 1.2mV and overshoot is 3mV. Offset σ is 3.9mV as measured from 17 chips (Fig. 10). THD is measured at different output amplitudes. The design exhibits 1% and 2% THD with 300mV_{rms} output magnitude with and without switched bias at 1kHz, respectively (Fig. 11). The preamp is integrated with a MEMS microphone and tested in a sound chamber. Fig. 12 shows THD measurement across sound pressure, showing 0.6% at 94dBA SPL and 5% at 113dBA SPL. Microphone SNR and sensitivity are 61.3 dBA and -29.5dBV, respectively, with 94dBA SPL input at 1kHz. Fig. 13 summarizes the proposed preamp and microphone performance and compares to prior work in this area, showing 14.7 \times lower power and 4.5 \times NEF improvement while achieving 61.3dB SNR.

References

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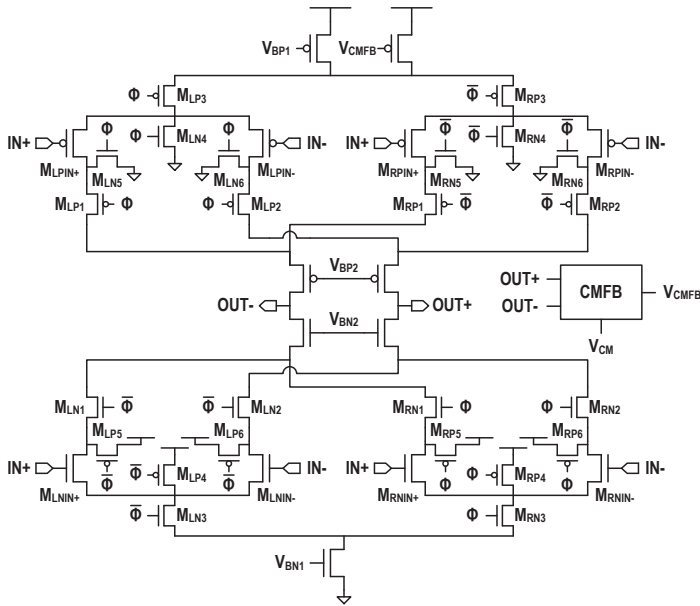


Fig. 1. Detailed implementation of the switched-bias preamp.

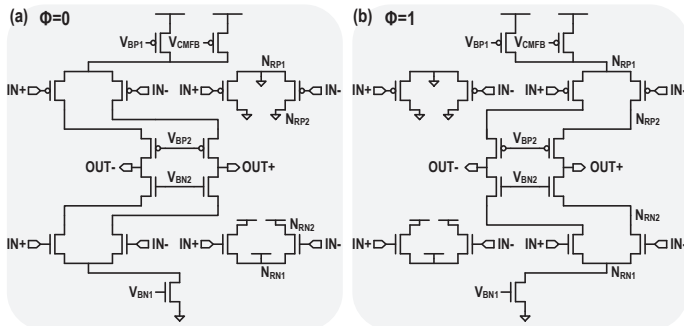


Fig. 2. Operation of the switched-bias preamp (a) $\Phi=0$ (b) $\Phi=1$.

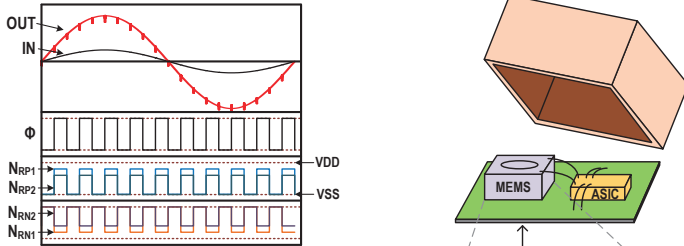


Fig. 3. Timing diagram of the preamp.

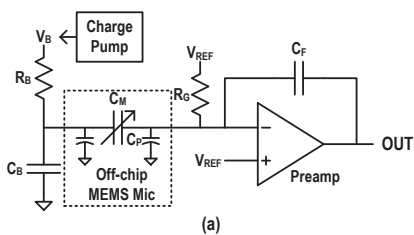


Fig. 4. MEMS microphone (a) assembly (b) sensing element.

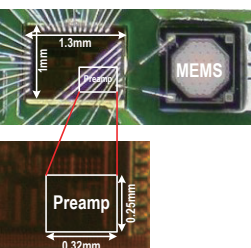


Fig. 6. Die photo.

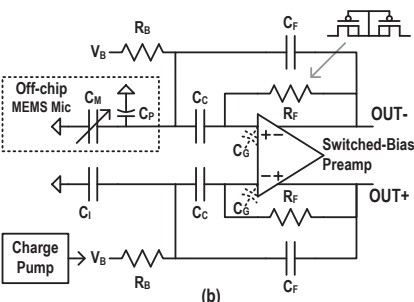


Fig. 5. MEMS microphone preamplifier (a) conventional (b) proposed.

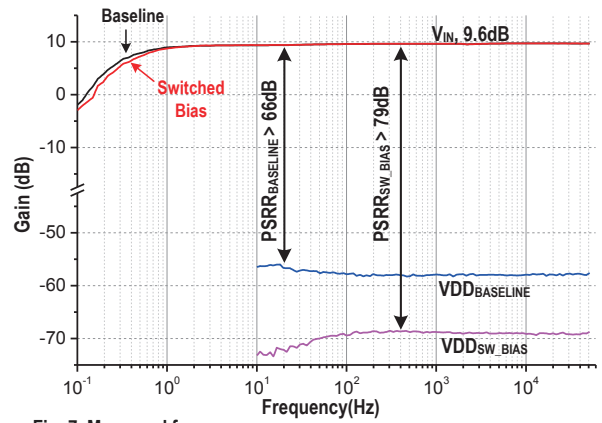


Fig. 7. Measured frequency response.

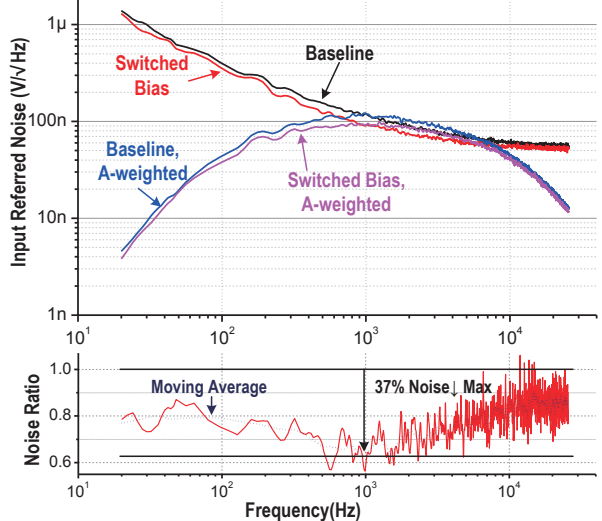


Fig. 8. Measured frequency response (top) and noise power ratio (bottom).

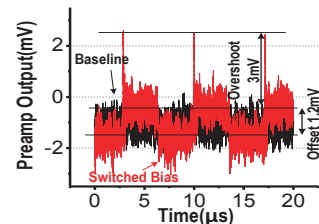


Fig. 9. Measured switching ripples.

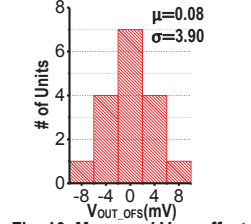


Fig. 10. Measured V_{OUT} offset.

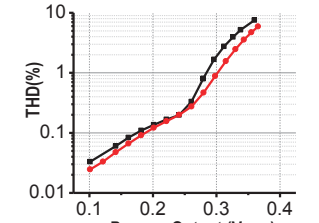


Fig. 11. Measured preamp THD.

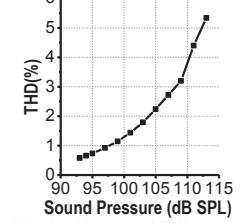


Fig. 12. Measured THD across SPL at 11V V_B & 1kHz.

Parameters	This Work	ISSCC 2009 [4]	ISSCC 2013 [5]	ESSCIRC 2009 [8]	JSSC 2012 [9]
Technology (nm)	180	180	160	350	40
VDD (V)	1.4	1.8	5	1.8	1.5
Active Area(mm ²)	0.07	2.98	0.25	0.9	0.19
Preamp Gain (dB)	9.6	8.5	N/A	8	0
Preamp Noise (μ V _{rms} , A-weighted)	7.3	5	N/A	25	4
Preamp Current (μ A)	3.4	120	500	50	220
Preamp NEF	3.3	14.9	N/A	48.20	16.2
SNR (dBA @1Pa)	61.3	62.5	58	27	N/A
Sensitivity (dBV @1Pa, 1kHz)	-29.5	-33	-35.1	-48	N/A
THD (% @dB SPL, 1kHz)	0.6 @94	0.4 @104	0.5 @94	0.2 @120	N/A

$$NEF = V_{rms,A} \sqrt{\frac{2 \times I}{\pi V_T \times 4KT \times BW_{20k}}}$$

Fig. 13. Performance summary and comparison.