Tae-Kwang Jang

Electrical Engineering, University of Michigan

E-Mail: tkjang@umich.edu

Education

Ph.D. in Electrical Engineering, University of Michigan **September 2013 – November 2017**

- Dissertation title: Circuit and System Designs for Millimeter Scale IoT and Wireless Neural Recording
- Adviser: Professor David T. Blaauw

M.S. in Electrical Engineering, Korea Advanced Institute of Science and Technology

March 2006 – February 2008

- Thesis title: Analysis and Design of Voltage-Controlled Oscillator based Analog-to-Digital Converter
- Adviser: Professor SeongHwan Cho

B.S. in Electrical Engineering, Korea Advanced Institute of Science and Technology

March 2002 – February 2006

Work Experience

Senior Engineer, Samsung Electronics Inc., Mixed-Signal Core Design Team **February 2008 – July 2017**

- Designed Integer-N, Fractional-N, Spread-spectrum PLLs and a DLL in 20nm, 28nm, 32nm, 45nm and 65nm CMOS processes for SoC applications.
- Designed integer-N and fractional-N digital PLLs in 20nm and 28nm CMOS process.
- Leave of absence for Phd study in University of Michigan in 2013-2017.

Intern, Hynix Semiconductor, DRAM 3-team **January 2005 – February 2005**

Publications

Conference

1. Y. Zeng, **T. Jang**, Q. Dong, M. Saligane, D. Sylvester and D. Blaauw, “A 1.7nW PLL-Assisted Current Injected 32kHz Crystal Oscillator for IoT,” *2017 Symposium on VLSI Circuits (**VLSI Circuits**).*
2. S. Oh, **T. Jang**, K. D. Choo, D. Blaauw and D. Sylvester, “A 4.7μW Switched-Bias MEMS Microphone Preamplifier for Ultra-Low-Power Voice Interfaces,” *2017 Symposium on VLSI Circuits (**VLSI Circuits**).*
3. **T. Jang**, S. Jeong, D. Jeon, K. Choo, D. Sylvester and D. Blaauw, “A 2.5ps, 0.8-3.2GHz, Bang-Bang Phase and Frequency Detector Based All-Digital PLL with Noise Self-Adjustment,” *2017 IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp. 201-202
4. S. Jeong, Y. Chen, **T. Jang**, J. Tsai, D. Blaauw, H.-S. Kim, D. Sylvester, “A 12nW Always-On Acoustic Sensing and Object Recognition Microsystem Using Frequency-Domain Feature Extraction and SVM Classification,” *2017 IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp. 508-509
5. W. Lim, **T. Jang**, I. Lee, H.-S. Kim, D. Sylvester and D. Blaauw, “A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation,” *2016 Symposium on VLSI Circuits (**VLSI Circuits**).*
6. **T. Jang**, M. Choi, Y. Shi, I. Lee, D. Sylvester and D. Blaauw, "Millimeter-scale computing platform for next generation of Internet of Things," *2016 IEEE International Conference on RFID (**RFID**)*, Orlando, FL, 2016, pp. 1-4, ***invited***.
7. **T. Jang**, M. Choi, S. Jeong, S. Bang, D. Sylvester and D. Blaauw, "A 4.7nW 13.8ppm/^{o}C self-biased wakeup timer using a switched-resistor scheme," *2016 IEEE International Solid-State Circuits Conference (**ISSCC**)*,

pp. 102-103.

8. M. Choi, **T. Jang**, J. Jeong, S. Jeong, D. Blaauw and D. Sylvester, "A current-mode wireless power receiver with optimal resonant cycle tracking for implantable systems," *2016 IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp. 372-373.
9. **T. Jang**, S. Jeong, M. Choi. W. Jung, G. Kim, Y.-P. Chen, Y. Kim, W. Lim, D. Sylvester and D. Blaauw, "FOCUS: Key building blocks and integration strategy of a miniaturized wireless sensor node," *2015 IEEE European Solid-State Circuits Conference (**ESSCIRC**)*, pp. 257-262, ***invited***.
10. M. Choi, S. Bang, **T.-K. Jang**, D. Blaauw and D. Sylvester, "A 99nW 70.4kHz resistive frequency locking on-chip oscillator with 27.4ppm/ºC temperature stability," *2015 Symposium on VLSI Circuits (**VLSI Circuits**)*, pp. C238-C239.
11. M. Choi, I. Lee, **T.-K. Jang**, D. Blaauw and D. Sylvester, "A 23pW, 780ppm/°C resistor-less current reference using subthreshold MOSFETs," *2014 IEEE European Solid State Circuits Conference (**ESSCIRC**)*, 2014, pp. 119-122.
12. J. Liu, **T.-K. Jang**, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park and H. Park, "A 0.012mm^2 3.1mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," *2014 IEEE International Solid-State Circuits Conference* (ISSCC), pp. 268-269.
13. **T. K. Jang**, X. Nan, F. Liu, J. Shin, H. Ryu, J. Kim, T. Kim, J. Park and H. Park, "A 0.026mm^2 5.3mW 32-to-2000MHz digital fractional-N phase locked-loop using a phase-interpolating phase-to-digital converter," *2013 IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp. 254-255.
14. J. P. Hong, J. Liu, N. Xing, **T.-K. Jang**, J. Park, J. Kim, T. Kim and H. Park, "A 0.004mm^2 250μW ΔΣ TDC with time-difference accumulator and a 0.012mm^2 2.5mW bang-bang digital PLL using PRNG for low-power SoC applications," *2012 IEEE International Solid-State Circuits Conference (**ISSCC**),* pp. 240-242.
15. J. Liu, S. Jeon, **T.-K. Jang**, D. Kim, J. Kim, J. Park and H. Park, "A 0.8V, sub-mW, varactor-tuning ring-oscillator-based clock generator in 32nm CMOS," *2011 IEEE Asian Solid State Circuits Conference (**A-SSCC**),* pp. 337-340.
16. F. J. Liu, S. Jeon, **T.-K. Jang**, D. Kim, J. Kim J. Park and B.-H. Park, "A Sub-1V, 1.6mW, 2.06GHz clock generator for mobile SoC applications in 32nm CMOS," *2010 International SoC Design Conference (**ISOCC**),* pp. 342-344.
17. J. Lee, K. Kim, J. Lee, **T. Jang** and S. Cho, "A 480-MHz to 1-GHz sub-picosecond clock generator with a fast and accurate automatic frequency calibration in 0.13-μm CMOS," *2007 IEEE Asian Solid-State Circuits Conference (**A-SSCC**),* pp. 67-70.

Journal

1. **T. Jang**, S. Jeong, D. Jeon, K. Choo, D. Sylvester and D. Blaauw, “A Noise Reconfigurable All Digital Phase Locked Loop Using a Switched Capacitor based Frequency Locked Loop and a Noise Detector,” in *IEEE **Journal of Solid-State Circuits***, vol. 53, no. 1, pp. 50-65, Jan. 2018, ***invited***
2. **T. Jang**, G. Kim, B. Kempke, M. B. Henry, N. Chiotellis, C. Pfeiffer, D. Kim, Y. Kim, Z. Foo, H. Kim, A. Grbic, D. Sylvester, H.-S. Kim, D. Wentzloff, D. Blaauw, “Circuit and System Designs of Ultra-low Power Sensor nodes with Illustration in a Miniaturized GNSS Logger for Position Tracking: Part II—Data Communication, Energy Harvesting, Power Management and Digital Circuits,” in *IEEE **Transactions on Circuits and Systems I**: Regular Papers*, vol. 64, no. 9*, **invited***.
3. **T. Jang**, G. Kim, B. Kempke, M. B. Henry, N. Chiotellis, C. Pfeiffer, D. Kim, Y. Kim, Z. Foo, H. Kim, A. Grbic, D. Sylvester, H.-S. Kim, D. Wentzloff, D. Blaauw, “Circuit and System Designs of Ultra-low Power Sensor nodes

with Illustration in a Miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques," in *IEEE* ***Transactions on Circuits and Systems I****: Regular Papers*, vol. 64, no. 9, ***invited***.

4. S. Jeong, Y. Chen, **T. Jang**, J. Tsai, D. Blaauw, H.-S. Kim, D. Sylvester, "Always-On 12nW Acoustic Sensing and Object Recognition Microsystem for Unattended Ground Sensor Nodes," *IEEE* ***Journal of Solid-State Circuits***, vol. 53, no. 1, pp. 261-274, Jan. 2018, ***invited***
5. M. Choi, **T. Jang**, J. Jeong, S. Jeong, D. Blaauw and D. Sylvester, "A Resonant Current-Mode Wireless Power Receiver and Battery Charger with -32 dBm Sensitivity for Implantable Systesms," in *IEEE* ***Journal of Solid-State Circuits****,* vol. 51, no. 12, pp. 2880-2892, Dec. 2016.
6. M. Choi, **T. Jang**, S. Bang; Y. Shi, D. Blaauw, D. Sylvester, "A 110 nW Resistive Frequency Locked On-Chip Oscillator with 34.3 ppm/°C Temperature Stability for System-on-Chip Designs," in *IEEE* ***Journal of Solid-State Circuits***, vol. 51, no. 9, pp. 2106-2118, Sept. 2016.
7. D. Yoon, **T. Jang**, D. Sylvester and D. Blaauw, "A 5.58 nW Crystal Oscillator Using Pulsed Driver for Real-Time Clocks," *in IEEE* ***Journal of Solid-State Circuits***, vol. 51, no. 2, pp. 509-522, Feb. 2016.
8. **T. K. Jang**, J. Kim, Y. G. Yoon and S. Cho, "A Highly-Digital VCO-Based Analog-to-Digital Converter Using Phase Interpolator and Digital Calibration," in *IEEE Transactions on Very Large Scale Integration (****VLSI****) Systems*, vol. 20, no. 8, pp. 1368-1372, Aug. 2012.
9. J. Kim, **T. K. Jang**, Y. G. Yoon and S. Cho, "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter," in *IEEE* ***Transactions on Circuits and Systems I****: Regular Papers*, vol. 57, no. 1, pp. 18-30, Jan. 2010.
10. Y. G. Yoon, J. Kim, **T. K. Jang** and S. Cho, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in *IEEE* ***Transactions on Circuits and Systems I****: Regular Papers*, vol. 55, no. 11, pp. 3571-3581, Dec. 2008. **(2009 Guillemin-Cauer Best Paper Award)**

Selected Design Experience

Academy

- A Stand-alone 2.7cm^3 GNSS Logger System
- A 1.8 NEF, 2.1μVrms 2.4μW Neural Recording Amplifier in 180nm CMOS
- A 4.7nW 13.8ppm/^{o}C Wake-up timer in 180nm CMOS
- A 2.5ps, 4GHz, Digital Integer-N PLL in 28nm FDSOI
- A 3.2ps, 3.2GHz, Digital Integer-N PLL in 28nm FDSOI
- A 1V, 3kHz, 4.7nW, 13.8ppm/^{o}C on-chip oscillator in 180nm CMOS
- A 20MHz input bandwidth, 52.5dB SNDR, 14.3mW 0.12mm^2 ADC in 0.13μm CMOS

Industry

- A 1V, 2GHz, Digital Integer-N PLL in 28nm SOI
- A 0.9V, 2GHz, Digital Fractional-N PLL in 20nm CMOS
- A 1V, 2GHz, Digital Fractional-N PLL in 28nm CMOS
- A low noise 1.1V, 900MHz, Fractional-N PLL in 45nm CMOS
- A 1V, 2GHz, Digital Integer-N PLL in 28nm CMOS
- A 1V, 1.6GHz, Fractional-N/Spread-spectrum PLL in 32nm CMOS
- A 1.1V, 2GHz, Integer-N PLL in 45nm CMOS
- A low noise 1.1V, 400MHz Integer-N PLL in 45nm CMOS
- A 1V, 2.5GHz, Digital Integer-N PLL in 32nm CMOS

- A 0.8V, 700MHz, Integer-N PLL in 32nm CMOS

Teaching Experience

Guest Lecturer: EECS427, VLSI Design I, University of Michigan **Fall 2016**

Teaching Assistant: EECS427 VLSI Design I, University of Michigan **Fall 2016**

Guest Lecturer: EECS312, Digital Integrated Circuits, University of Michigan **Fall 2016**

Scholarly Experience

Invited talk: "Millimeter Scale Computing Platform for Next Generation of Internet of Things," in *2016 IEEE International Conference on RFID* **May 2016**

Invited talk: "Circuit and System Designs for Millimeter Scale Internet-of-Things," Yonsei University **Nov. 2017**

Graduate Research Assistant: Michigan Integrated Circuits Lab, University of Michigan **August 2013 – Nov. 2017**

MS Student: Communication Circuits and Systems Laboratory, KAIST **December 2005 – February 2008**

Intern Student: Neural Networks and Machine Intelligence Laboratory, KAIST **December 2003 – February 2004**

Visiting Student: The University of California, Los Angeles **July 2007 – August 2007**

Member: KAIST Micro Robot Research **March 2002 –February 2008**

Member: KAIST Mathematical Problem Solving Group **March 2002 – August 2002**

Editorial Activities

Ad hoc reviewer

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Internet of Things Journal

Patents

Main inventor

- "Oscillator regulation circuitry and method," (patent number: 9490744)
- "Multi-phase generator," issued in U.S. (patent number: 8981828)
- "Digital phase-locked loop using phase-to-digital converter, method of operating the same, and devices including the same," issued in U.S. (patent number: 9041443)
- "Current generator, method of operating the same, and electronic system including the same," issued in U.S. (patent number: 9618958)
- "Phase locked loop circuit and system having the same," issued in U.S. (patent number: 8493115)
- "Phase locked-loop circuit, method of detecting lock, and system having the circuit," issued in U.S. (patent number: 8368439)
- "Analog-to-Digital Converter and Analog-to-Digital Conversion Method," issued in Korea Republic. (patent number: 100916553)
- "Voltage Controlled Oscillator Using Sub-feedback Loop and Analog-Digital Converter Having the Same," issued in Korea Republic. (patent number: 100936770)

Co-inventor

- "Ultra low power temperature insensitive current source with line and load regulation," issued in U.S. (patent

number:US9639107)

- “Phase locked loop, method of operating the same, and devices having the same,” issued in U.S. (patent number: 8981824)
- “All-digital phase-locked loop for adaptively controlling closed-loop bandwidth, method of operating the same, and devices including the same,” issued in U.S.(patent number: 9077351)
- “Duty correcting circuit, delay-locked loop circuit including the circuit, and method of correcting duty,” issued in U.S. (patent number: 8456212)

Research Interests

Analog and mixed circuits: (Frequency synthesizers, Data converters)

Low power systems: (Ultra-low power circuits, Sensor networks)

Bio-medical circuits: (Neural recording)

Awards & Scholarships

IEEE Transactions on Circuits and Systems 2009 Guillemin-Cauer Best Paper Award **May 2009**

- Title: A time-based bandpass ADC using time-interleaved voltage-controlled oscillators.

Bronze, Hyundai Automobile Electronics Car Competition **October 2004**

- Topic: An automated parking vehicle

Academic Honor Scholarship, KAIST **March 2002. – February 2006**

The Korea Foundation for Advanced Studies **March 2006. – February 2008**