23.3 A 3nW Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor DC-DC Converter

Wanyeong Jung, Sechang Oh, Suyoung Bang, Yoonmyung Lee, Dennis Sylvester, David Blaauw

University of Michigan, Ann Arbor, MI

Recent advances in low-power circuits have enabled mm-scale wireless systems [1] for wireless sensor networks and implantable devices, among other applications. Energy harvesting is an attractive way to power such systems due to limited energy capacity of batteries at these form factors. However, the same size limitation restricts the amount of harvested power, which can be as low as 10s of nW for mm-scale photovoltaic cells in indoor conditions. Efficient DC-DC up-conversion at such low power levels (for battery charging) is extremely challenging and has not yet been demonstrated.

Boost DC-DC converters are widely used to harvest energy from DC sources and yield high conversion efficiency [2]. However, they require a large off-chip inductor at low harvested power levels, increasing system size. Alternatively, switched-capacitor (SC) DC-DC converters can be fully integrated on-chip and are favored for form-factor constrained applications [3-8]. However, at low power levels, SC converter efficiency has been constrained by overheads of clock generation and level-conversion to drive the switch capacitors. As a result, efficient SC converter operation has been limited to the µW range.

This paper presents a fully integrated energy harvester maintaining >35% end-to-end efficiency when harvesting from a 0.84mm^2 solar cell in low light condition of 260lux, converting 7nW input power from 250mV to 4V. The key contribution of this work lies in the proposed SC DC-DC voltage doubler structure, in which an oscillator is completely internalized within the SC network. This eliminates power overhead of clock generation and level shifting, and enables higher efficiency at lower power levels. Voltage doublers are cascaded to form a complete harvester with a wide load range from 5nW to 5µW and self-starting operation down to 140mV. Since each doubler is self-oscillating, the frequency of each stage can be independently modulated, thereby optimizing the overall conversion efficiency. The harvester conversion ratio is configurable from 9× to 23× and idle power consumption is less than 3nW.

Figure 23.3.1 shows a conventional SC DC-DC voltage doubler that includes a clock generator, level shifter, and clock buffers. Each of these blocks introduces power overhead, reducing efficiency. The proposed doubler consists of two stacked ring oscillators with the output nodes of corresponding stages connected through flying caps (C_{FLY}). In each stage, inverters from the top and bottom ring either charge or discharge the flying cap thereby transferring power to the upper ring. Simultaneously, the inverters drive the next stage in their ring, creating a multi-phase DC-DC converter with overlapping charge/discharge phases and self-sustaining operation. Because the two oscillators are synchronized at every stage, phase mismatch is <0.01×FO4, reducing contention loss to <1% of switching loss (simulation) and avoiding the need for non-overlapping clocks. R_{DLY} is a delay element that ensures matching of the flying cap charging/discharging time to the oscillation period. In the harvester, this delay is automatically tuned to balance switching and conduction losses and maintain optimum conversion efficiency across a range of load currents.

Figure 23.3.2 shows the detailed implementation of the voltage doubler. The delay element R_{DLY} consists of two coupled leakage-based delay elements [1] and a pass transistor T_P, followed by two buffers. When the inputs H_{NC} and L_{NC} of the stage switch from high to low, output nodes H_{1A} and L_{1A} (driven low) become isolated. T_P then provides a leakage path from L_1 to L_{1A} that slowly raises L_{1A} and, through C_{C1}, also H_{1A}. Back-to-back inverters of the delay element provide positive feedback and amplify the transition once it reaches V_{TH}, creating a sharp edge. This transition is then buffered and passed to the next stage. The opposite transition functions similarly. Due to the output isolation the structure can produce very long, synchronized delay while the coupled positive feedback creates a sharp edge that limits short-circuit current and contention loss, enabling ultra-low power operation.

For each doubler, the delay tuning voltage V_{CON} is dynamically adjusted to balance conduction and switching losses by examining the ratio of output to input voltage (R_{DIV}). A low R_{DIV} indicates a large voltage across the switches and dominant conduction loss. Conversely, high R_{DIV} indicates low conduction loss (zero as $R_{DIV}{\rightarrow}2$) and dominant switching losses. This property is used to modulate the oscillation frequency of the doubler and maintain optimum efficiency across load currents. A clocked comparator, operating at a fraction of the internal oscillator frequency, takes in a divided form of the doubler output voltage ($V_{DIV} = V_{OUT}/R_{DIV\_DESIRED}$) and the input voltage (V_{MID}). The division ratio is configurable and is set to 1.73 in all measurements. A charge pump then takes in the corresponding pull-up/pull-down signals, and adjusts V_{CON} as needed to either speed or slow the oscillation. The voltage divider is implemented with a combination of a diode stack and capacitive divider to provide fast response and good low-frequency behavior.

Figure 23.3.3 shows the block diagram of the complete harvesting system, consisting of 4 stages of cascaded voltage doublers, a negative voltage generator, and circuits for conversion ratio control. A negative voltage is used to boost overall conversion ratio and to power control circuits, and is generated by connecting V_{HIGH} and V_{MED} of the doubler to V_{IN} and ground, respectively, resulting in $V_{NEG}{\approx}-V_{IN}$ at the V_{LOW} port of the doubler. To facilitate energy harvesting from a low voltage source (e.g., photovoltaic cell under low light), the first stage and negative voltage generator use low V_{TH} (~300mV) devices for their flying cap drivers. Bootstrapping is also used with these low V_{TH} switches to improve I_{ON}/I_{OFF} at low input voltages. I/O devices are used in the final stage to protect the circuit from high voltages used to charge energy storage devices (e.g., batteries).

The conversion ratio is adjusted by changing the number of cascaded stages. In addition, we propose a new adjustment scheme where the V_{LOW} of a doubler is switched among V_{IN}, GND and V_{NEG}. If V_{LOW} is set to $-V_{IN}$, the voltage across the flying cap increases, resulting in $V_{OUT} = (V_{MED}+V_{IN})\times2-V_{IN} = 2\times V_{MED}+V_{IN}$. If V_{LOW} is set to GND for 4 cascaded stages, overall conversion ratio is 16×. However, if final stage V_{LOW} is set to V_{NEG}, overall conversion ratio increases by 1×, becoming 17×. Similarly, setting V_{LOW} to V_{IN} decreases conversion ratio. In a binary manner, the conversion ratio is controlled from 9× to 23×. Measured results in Fig. 23.3.4. demonstrate that a 0.35V input can be converted to a 2.2 to 5.2V voltage range with similar conversion efficiencies across settings.

To enable cold start of the complete system, the control logic operates between V_{NEG} and V_{IN} rails. Upon initial system startup, V_{NEG} and V_{2X} become available first and allow the control logic to turn on and configure the switches. As each stage is powered up, its internal frequency modulation is enabled and begins to control the frequency for optimum efficiency.

The voltage doubler and energy harvester are fabricated in 0.18µm CMOS (Fig. 23.3.7). Figure 23.3.4 shows a single doubler has >70% efficiency across 1nA to 0.35mA output current (>10^5 range), with low idle power consumption of 170pW. Figure 23.3.5 shows measured results of the complete harvester. When V_{IN}=0.45V, the harvester delivers 5nW to 5µW output power with >40% efficiency, and has an idle power consumption <3nW. For V_{IN}=0.25V, corresponding to a solar cell under very low light, the harvester can take in between 10nW and 120nW to charge a ~4V battery voltage with >35% efficiency. Measured results with a small silicon solar cell (0.84mm^2) show actual harvesting operation under dim light of <100lux. The harvester cold starts with <200lux of light and 6nW power source. Figure 23.3.6 summarizes the performance of the proposed design and compares it to prior work.

References:
[1] G. Chen, M. Fojtik, D. Kim, *et al.*, "Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells," *ISSCC Dig. Tech. Papers*, pp. 288-289, Feb. 2010.
[2] J.-P. Im, S.-W. Wang, K.-H. Lee, *et al.*, "A 40mV Transformer-Reuse Self-Startup Boost Converter with MPPT Control for Thermoelectric Energy Harvesting," *ISSCC Dig. Tech. Papers*, pp. 104-105, Feb. 2012.
[3] H. Shao, C.-Y. Tsui, and W.-H. Ki, "An Inductor-Less MPPT Design for Light Energy Harvesting Systems," *Proc. ASP-DAC*, pp. 101-102, Jan. 2009.
[4] P.-H. Chen, K. Ishida, X. Zhang, *et al.*, "A 120-mV Input, Fully Integrated Dual-Mode Charge Pump in 65-nm CMOS for Thermoelectric Energy Harvester," *Proc. ASP-DAC*, pp. 469-470, Jan. 2012.
[5] D. Somasekhar, B. Srinivasan, G. Pandya, *et al.*, "Multi-Phase 1 GHz Voltage Doubler Charge Pump in 32 nm Logic Process," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 751-758, Apr. 2010.
[6] L. Chang, R.K. Montoye, B.L. Ji, *et al.*, "A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm^2," *IEEE Symp. VLSI Circuits*, pp. 55-56, June 2010.
[7] T.V. Breussegem and M. Steyaert, "An 82% Efficiency 0.5% Ripple 16-Phase Fully Integrated Capacitive Voltage Doubler," *IEEE Symp. VLSI Circuits*, pp. 198-199, June 2009.
[8] I. Doms, P. Merken, R. Mertens, C. Van Hoof, "Integrated Capacitive Power-Management Circuit for Thermal Harvesters with Output Power 10 to 1000µW," *ISSCC Dig. Tech. Papers*, pp. 300-301, Feb. 2009.
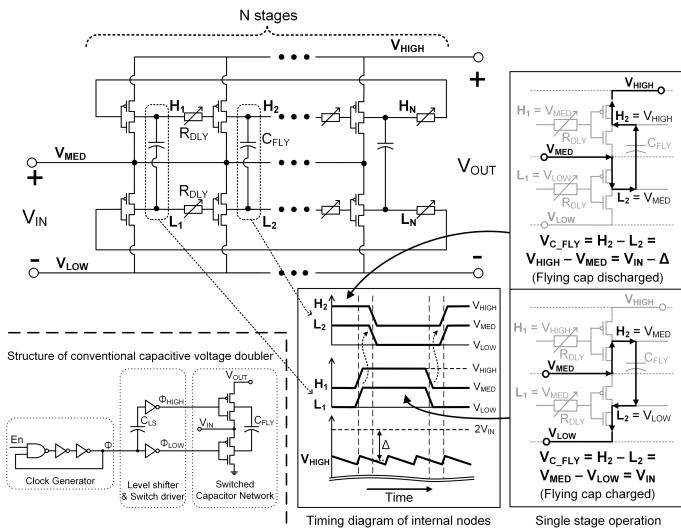
Figure 23.3.1: Concept of the proposed voltage doubler.
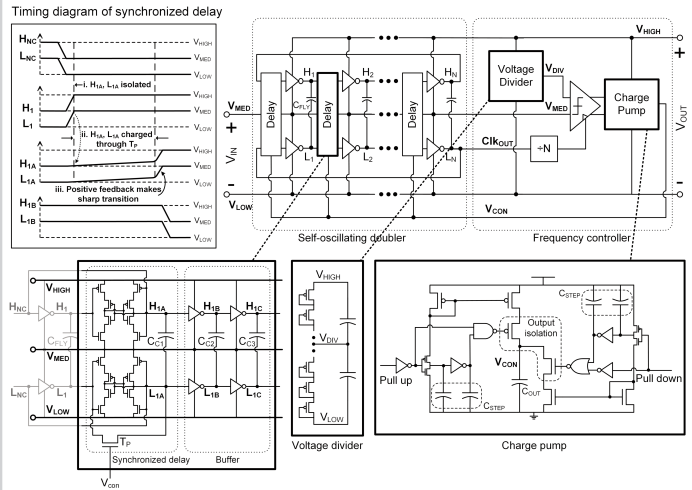

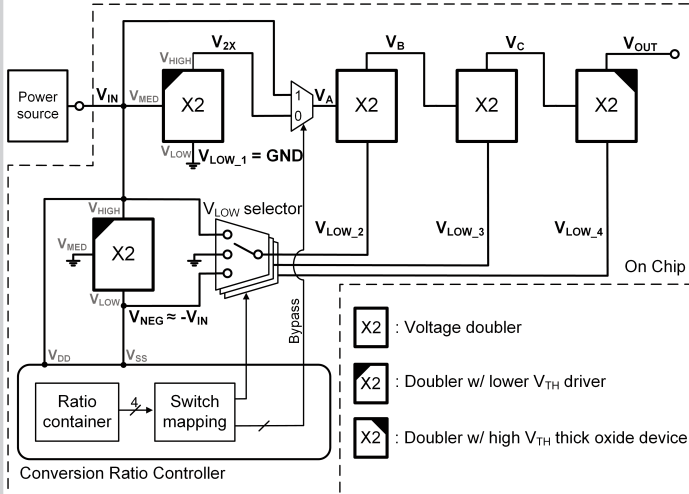Figure 23.3.2: Schematic of the voltage doubler.
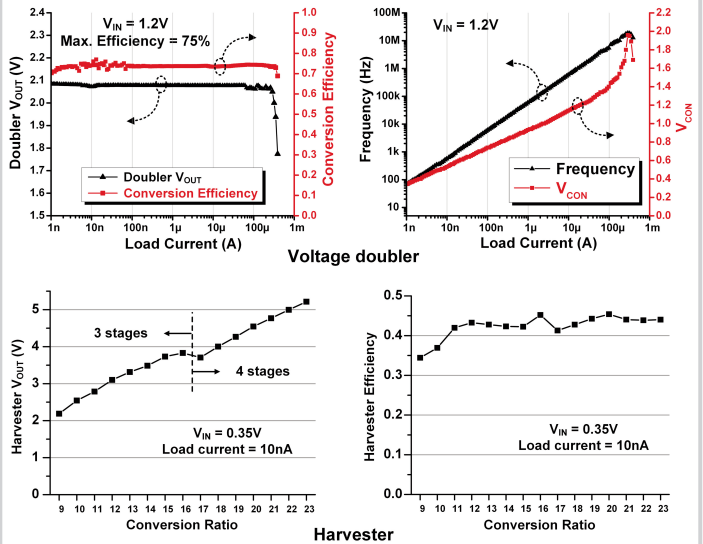

Figure 23.3.3: Structure of the harvester.

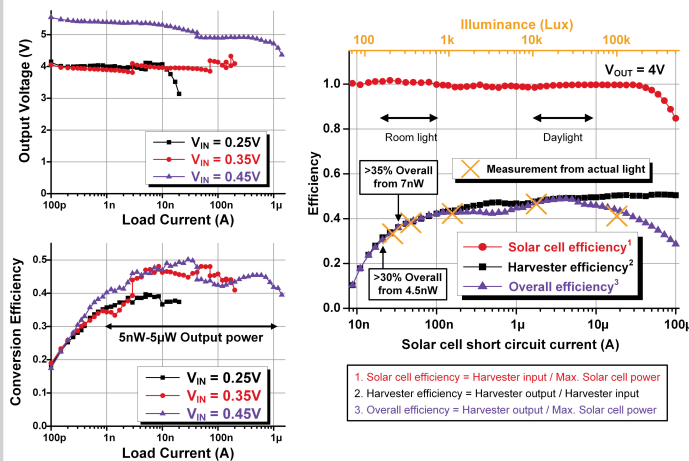Figure 23.3.4: Measured results of the doubler and harvester.

Figure 23.3.5: Measured results of the harvester.

Figure 23.3.6: Performance summary and comparison.

	[5]	[6]	[7]	This work (Doubler)
Technology	32nm CMOS	45nm SOI CMOS w/ trench cap	0.13μm CMOS	0.18μm CMOS
Architecture	Multi-phase voltage doubler	1:2 step-up/down converter	Multi-phase voltage doubler	Self-oscillating voltage doubler
Conversion ratio	1 : 2	2 : 1, 1 : 2	1 : 2	1 : 2
Tested input voltage	1V-1.2V	1V	1V-1.2V	1.2V
Frequency	250MHz-2GHz [1]	100MHz	N/R	70Hz-19MHz
Peak efficiency	64%	90%	82%	75%
Load range	0.4mA-9mA w/ >40% efficiency [1]	0.5mA-5mA w/ >80% efficiency [1]	0.15mA-2.2mA w/ >70% efficiency [1]	1nA-0.35mA w/ >70% efficiency
Area	0.0067mm²	0.0012mm²	2.25mm²	0.069mm²

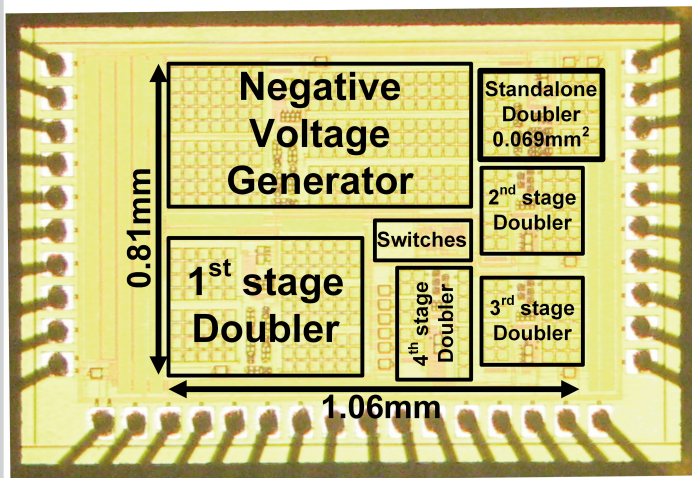|	[2]	[4]	[8]	This work (Harvester)
Technology	0.13μm CMOS	65nm CMOS	0.35μm CMOS	0.18μm CMOS
Architecture	Transformer self-startup	Integrated charge pump	Integrated charge pump	Cascade of integrated voltage doublers
Fully integrated	No (off-chip transformer)	Yes	Yes	Yes
Self-startup	Yes (min. 40mV)	Yes (min. 120mV)	N/R	Yes (min. 140mV)
Input voltage	40mV-300mV	0.12V-0.16V	0.6V-4V	0.14V-0.5V
Output voltage	2V	1V, 1.8V, 3V	N/R	2.2V-5.2V (0.35V VIN, 10nA I_LOAD)
Peak efficiency	61% @ 0.3V VIN	38.8% @ 0.12V VIN	70% @ 2V VIN	50% @ 0.45V VIN
Output power range	N/R	1μW-3μW @ 0.12V VIN [1] 2μW-7μW @ 0.14V VIN [1] 3μW-10μW @ 0.16V VIN [1] (w/ >15% efficiency) [1]	1μW-1mW (Only peak efficiency reported)	5nW-5μW w/ >40% efficiency
Idle power consumption	N/R	N/R	2μW @ 100μW input 7μW @ 1mW input	<3nW
Minimum input power	N/R	N/R	N/R	6nW for self-startup 1.7nW to sustain harvesting
Area	0.093mm²	0.78mm²	59mm²	0.86mm²

N/R: Not reported
[1] Estimated number from the paper

23

Figure 23.3.7: Die micrograph of the 0.18μm CMOS test chip.