A Modular 1 mm^3 Die-Stacked Sensing Platform With Low Power I^{2}C Inter-Die Communication and Multi-Modal Energy Harvesting

Yoonmyung Lee, *Member, IEEE*, Suyoung Bang, *Student Member, IEEE*, Inhee Lee, *Student Member, IEEE*, Yejoong Kim, *Student Member, IEEE*, Gyouho Kim, *Student Member, IEEE*, Mohammad Hassan Ghaed, *Student Member, IEEE*, Pat Pannuto, *Student Member, IEEE*, Prabal Dutta, Dennis Sylvester, *Fellow, IEEE*, and David Blaauw, *Fellow, IEEE*

***Abstract*—A 1.0 mm^3 general-purpose sensor node platform with heterogeneous multi-layer structure is proposed. The sensor platform benefits from modularity by allowing the addition/removal of IC layers. A new low power I^{2}C interface is introduced for energy efficient inter-layer communication with compatibility to commercial I^{2}C protocols. A self-adapting power management unit is proposed for efficient battery voltage down conversion for wide range of battery voltages and load current. The power management unit also adapts itself by monitoring energy harvesting conditions and harvesting sources and is capable of harvesting from solar, thermal and microbial fuel cells. An optical wakeup receiver is proposed for sensor node programming and synchronization with 228 pW standby power. The system also includes two processors, timer, temperature sensor, and low-power imager. Standby power of the system is 11 nW.**

***Index Terms*—Ultra-low power, wireless sensor node, smart dust.**

I. Introduction

CONTINUOUS fabrication technology scaling has led to the integration of computational capabilities in an increasingly smaller volume. This has been leveraged to create very small yet highly capable systems, as well as new multi-core and/or networking technologies that push the upper limits of modern computing performance. This, in turn, has produced a diversification of computing platforms, ranging from portable handheld devices to building-scale data centers. According to Bell's Law, a new class of less expensive computers is developed approximately every decade by using fewer components or fractional parts of state-of-the-art computing system [1]. In addition, the size of each subsequent classes of computing system becomes approximately 100 times smaller than its predecessor [2]. The first computers introduced in 1940s were room-sized or even as large as a small building. Smaller and more affordable computers were introduced in the form of workstations in 1970s and personal computers in 1980s, and mobility was added with laptops in 1990s and portable handheld devices in 2000s, as shown in Fig. 1. Recently, a growing amount of research has shown the potential of wireless sensor nodes, which is expected to be the next class of computers beyond hand-held devices. These wireless sensor nodes can be used in a wide range of applications including smart buildings [3], infrastructure monitoring [4], [5], and biomedical implants [6].

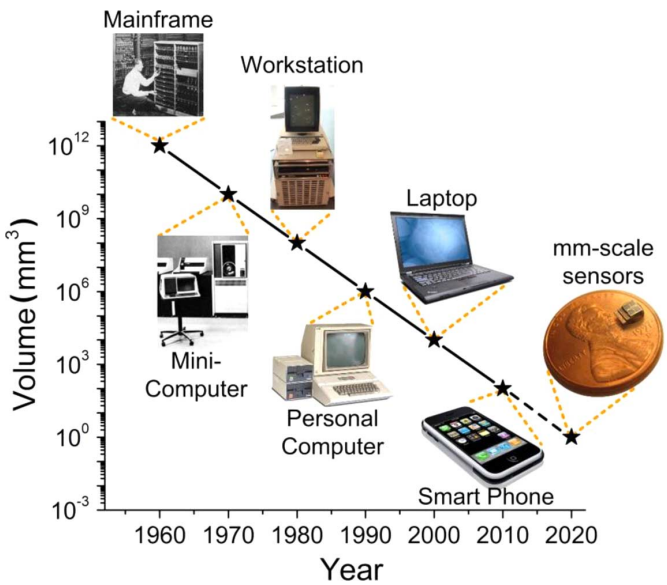

Fig. 1. Bell's Law [1] predicts continuous scaling of micro-size computing systems.

However, modern wireless sensors are composed of multiple components on a printed circuit board (PCB). Bulky batteries are included to power the circuit components with adequate lifetimes. The result is milliwatt-level systems that are centimeters or tens of centimeters on a side, failing to realize the "smart dust" vision of [7]. Smart dust requires mm^3-scale, wireless sensor nodes with perpetual energy harvesting. Recently, two application-specific implantable microsystems [8], [9] demonstrate the potential of mm^3-scale system in medical applications. However, [9] is not programmable and [8] lacks a method for re-programming or re-synchronizing once encapsulated. They are also made for a dedicated application, which limits their use for other purposes. Other important usability and deployment features also remain unaddressed, such as a

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The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: sori@umich.edu).

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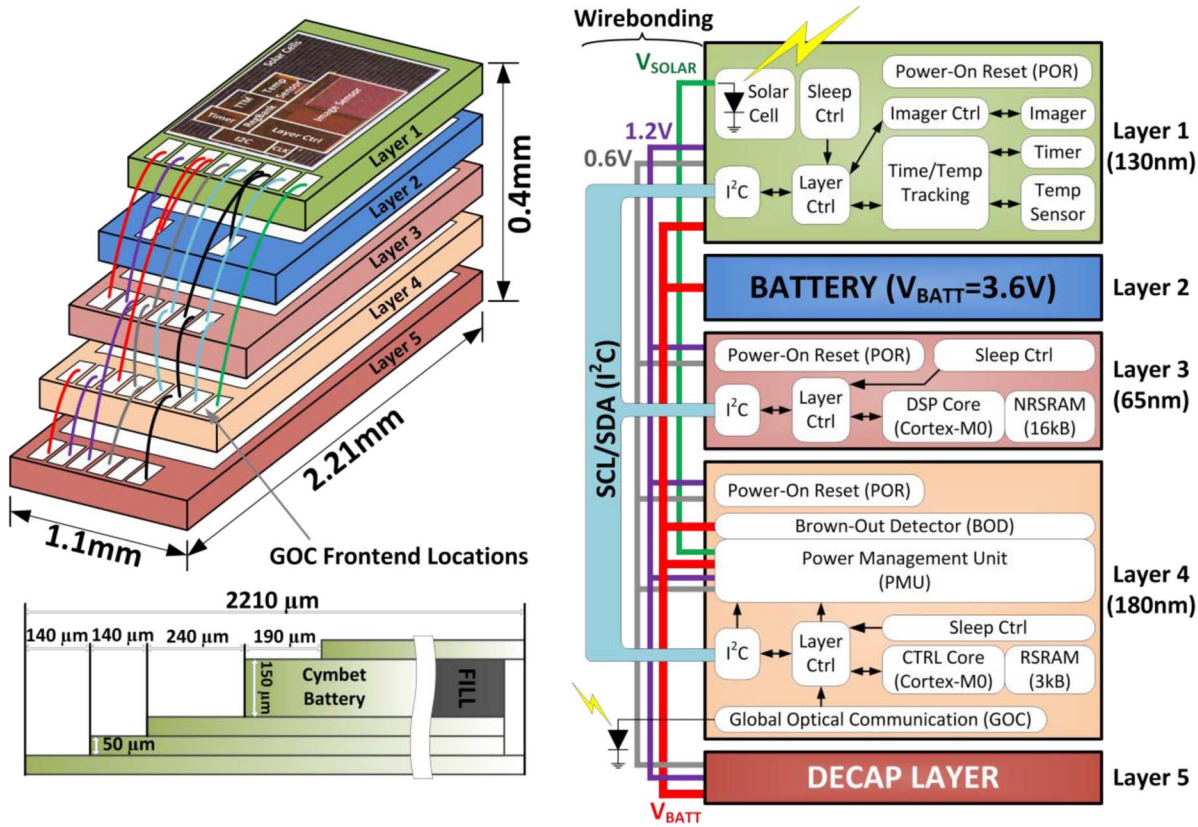


Fig. 2. Diagram and cross-sectional view of proposed 1.0 mm^3 sensing platform.

means to protect the battery during the time period between system assembly and deployment, wireless synchronization and batch programming, and flexible design to enable use in multiple application domains. A key challenge to implementing such features in a very small form factor is the additional power consumption incurred. To achieve long lifetime in a mm^3-scale system, power consumption of each component must be aggressively reduced to stay within a stringent power budget of $\sim$10 nW.

To this end, we propose a 1.0 mm^3 general purpose reconfigurable sensor node platform with a heterogeneous stackable multi-layer structure. The key components implemented to realize this form-factor includes ultra-low power I^{2}C (Inter-Integrated Circuit), a 228 pW standby power optical wakeup receiver, ultra-low power power management unit (PMU) and brown-out detector (BOD).

II. System Overview

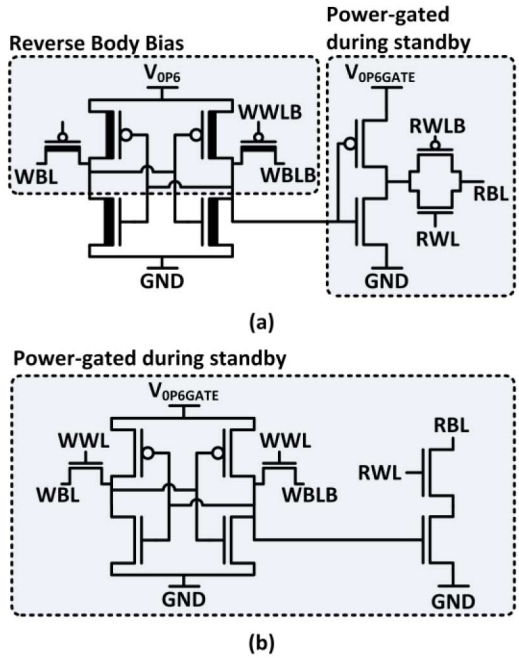
The 1.0 mm^3 sensing platform is designed with stacked integrated circuit (IC) dies fabricated in three different technologies. Fig. 2 shows the dimension of each die and the wirebonding scheme for electrical connectivity of the sensor system. To enforce 1.0 mm^3 volume, each layer measures less than 2.21×1.1 mm and the length of each layer has to be reduced by 140 μm compared to the lower layer to provide enough clearance for bond-wires. The height of each IC layer is thinned to $<$50 μm, while the custom thin-film Li battery is 150 μm thick. The system's die-stacked structure with wirebonding provides maximum functionality (or silicon area) per unit volume and also enables easy expansion of the system with additional layers. End users can create a sensor system for new applications by designing an application-specific layer in a preferred technology, which complies with the system power and energy budget, and providing an identical inter-layer communication interface.

Fig. 2 shows the system block diagram. The various components in the system are categorized as CPU, memory, power management, timer, and sensors.

CPU

The sensor system operation sequence is managed by a control microprocessor, which requires low computational performance and hence can be optimized for low power operation. However, some sensors, such as an imager, require high performance for digital signal processing (DSP) operations. For this reason, two ARM® Cortex-M0 processors are located in separate layers with different functionality as follows:

1) The DSP CPU efficiently handles data streaming from the imager (or other sensors), thus is built in 65 nm CMOS (Layer 3) with a large 16 kB non-retentive SRAM (NRSRAM). In such an advanced technology node, the DSP CPU runs faster than the control CPU (fabricated in 180 nm) and accommodates the larger memory capacity that is required for complex DSP operation. However, due to the high leakage current in this process, the SRAM has to be power-gated in standby mode and is non-retentive.
2) The CTRL CPU manages the system using an always-on 3 kB retentive SRAM (RSRAM) to maintain the stored operating program, and is built in low leakage 180 nm CMOS (Layer 4).



	RSRAM	NRSRAM
Topology	Low leakage 10T[10]	Low voltage 8T[11]
Bitcell Area	17.48 μm^2	1.548 μm^2
Standby Power	3.3 fW/bit	14 pW/bit

Fig. 3. SRAM topologies used for (a) NRSRAM, (b) RSRAM, and their comparison.

Memory

Fig. 3 shows the SRAM topologies used for NRSRAM and RSRAM. For RSRAM, a 10T bitcell with high threshold voltage (V_{th}) I/O transistors [11] is used to minimize the leakage power. Although it exhibits very low leakage power (3.3 fW/bit), the large bitcell area of 17.48 μm^2 limits its capacity on Layer 4 to 3 kB due to the large spacing requirements of I/O transistors and older process technology. For NRSRAM, larger capacity is achieved with an 8T SRAM structure [12] with regular-V_{th} transistors, and bitcell area of 1.548 μm^2. However, the low V_{th} of regular transistors in 65 nm technology compared to I/O transistors in 180 nm incurs a high bitcell leakage power of 14 pW/bit, which necessitates the power-gating of the entire NRSRAM array during standby. This means that execution code and data in NRSRAM is lost during standby; therefore execution code is first transferred from RSRAM whenever DSP operation is activated and the DSP processor functions much like a co-processor.

Power Management and Harvesting

Solar cells for energy harvesting and a low-power imager are placed in the top layer (Layer 1) for light exposure. Power consumption ranges from 11 nW in sleep mode up to $\sim$40 μW in active mode. A flexible PMU allows harvesting for perpetual operation from multiple sources, including solar, TEG (Thermo-Electric Generator), and microbial fuel cells. A brown out detector (BOD) monitors the battery voltage and when brown out is detected, it shuts down entire system to prevent Li battery damage due to excessive drainage.

Timer

A gate-leakage-based timer [10] and temperature sensor is also implemented in Layer 1, which is fabricated in 130 nm CMOS for gate-leakage current optimization for timer accuracy. Time tracking with temperature compensation is implemented using this timer, providing a timing reference to synchronize the radios that are included in our second system configuration.

Sensors

A low power temperature sensor and 96 $\times$ 96 pixel low power CMOS image sensor are implemented in Layer 1.

The remainder of this paper is organized as follows. Section III describes the low power I^{2}C communication protocol. Section IV discusses power management in the proposed system including multi-modal harvesting and battery voltage monitoring. A low power optical wake up receiver is presented in Sections V, and VI presents the timer and sensors in the proposed system. In Section VII, two configurations of the system are demonstrated: The first system is the base-line system equipped with a control processor and a dedicated DSP processor with image sensor. The second system replaces Layer 3 (DSP CPU) with a radio layer that includes a near-field radio and pressure sensor interface described in [8]. Finally, Section VIII summarizes and concludes the paper. In this paper, measurement result for each component is presented in each section, while system measurement results are demonstrated in Section VII.

III. Low Power I^{2}C Communication

The die-stacked structure of the proposed sensor platform requires communication among different layers. Due to pad count limitations arising from the 1 mm^3 form factor, the number of wires used for communication is of critical concern. I^{2}C [13] is a widely used industry standard serial communication protocol that only requires two wires—serial clock (SCL) and serial data (SDA)—and is easy to expand with any I^{2}C-compatible devices. However, conventional I^{2}C relies on pull-up resistors, as shown in Fig. 4, which consume mW-order power when the wires are pulled down. Assuming a 1.2 V supply voltage and 1 kΩ pull-up resistance, the average pull-up current for both wires is 1.2 mA, which results in 1.44 mW power wasted simply for pull-up current without considering decoder and driver overhead. This is clearly unacceptable for a sensor platform targeting tens of μW active power. Therefore, a modified communication protocol is required to meet the stringent power budget of the system, while maintaining compatibility to the standard I^{2}C protocol to enable expansion with I^{2}C compatible devices.

Fig. 5 shows the circuit diagram for the proposed low power I^{2}C protocol. Pull-up resistors in conventional I^{2}C act as 1) a pull-up device when the wire is at ground potential and pull-down is released by attached devices, and 2) a keeper for holding high once the wire is fully charged to the supply voltage. To provide the pull-up device function without use of the pull-up resistor, the SCL-low cycle is divided into five sub-cycles where a master device always pulls up SDA in the second sub-cycle and holds high using small keepers. Any attached device can

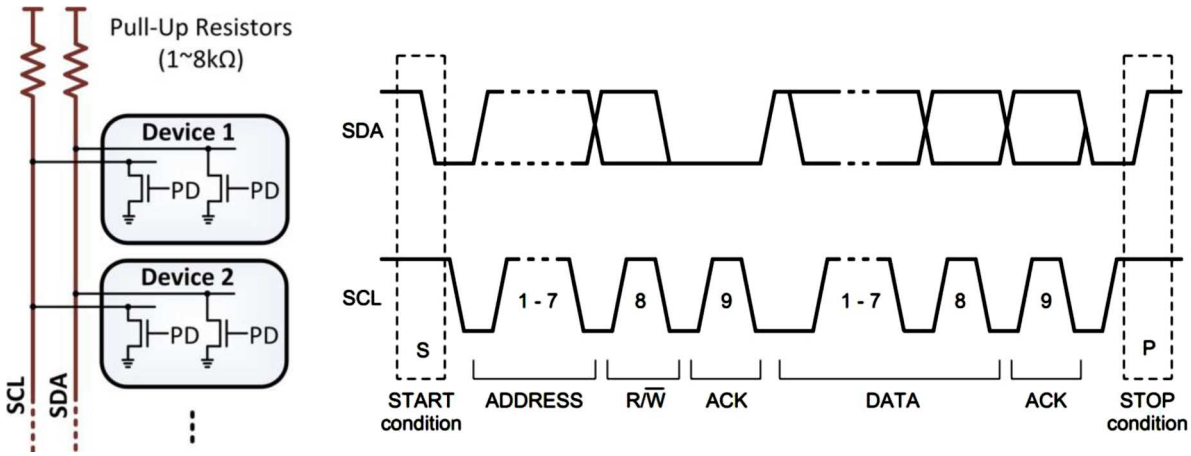


Fig. 4. Conventional I^2C circuit diagram and data transfer waveform [13].

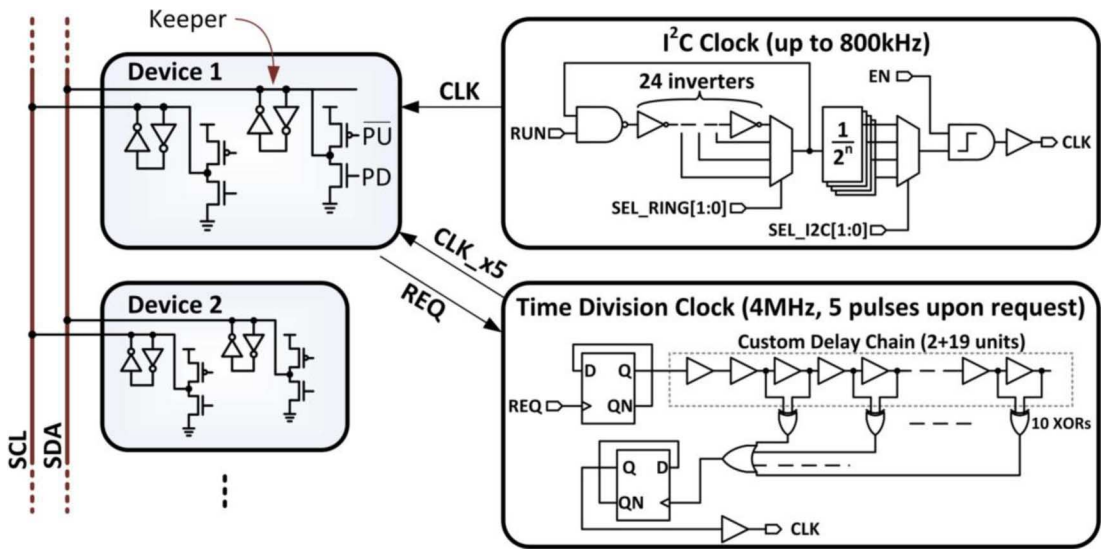


Fig. 5. Proposed low power I^2C circuit diagram.

pull-down in the fourth sub-cycle, which complies with the I^2C standard—SDA can change only when SCL is low and a layer pulling down has the higher priority. The length of the sub-cycle is determined by a sub-cycle clock generator (Fig. 5) and marginal sub-cycles (first, third, fifth) provide margins for die-to-die sub-cycle length variations, which are directly related to the variation in the sub-cycle clock generating circuit. With provided margins, sub-cycle length variation up to 25% can be tolerated.

To provide the keeper function of the removed pull-up resistor, a keeper is attached to each wire. The proposed low power I^2C scheme allows communication between a low power I^2C master device and standard I^2C slave devices if a proper power supply is provided. The only additional cost for such a configuration is occasional short circuit current during the second sub-cycle, when the low power I^2C master device pulls up SDA and the standard I^2C slave device pulls down SDA for acknowledge. Energy overhead due to such short circuit current in I^2C write to slave would not be significant since it occurs only during one sub-cycle and only for acknowledge operation, which is once every 8 bit transmission. However, the overhead is larger for read operations between low power I^2C master and standard I^2C slave. In this case, the master should pull SDA high for each data cycle due to the lack of a pull up resistor, which can generate short circuit current whenever the transferred bit is a 0. Even so, current consumption in this situation is still lower than standard I2C system which employs pull up resistor that continually draws current when SDA or SCL are pulled low. To tolerate a current surge, external power supplies with higher current capacity may be required, which could be provided by simply sharing the power supply for the attached standard I^2C device.

Fig. 6 shows the measured low power I^2C waveform. The figure clearly shows that in each SCL-low cycle, SDA is raised only in the second sub-cycle and pulled down in the fourth sub-cycle, which is most clear in the acknowledge cycle where both pull-up and pull-down operation are performed. Measured energy consumption is 88 pJ/bit, which is more than an order of magnitude lower than 3.6 nJ/bit, the theoretical minimum energy needed to drive the wires in standard I^2C protocol (excluding overhead) for decoding and driving logic at the maximum data-rate in 'fast mode' I^2C, 400 kbps [13].

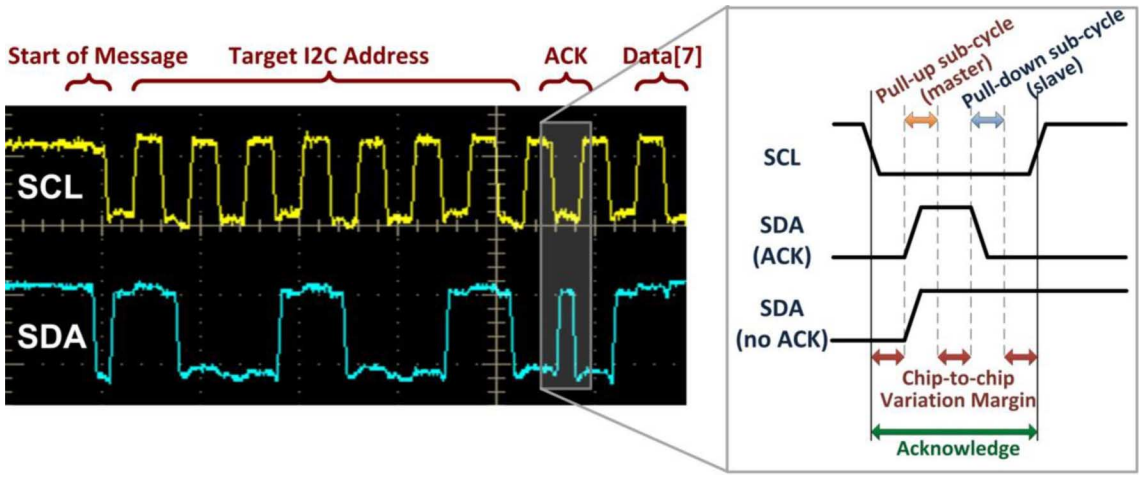


Fig. 6. Measured I^{2}C waveform and illustration of SCL-low sub-cycle.

IV. Power Management Unit (PMU)

The thin-film Li-ion battery in the proposed sensor platform outputs voltages as high as 4.1 V while low power electronics often operate below 0.5 V, resulting in a challenging DC-DC conversion ratio. The PMU must enable both up-conversion during harvesting and down-conversion in the absence of harvesting conditions. Further, it must accommodate a $>1000\times$ spread in current draw between sleep/active modes and low/high harvesting conditions. Having switches that can accommodate 10 s of μA in active mode, while at the same time maintaining high efficiency conversion with load currents as low as single digit nAs in sleep mode, is extremely challenging. Finally, different harvesting sources have varying optimal operating points that change with harvesting conditions. For instance, a solar cell has an open circuit voltage as low as 350 mV in indoor conditions, increasing to 530 mV in sunlight, while a microbial fuel cell (MFC) has an open circuit voltage that tends to fluctuate over time from 500 to 800 mV. These requirements call for the PMU in the proposed sensor platform to be highly adaptive to load current and harvesting source conditions.

The proposed PMU is fully integrated with a chip area of 0.95 mm^2 (Active region: 0.24 mm;^{2} MIM-capacitance area: 0.71 mm^2) and automatically adapts to different harvesting conditions and can be configured to operate with different harvesting sources. The PMU consists of two ladder-type switch capacitor networks (SCNs), as shown in Fig. 7; one for converting between battery and processor voltages (*battery SCN*) and one for converting between processor and harvester voltages (*harvester SCN*). During down conversion, when the processor draws current from the battery, the battery SCN is automatically reconfigured between $5\times$ and $6\times$ modes, providing the ability to adapt to different load currents and battery condition from 3–4.1 V.

During harvesting, both SCNs up convert the harvested voltage and provide current to the processor and battery. The harvester SCN has $2\times$ and $3\times$ modes and is connected to the battery SCN in one of three possible configurations to adapt to different harvesting sources and harvesting conditions. The key challenge in efficient harvesting is to determine the configuration that forces a voltage at the harvester leading to extraction of maximum energy from the harvester. Measurement with a solar cell in Layer 1 showed that the extracted power peaks when the extraction voltage is approximately $0.83\times$ of the open circuit voltage ($\mathrm{V_{OC}}$). However, the $\mathrm{V_{OC}}$ varies between 350 and 500 mV depending on light conditions, and hence the harvest extraction voltage must be adjusted accordingly. In addition, different energy sources have different power profiles leading to the need to adjust the fraction of $\mathrm{V_{OC}}$ at which the harvested power is extracted.

The proposed PMU adapts to different harvesting conditions using a two phase process. First, the battery and harvester SCNs are disconnected for a short monitoring time period. During this time, the harvester develops its open-circuit voltage, which is up converted by the harvester SCN by $2\times$ and $3\times$, and then divided using two reconfigurable, high-impedance fractional voltage dividers, after which the resulting voltage levels are compared to battery SCN voltages to find the optimal harvesting configuration. During the subsequent harvesting time period, the battery and harvester SCNs are connected according to the optimal configuration determined during the monitoring period, and both processor and battery are powered by the harvesting unit. The monitoring/harvesting cycle is repeated every 6 seconds to allow the PMU to adapt to changing harvesting conditions. If there is insufficient harvested energy, the PMU automatically disconnects the harvester SCN from the battery SCN. The voltage dividers can be configured by the processor to adjust to harvesting sources with different power profiles. There is a trade-off between loss in harvesting time and response time to harvesting condition change with the monitoring/harvesting cycle time.

A. DC-DC Down-Conversion Operation

During down conversion, the PMU converts the battery voltage to two voltage domains ($\mathrm{VDD1} = 0.6$ V and $\mathrm{VDD2} = 1.2$ V, nominally) to power the processor and an array of peripherals. The proposed PMU has two operating modes with

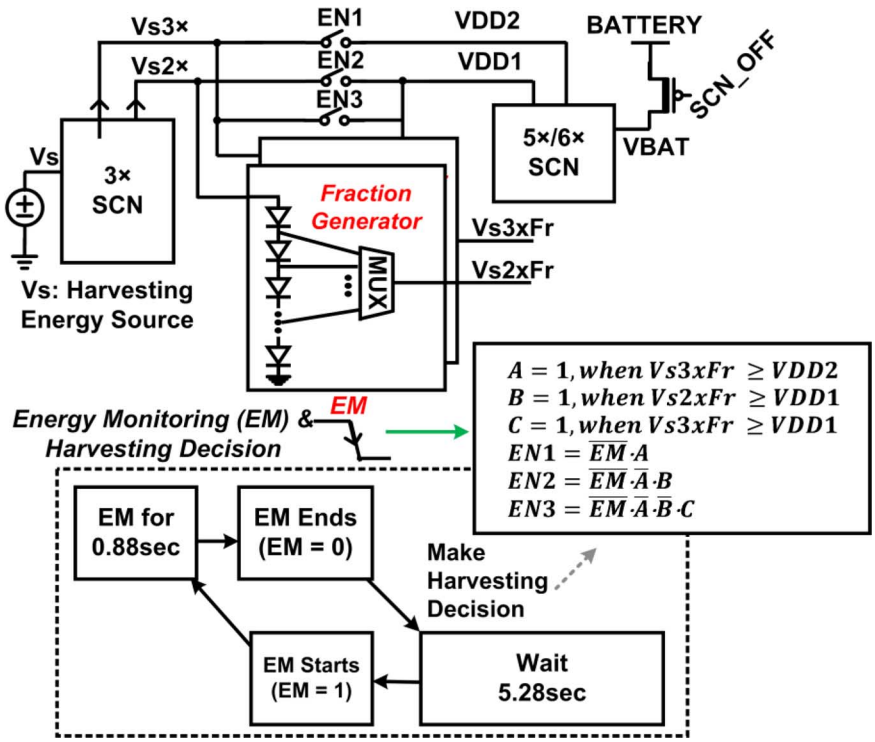


Fig. 7. Proposed overall PMU diagram and adaptive harvesting technique.

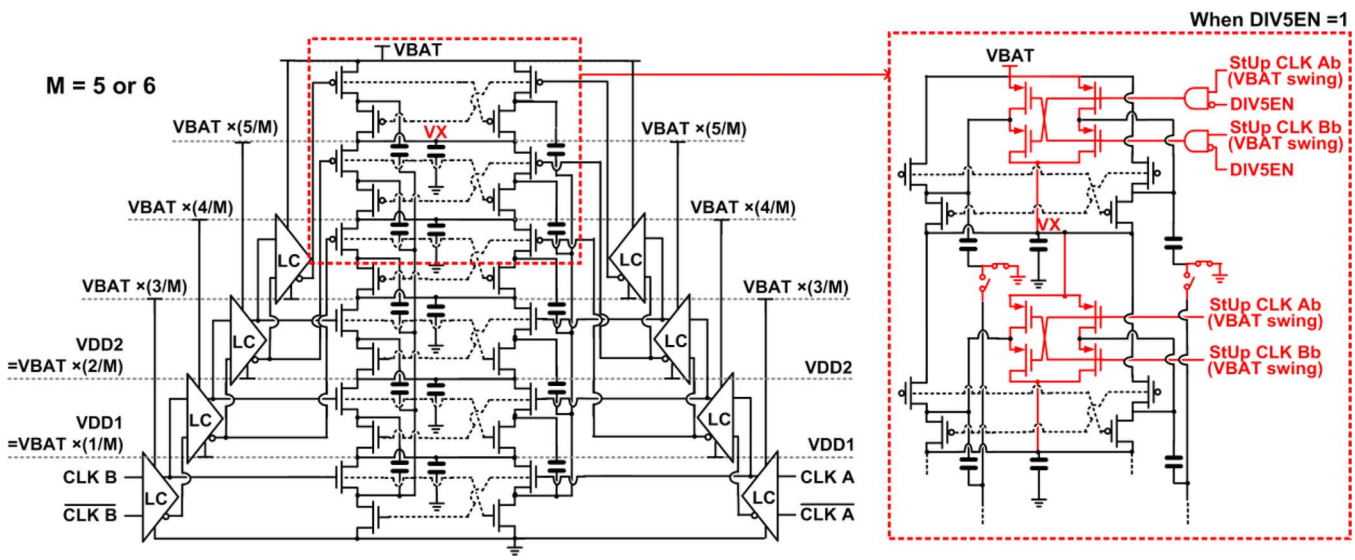


Fig. 8. Two-way phase-interleaved ladder-type SCN with variable $(5\times/6\times)$ conversion ratio. Thick-gate oxide switches for start-up sequence are indicated using arrow FET notation.

vastly different power budgets: 1) sleep mode when the processor is inactive has a current draw of 1–10 nA and 2) active mode when the processor is running has a current draw of 1–10 μA. To efficiently perform DC-DC down-conversion, the PMU uses four different oscillators: a start-up sequence clock (5 kHz, simulated), sleep mode clock (340 Hz, measured), active mode clock (335 kHz, measured), and an additional SCN clock (3.125 kHz, measured) for harvesting in sleep mode. To reduce ripple magnitude on the output voltage levels at a given SCN frequency and capacitance, a two-way phase interleaved ladder is used as shown in Fig. 8.

When the battery SCN starts up for the first time, no charge is stored on internal nodes. Hence, the start-up clock operates at the battery voltage with full amplitude signals and thick-gate oxide switches. Once start-up is completed, the PMU enters operational mode, and the clocks operate with VDD1 amplitude in active mode and VDD2 in sleep mode, driving thin-oxide switches. Using lower clock voltage swing and smaller thin-oxide switches reduces PMU power consumption and increases conversion efficiency. Level conversion is required for driving the different switches in the ladder and is implemented using a chain of level converters as seen in Fig. 8.

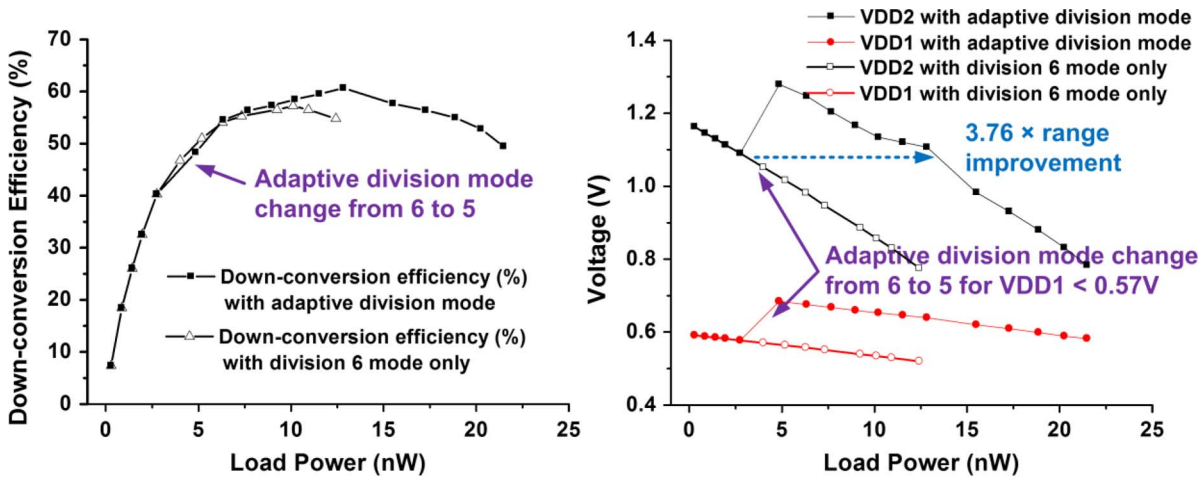


Fig. 9. Measured down-conversion efficiency in sleep mode with VBAT = 3.6 V and 340 Hz sleep mode clock (left). Measured VDD2 and VDD1 with adaptive division mode, and with division 6 mode only (right).

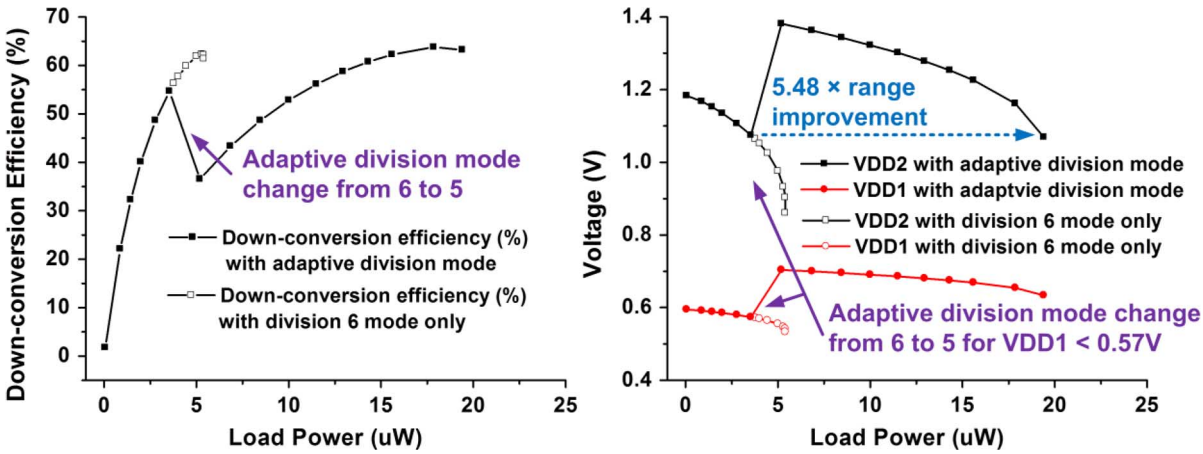


Fig. 10. Measured down-conversion efficiency in active mode with VBAT = 3.6 V and 335 kHz active mode clock (left). Measured VDD2 and VDD1 with adaptive division mode, and with division 6 mode only (right).

The PMU switches between active and sleep mode based on control signals from the processor and timers. The battery has an adaptive conversion ratio of 6× or 5× to address battery voltage variation and a wide range of load power. When 5× is enabled, switches reconfigure the top stage of the ladder such that VBAT and VX are shorted and the bottom plate of the flying capacitor is grounded. This reconfiguration is triggered by two comparators that compare fractions of VDD1 to a voltage [16]. Hysteresis is introduced between the transition to prevent oscillation between the 6× and 5× modes.

The measured power consumption of the sensor platform ranges from <3 nW in sleep mode and up to ∼20 μW in active mode, which can vary with system configuration. Figs. 9/10 shows the down conversion efficiency of the proposed PMU which is nearly equal in sleep mode compared to active mode, due to the use of the VDD1 voltage domain for the SCN clocks in sleep mode. Figs. 9/10 also shows how the configurability of the battery SCN increases the load power range by 3.76×/5.48× for sleep/active modes over the case without this capability (VBAT = 3.6 V). The battery SCN conversion ratio changes from 6 to 5 when VDD1 drops below 0.57 V, and reverts back to 6× when VDD1 exceeds 0.71 V.

B. PMU Up-Conversion for Adaptive Harvesting

During harvesting, the harvester SCN up-converts the harvesting source voltage by 2× and 3×, and connects either of these outputs to the VDD1 or VDD2 ports of the battery SCN (Fig. 7) The two SCNs are connected in three different ways to accommodate harvesting sources with output voltages from 360–800 mV. The open-circuit voltage develops during the monitoring phase, which lasts 0.88 sec. During this phase a highly resistive diode-connected fraction generator (with configurable output voltage from 0.2× to 0.95×) is applied to both the 2× and 3× outputs of the harvester SCN. These two factional OCVs are then compared to VDD1 and VDD2 from the battery SCN according to three possible configurations (Config #1: 3× = VDD1, Config #2: 2× = VDD1, Config #3: 3× = VDD2). The three configurations are rank ordered according to the harvesting voltage that they induce and a configuration in which the fractional voltage minimally exceeds the voltage from the battery SCN is automatically selected to ensure near-optimal energy extraction from the harvesting source.

The proposed method automatically adjusts the harvesting setting in response to the harvester's V_{OC} (addressing different

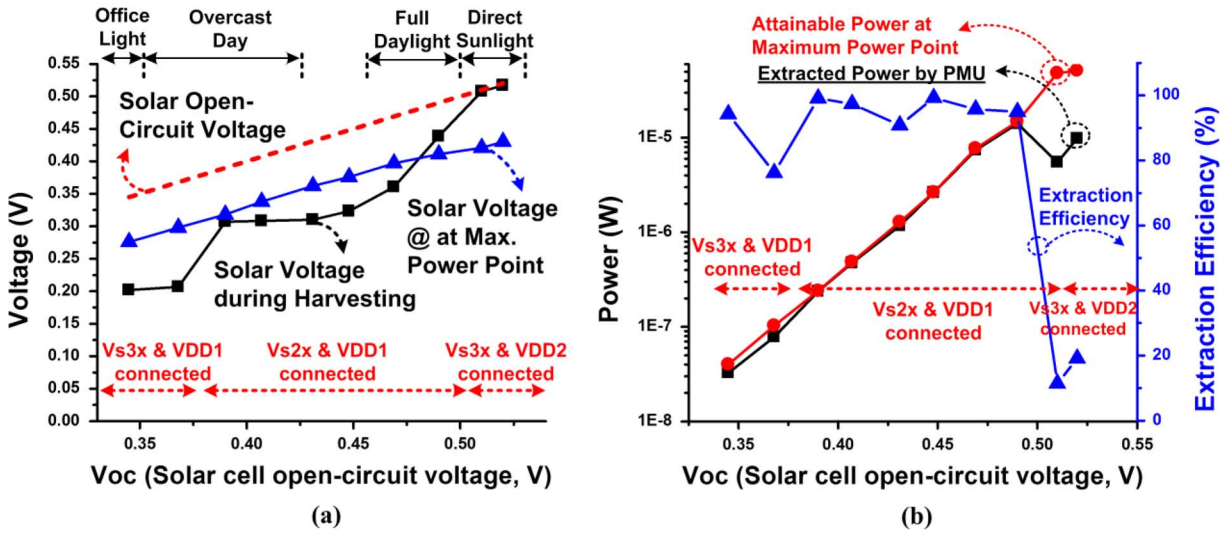


Fig. 11. (a) Maximum power point tracking and (b) harvested power of the proposed PMU for energy harvesting with 1.62 mm^2 solar cell.

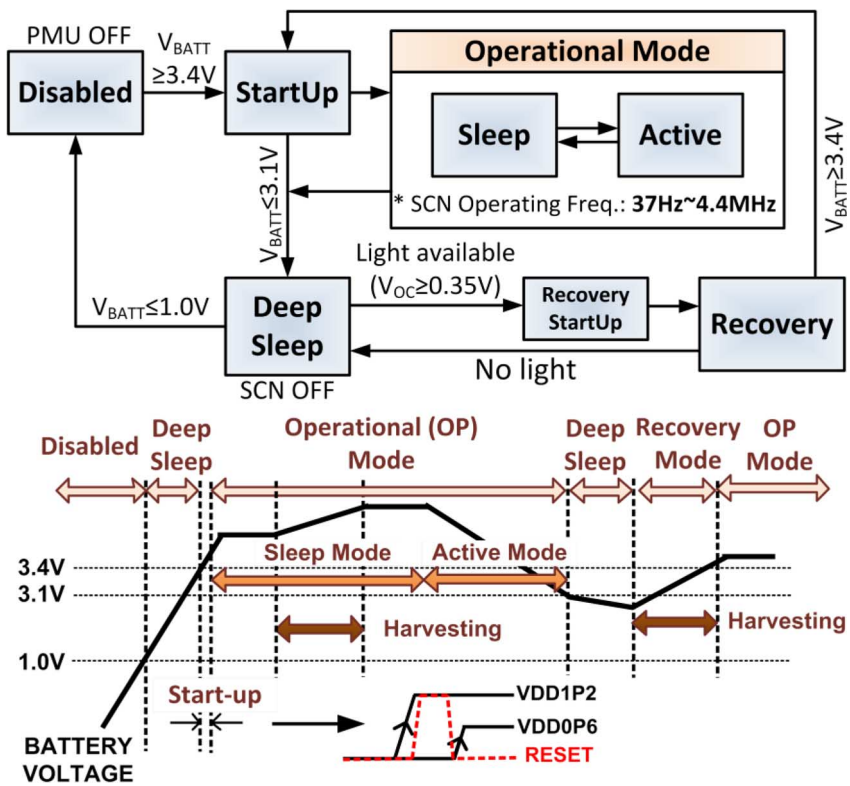


Fig. 12. PMU FSM state diagram and PMU state change along with battery voltage variations.

harvesting conditions), the battery voltage (addressing different battery charge states), and the setting of the fractional generator (addressing different harvesting sources). For example, when battery voltage is 3.0 V and the OCV fraction is 0.65, configuration 1 corresponds to an V_{OC} of 307–462 mV, configuration 2 to 462–615 mV, and configuration 3 to $V_{OC} >$ 615 mV. In a situation with $V_{OC} <$ 307 mV, the harvester is automatically disabled to prevent possible drain through the harvesting unit. Finally, after the monitoring phase, the chosen configuration is established during the harvesting phase, which lasts 5.28 s.

The proposed approach was tested with three harvesting sources: solar cell, microbial fuel cell (MFC), and thermoelectric generator (TEG). The proposed PMU achieves an overall energy harvesting efficiency of 39.8% with an MFC, and 28.1% with a 2.56 cm^2 TEG and 26.9% with a 1.62 mm^2 solar cell. To demonstrate the proposed method for maximum power point tracking (MPPT), we show in Fig. 11(a) how the harvest voltage forced by the PMU tracks the optimum harvesting voltage. As light intensity increases from office light to outdoor lighting, the PMU automatically switches from the first configuration (with force harvest voltage of 200 mV) to the

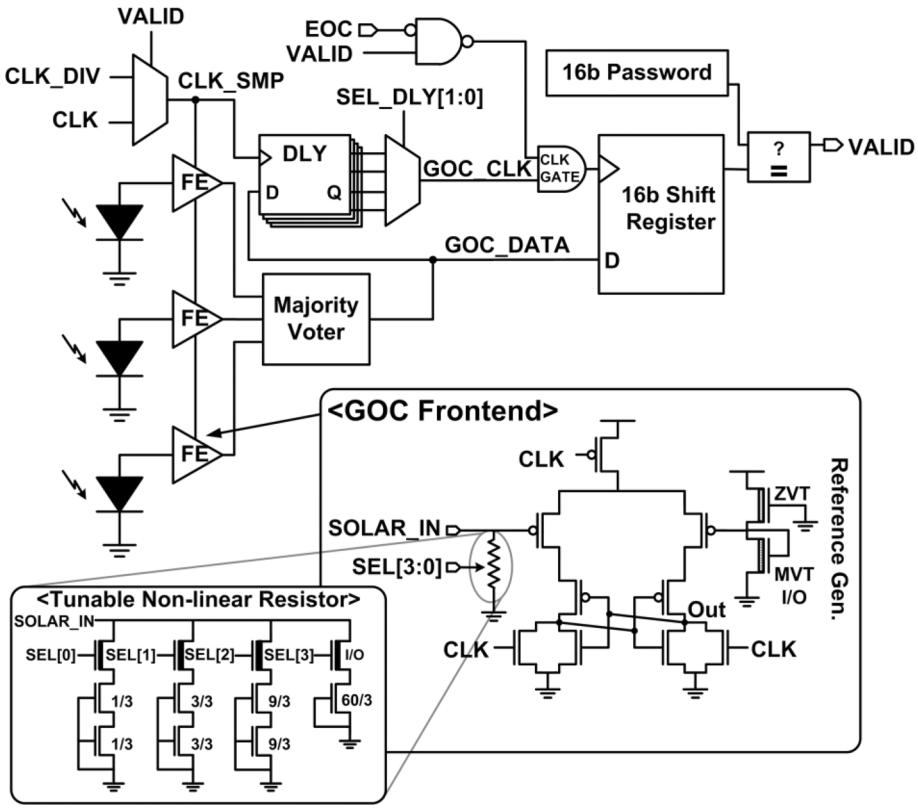


Fig. 13. GOC circuit diagram.

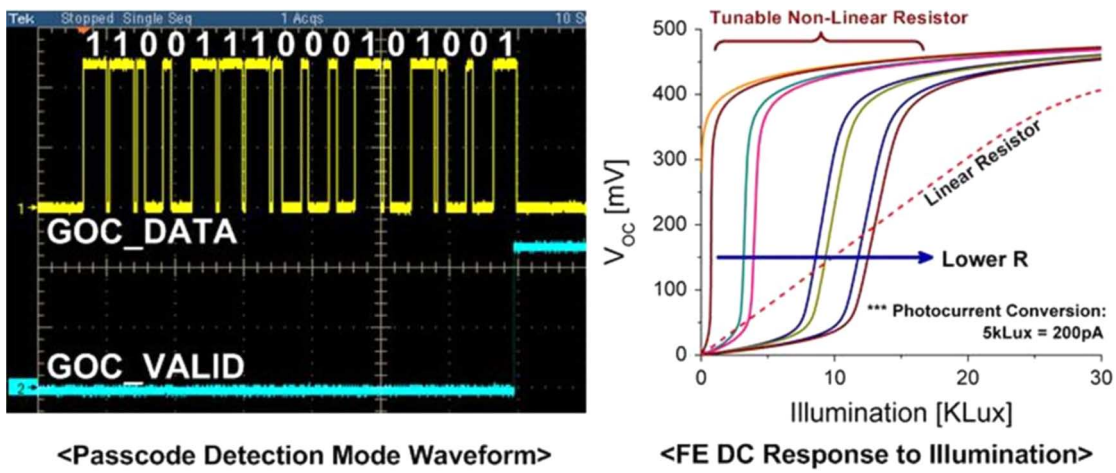


Fig. 14. Measured waveform of GOC operation during passcode detection mode (left). Simulated results for GOC front-end show that non-linear resistance offers 14× sharper slope at the desired 200 mV threshold (right).

second configuration (300 mV). Fig. 11(b) compares the power extracted from the solar cell by the PMU with the maximum attainable power and the extraction efficiency

$$\frac{\text{Extracted power from solar cell by PMU}}{\text{Attainable power at Maximum Power Point}}.$$

For light intensities from office light to full daylight, the average extraction efficiency is 93.5%, with a maximum efficiency of 99.2% and minimum efficiency of 76.1%. When the solar cell is exposed to direct sunlight, Voc increases to 520 mV and the PMU switches to the third configuration (400 mV). However, the current at this light condition reaches up to 100 μA (>2 orders of magnitude higher than in office lighting), exceeding the conversion capability of the PMU. Hence the PMU can no longer force the intended 400 mV harvest voltage, resulting in a drop in extraction efficiency.

C. Battery Voltage Monitoring

A battery voltage monitoring unit [14] is included to detect changes in battery voltage and to allow the PMU to take appropriate action. Fig. 12 shows PMU state transitions in response to battery voltage fluctuations. Once the battery voltage stabilizes above 3.4 V, the PMU enters *Operational* mode and the system is activated. Discharging the battery below 3.0 V due to heavy

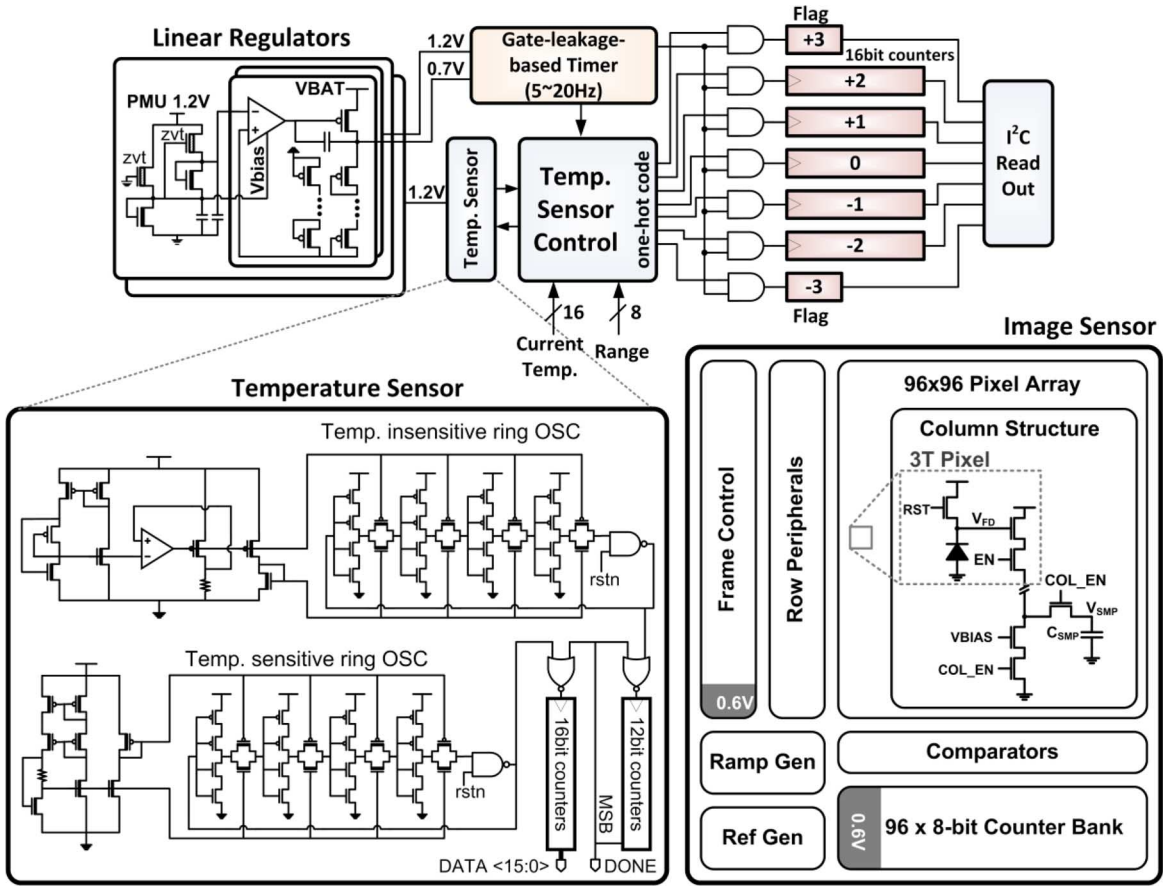


Fig. 15. Circuit diagrams for LDO (top left) and temperature sensor (bottom left), along with the block diagram for time/temperature tracking (top middle).

use or wear-out can incur permanent damage to the Li battery. To prevent this, the monitoring unit detects voltage levels below 3.1 V and the system enters a 185 pW *Deep Sleep* mode where all supplies are turned off. The availability of harvested energy is monitored in Deep Sleep mode and when sufficient light is detected, the system enters *Recovery* mode, recharging the battery from the harvested energy. After the battery has reached a sufficiently high voltage ($>$3.4 V), the system returns to its normal Operational mode and distributes a power on reset (POR) signal to all IC layers by sequentially releasing the 1.2 V and 0.6 V supplies. This sequence is detected by the POR circuit in each IC layer, which forces local reset for proper initialization.

V. Global Optical Communication

GOC serves three critical purposes that enhance the usability of this sensing platform: initial programming after system assembly, re-synchronization during use, and re-programming out of Deep Sleep mode or when the program has become corrupted. At 228 pW standby power, GOC consumes $\sim$20,000$\times$ less power than typical RF wakeup radios (4.4 μW in [15]), which rely on an un-corrupted software stack (defeating the purpose of re-programming). The GOC module consists of a main control block and three redundant front-end receiver circuits for robustness (Fig. 13). The front-end consists of a photodiode, a pull-down resistor for faster response time, and a comparator. The tunable resistor is intentionally implemented with off-state MOSFETs, whose non-linear resistance profile improves light detection sensitivity by 14$\times$ compared to a linear resistor, as seen in Fig. 14. The comparator compares the photodiode's anode voltage to a reference voltage of approximately 200 mV, generated by a 2-T reference generator [16], to determine whether the light level corresponds to a "1" or a "0". The outputs of the three comparators are majority-voted, and this digitized signal, GOC_DATA, is then delayed by a tunable delay chain to generate GOC_CLK. Subsequently, GOC_CLK's rising edge samples GOC_DATA to determine data "1" or "0".

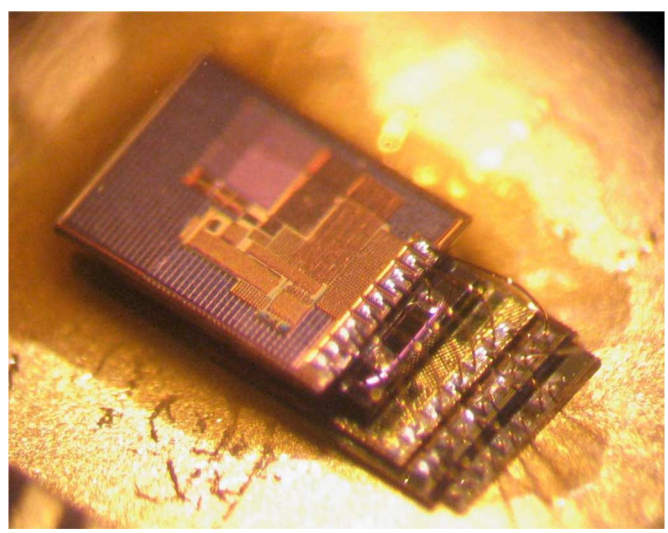


Fig. 16. Photo of proposed 1.0 mm^3 sensing platform.

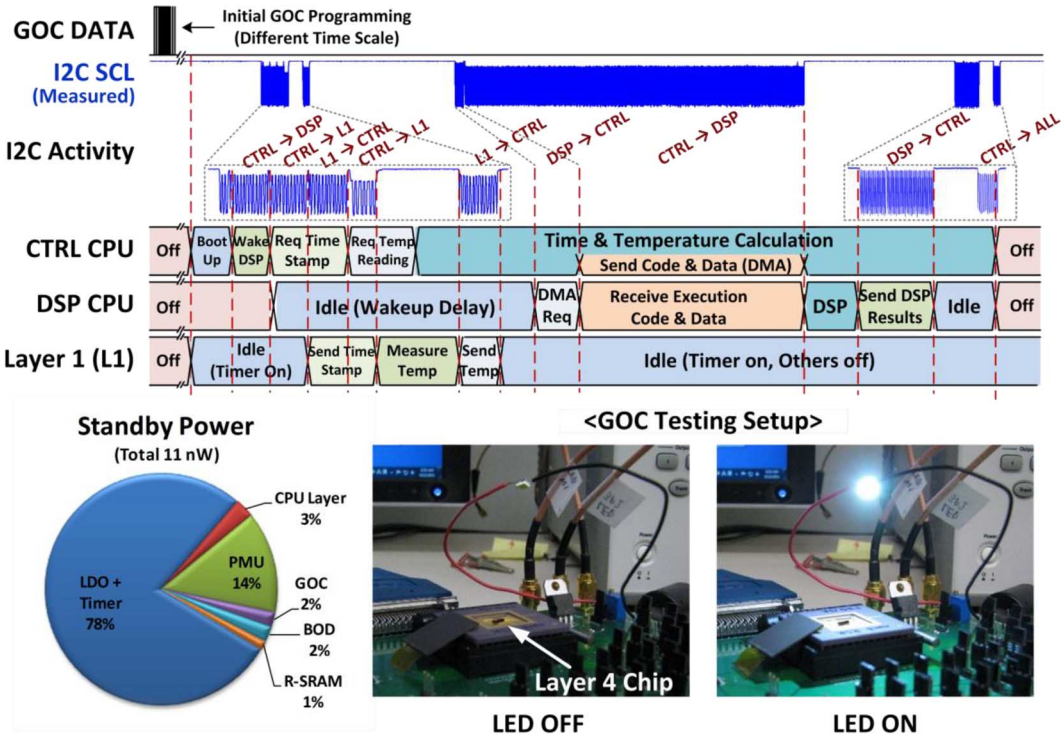


Fig. 17. Measured waveform of the I^{2}C SCL line along with the corresponding usage scenario (top). Measured standby power distribution (bottom left) and testing setup for GOC (bottom right).

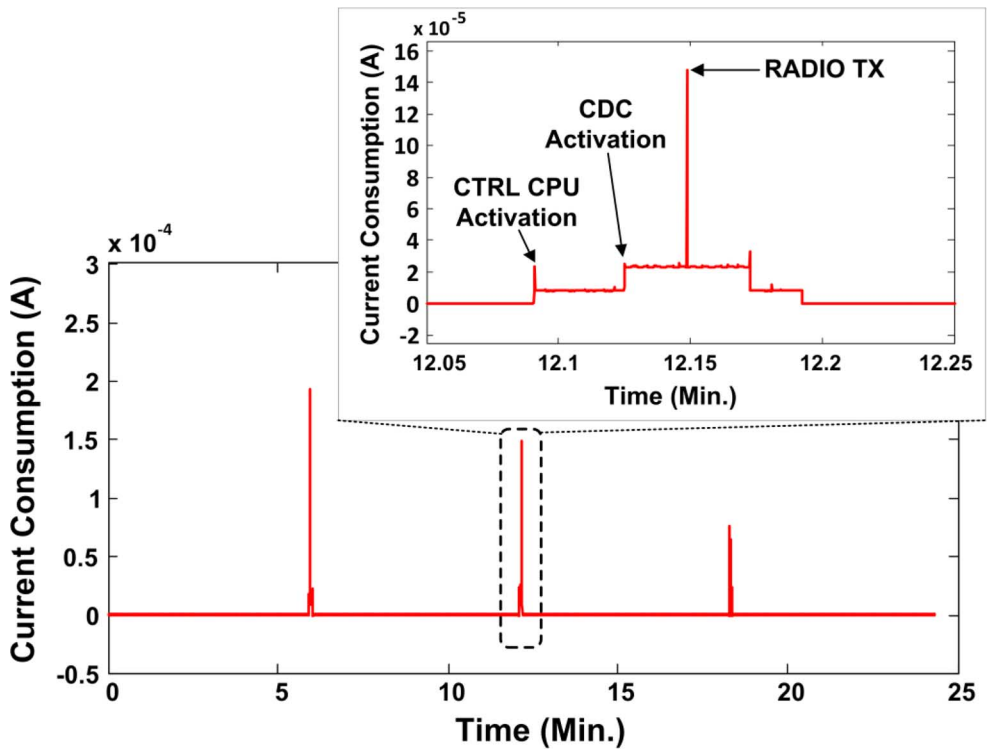


Fig. 18. Measured current waveform of a periodically operating sensor node with a radio layer.

Since the GOC is located in Layer 4, the front-end receivers are placed between bonding pads for light exposure. To prevent false triggers from ambient light, a 16-bit predetermined bit pattern is used as a global passcode to initiate a GOC transaction. Once the passcode is validated, GOC runs at an 8× faster rate to enable higher transmission rate while avoiding the high standby mode power associated with such a clock. Additionally, a local chip-ID/masking scheme allows for selective batch-programming of different groups of sensor nodes. GOC is measured to be operational up to 120 bps and consumes 72 pJ/bit.

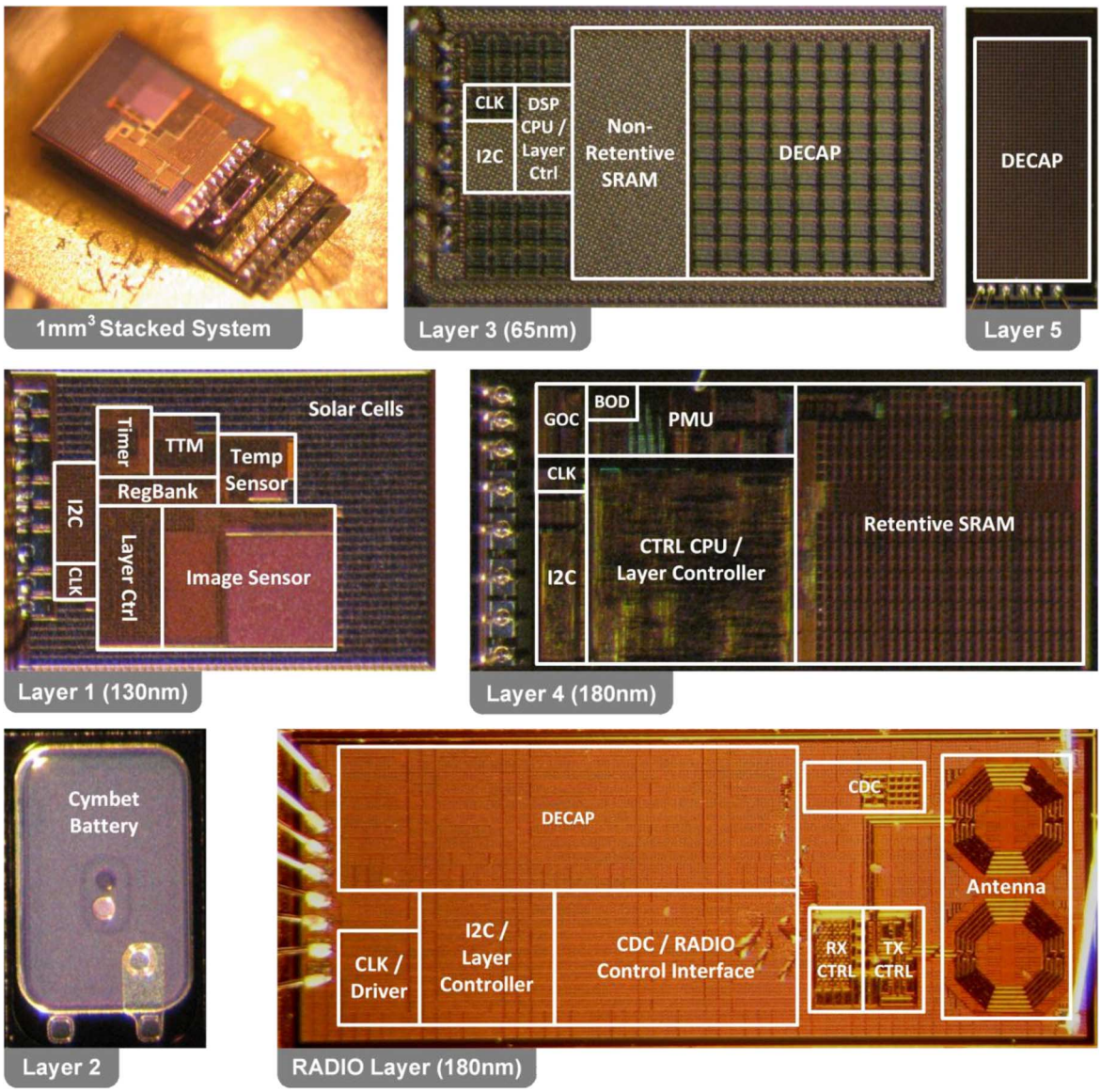


Fig. 19. Photograph of the 1 mm^3 stacked sensor platform (top left) and die micrograph of each layer in the stacked system.

VI. Timer and Sensors

A gate leakage based timer and temperature monitor provide temperature-compensated time tracking, which is critical for synchronizing wireless communication. The timer [10] is augmented with a temperature sensor (Fig. 15) so that temperature compensation and/or calibration can be provided. The temperature sensor includes a reference current generator and a PTAT (proportional to absolute temperature) current generator. The reference current generator provides a constant current over temperature while the PTAT current generator gives current proportional to temperature. Voltage from those current generators is fed to two separate ring oscillators in order to convert current to frequency. The ring oscillator consists of a chain of stacked inverters with transmission gates between the inverters. Voltage from the current generator drives the gates of the transmission gates, changing their resistance and setting the ring oscillator frequency. Since the driving current controlled by the reference current generator does not change over temperature, the frequency of its oscillator is also constant. The output of the temperature insensitive ring oscillator is counted by a 12-bit counter, and its MSB is used to measure the fixed time. For this constant time, a 16-bit counter counts the output of the sensitive one. Thus, temperature information is stored in the 16-bit counter in digital format. This temperature sensor is measured to consume 806 nJ/pt with a standard deviation of 0.51°C.

Also shown in Fig. 15 is a low power, dual-supply 96×96 imager that uses $\mathrm{psub/n+}$ parasitic diodes in the standard CMOS process as photodiodes. A conventional 3-T pixel structure is used to achieve a high pixel fill-factor of 74%. The column source followers are biased in subthreshold to limit the tail currents, and a pulsed control signal activates the source followers only for a short period. The pixel array and the comparators in the 8-bit single-slope ADC use 1.2 V supply for better signal-to-noise ratio, whereas the digital components use 0.6 V supply to minimize switching power. The image sensor consumes 680 nJ/frame.

VII. System Operation

We demonstrate and provide measurement results of the reconfigurable platform implemented in two different systems. The first system is the baseline system consisting of three die whose micrograph is shown in Fig. 16: 1) imager, timer, solar cells; 2) control processor, PMU and 3) DSP processor. Measured waveforms of the SCL wire in I^{2}C in Fig. 17 shows the communication activity among the layers and the state transition graph at bottom describes the operation of each layer. In this trace, dies were connected using board-level connections that are identical to the connections in the stacked system. Also the dies themselves were identical to those shown in the stacked system of Fig. 2, with the exception of added observability circuits to aid measurement. After initial shipping from manufacturing, the sensor node is in sleep mode and can be programmed through GOC as shown by the 'GOC DATA' waveform in Fig. 14. Control CPU Layer then initiates a boot up sequence and also wakes up the DSP CPU Layer. As shown, timestamp and temperature measurement request is sent to Layer 1 and results are transferred back to the Control CPU Layer for temperature-calibrated timestamp calculation. Meanwhile, DSP execution code and data is transferred to the DSP CPU Layer while the Control CPU Layer is performing its operation. This way, the Control CPU Layer and the DSP CPU Layer can concurrently process data. When the DSP Layer completes, its result is sent back to the Control CPU Layer to be stored in retentive memory located on the Control CPU Layer. The Control CPU then places the entire system into standby mode so that the full system consumes minimum power until the next active operation for periodic sensor measurement.

Fig. 17 also shows the power budget of the system in standby mode. Total standby power consumption is 11 nW with the dominant portion consumed by the gate-leakage-based timer. The timer is the only nW-level active unit in the entire system in standby mode and is required to provide an accurate timing reference. Without any harvesting, the integrated 0.6 μAh thin-film battery can support the system in sleep mode for up to 2.3 days. For applications where accurate timing is not required, standby power can be reduced to 2.4 nW with a pW timer [17], allowing 10.5 days of sleep mode operation without energy harvesting.

By taking advantage of the re-configurability of the proposed sensor system, we also demonstrate a second system where the DSP processor layer is swapped with a new layer that includes a capacitance-to-digital converter (CDC) and a near-field radio [8], while all other layers are reused. This configuration represents a sensor node that periodically wakes up to take pressure sensor measurements and transmits measured data through a radio for monitoring of pressure in tumors as an early diagnostic tool for determining chemo-therapy effectiveness Operation of the second system is measured as shown in Fig. 18. The sensor node wakes up every 6 minutes and has current consumption on the order of 3 nA in standby, <5 μA for active mode without radio transmission, and peaks to >10 μA when radio transmission is active. Note that the differences in the current peak height are due to the limited sampling frequency in the long-term trace, which leads to some samples being reported higher than others.

Fig. 19 shows the micrograph of the proposed 1.0 mm^3 sensor system and chip micrograph of each layer in the system.

VIII. Conclusion

A 1.0 mm^3 die-stacked sensor microsystem is demonstrated as a platform for future mm^3-scale sensor applications. Its modular die-stacked structure allows easy extension to additional mm-scale sensors. A new multi-modal energy harvesting scheme enables harvesting from a wide range of energy sources and a battery-voltage dependent power management scheme allows safe operation without battery over-discharge. Low power I^{2}C is proposed to facilitate efficient communication among layers, while remaining compatible with standard I^{2}C devices with proper power supplies. A low power optical communication scheme allows energy efficient programming and synchronization of sensor nodes. These circuit techniques together create an ultra-low power sensor platform, encapsulating two micro-processors, 19 kB memory, and low power image sensors and timers in 1.0 mm^3 volume, creating exciting new opportunities for future mm^3-scale sensor applications.

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Yoonmyung Lee (S'08–M'12) received the B.S. degree in electronic and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2008 and 2012, respectively. During his Ph.D. study, he worked at research labs with Intel Corporation and IBM, exploring novel circuit designs for low power on-die interconnect fabrics and SRAM.

He is currently a research fellow at the University of Michigan, where he researches energy-efficient ultra-low power integrated circuits for low-power high-performance VLSI systems and millimeter-scale wireless sensor systems.

Dr. Lee received the Best Paper Award at 2009 ACM/IEEE International Symposium on Low-Power Electronics Design (ISLPED) and was a recipient of Samsung Scholarship and Intel Ph.D. fellowship.

Suyoung Bang (S'09) received the B.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), South Korea, in 2010. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Michigan, Ann Arbor.

His research interests include switched-capacitor-based DC-DC converter, energy harvesting circuit, and power management unit for ultra-low power sensor system.

Inhee Lee (S'07) received the B.S. and the M.S. degrees in electrical1 and electronic engineering from Yonsei University, Seoul, Korea, in 2006 and 2008, respectively. He is pursuing the Ph.D. degree in University of Michigan, Ann Arbor.

His current research interest includes developing a low-power capacitive energy harvester, a low-power battery supervisory circuit and a mm-scale wireless sensor node.

Yejoong Kim (S'08) received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 2008, and the M.S. degree in electrical engineering and computer science from the University of Michigan, Ann Arbor, in 2012. He is currently working toward the Ph.D. degree at the University of Michigan, Ann Arbor.

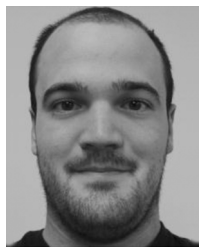
His research interests include subthreshold circuit designs, ultra-low power SRAM, and the design of millimeter-scale computing systems and sensor platforms.

Gyouho Kim (S'12) received the B.S. and M.S. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2009 and 2011, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include ultra-low power and energy-efficient VLSI design.

Mohammad Hassan Ghaed (S'08) received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2008, and the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2008, where he is currently working towards the Ph.D. degree. As a Ph.D. student he was the recipient of Horace H. Rackham graduate fellowship.

In summer 2012, he held a research intern position with Rambus Corp., Sunnyvale, CA. His current research interests include analog, mixed signal and RF-IC design.



Pat Pannuto received the B.S.Eng. degree from the University of Michigan in 2012. He is currently pursuing the Ph.D. degree at the University of Michigan, focusing on wireless and embedded systems.

Prabal Dutta received the B.S. degree in electrical and computer engineering, in 1997, the M.S. degree in electrical engineering, in 2004, from the Ohio State University, and the Ph.D. degree in computer science from University of California, Berkeley, in 2009, where he was an National Science Foundation and Microsoft Research Graduate Fellow.

From 1997 to 2002, he worked in the high-tech industry. Since 2009, he has been an Assistant Professor of Electrical Engineering and Computer Science at the University of Michigan, where he researches systems issues in the design, deployment, and scaling of wireless, embedded, networked, and sensory systems for applications in health, energy, and the environment.

Dennis Sylvester (S'95–M'00–SM'04–F'11) received the Ph.D. degree in electrical engineering from the University of California, Berkeley, where his dissertation was recognized with the David J. Sakrison Memorial Prize as the most outstanding research in the UC-Berkeley EECS department.

He is a Professor of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor and Director of the Michigan Integrated Circuits Laboratory (MICL), a group of ten faculty and more than 60 graduate students. He previously held research staff positions in the Advanced Technology Group of Synopsys, Mountain View, CA, Hewlett-Packard Laboratories in Palo Alto, CA, and a visiting professorship in Electrical and Computer Engineering at the National University of Singapore. He has published over 300 articles along with one book and several book chapters. His research interests include the design of millimeter-scale computing systems and energy efficient near-threshold

computing for a range of applications. He holds 11 US patents. He also serves as a consultant and technical advisory board member for electronic design automation and semiconductor firms in these areas. He co-founded Ambiq Micro, a fabless semiconductor company developing ultra-low power mixed-signal solutions for compact wireless devices.

Dr. Sylvester received an NSF CAREER award, the Beatrice Winner Award at ISSCC, an IBM Faculty Award, an SRC Inventor Recognition Award, and eight best paper awards and nominations. He is the recipient of the ACM SIGDA Outstanding New Faculty Award and the University of Michigan Henry Russel Award for distinguished scholarship. He has served on the technical program committee of major design automation and circuit design conferences, the executive committee of the ACM/IEEE Design Automation Conference, and the steering committee of the ACM/IEEE International Symposium on Physical Design. He has served as Associate Editor for IEEE TRANSACTIONS ON CAD and IEEE TRANSACTIONS ON VLSI SYSTEMS.

David Blaauw (SM'07–F'12) received the B.S. degree in physics and computer science from Duke University in 1986, and the Ph.D. degree in computer science from the University of Illinois, Urbana, in 1991.

Until August 2001, he worked for Motorola, Inc. in Austin, TX, where he was the manager of the High Performance Design Technology group. Since August 2001, he has been on the faculty at the University of Michigan where he is a Professor. He has published over 350 papers and hold 40 patents. His work has focused on VLSI design with particular emphasis on ultra-low power and high performance design.

Dr. Blaauw was the Technical Program Chair and General Chair for the International Symposium on Low Power Electronic and Design. He was also the Technical Program Co-Chair of the ACM/IEEE Design Automation Conference and a member of the ISSCC Technical Program Committee.