7.4 A 915MHz Asymmetric Radio Using Q-Enhanced Amplifier for a Fully Integrated 3×3×3mm³ Wireless Sensor Node with 20m Non-Line-of-Sight Communication

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Enabling long range (>10m) wireless communication in non-line-of sight (NLOS) scenarios would dramatically expand the application space and usability of mm-scale wireless sensor nodes. The major technical challenges posed by a mm-scale form-factor are poor antenna efficiency and the small instantaneous current limit (~10s of μA) of thin-film batteries. We address these challenges in several ways: 1) We found that a magnetic dipole antenna achieves better efficiency at an electrically-small size than an electric dipole, when the antennas are resonated with off-chip lumped components. In addition, the high impedance of electrically-small electric dipoles (~4kΩ compared to 10Ω for the magnetic antenna) requires an impractically large off-chip inductor to resonate. 2) By simultaneously considering the magnetic dipole efficiency, frequency-dependent path-loss, and wall penetration loss, we found that a 915MHz carrier frequency is optimal for a 3×3×3mm³ sensor node in NLOS asymmetric communication with a gateway. This is despite the resulting low antenna efficiency (0.21%) which typically drives mm-scale radios to operate at >>1GHz frequency [1]. 3) In transmit (TX) mode, instead of using a PA and PLL, we utilize a cross-coupled driver to resonate the magnetic antenna at 915MHz with a quality factor (Q) of 110 in order to reduce overall power consumption. 4) In receive (RX) mode, we propose an approach of reusing the cross-coupled driver in a non-oscillating mode to raise the Q of the resonant tank to 300, resulting in 49dB voltage gain at 43μW, thereby replacing a power-hungry LNA and bulky off-chip filter. 5) A sparse pulse-position modulation (PPM) combined with a sensor-initiation communication protocol [2] shifts the power-hungry calibration of frequency offset to the gateway, enabling crystal-free radio design. The complete radio, including the transceiver IC, a 3D antenna, off-chip capacitors, a processor, a power management unit (PMU) and memory, is integrated within a 3×3×3mm³ sensor node, demonstrating stand-alone bi-directional 20m NLOS wireless communication with variable data rates of 30b/s to 30.3kb/s for TX and 7.8kb/s to 62.5kb/s for RX. The transmitter generates -26.9 dBm equivalent isotropically radiated power (EIRP) consuming 2mW power and the receiver has a sensitivity of -93dBm consuming 1.85mW.

The overall architecture of the proposed sensor radio system is shown in Fig. 7.4.1. The 3D magnetic dipole antenna is manufactured using a 3×3×2mm³ circuit board printed on a low-loss Rogers RT/duroid® 5880 substrate. Its 4-loop configuration, constructed from two copper layers and 2mm-height vias, achieves a 0.21% efficiency at 915MHz. The off-chip SMD capacitor C_1 (0.5pF) and the integrated digitally-switched capacitor array C_2 complete a resonant tank with a Q of 110 at 915MHz. The resonant frequency is tuned using C_2 within the 891.4-to-932 MHz range. Figure 7.4.1 shows that the efficiency of a magnetic antenna exceeds that of a more traditional electric dipole antenna for extremely small electrical sizes (< 0.015λ) when resonated with off-chip lump components. Furthermore, an electric dipole typically requires physical separation from the electronics, while the proposed magnetic dipole allows electronics to be stacked on top and bottom, enabling compact integration. The electronics stack, along with three off-chip capacitors, is placed on the top of the antenna while a photo-voltaic (PV) cell and batteries are on bottom (Fig. 7.4.1). This exposes the PV while protecting sensitive electronics from light when coated in black epoxy.

In TX mode, a cross-coupled driver resonates the magnetic antenna at 915MHz with a bias current >100μA. This architecture delivers power to the antenna with an efficiency of 32.4% and replaces the power-hungry PA and PLL. However, open-loop operation results in carrier frequency drift, which we address with a wider frequency search at the gateway at the cost of increased gateway complexity. Because the peak TX current exceeds the thin-film battery current limit, the TX circuits operate from a 0.5μF storage cap (when C_3 and C_4 are series-connected) while the thin-film battery (~4V), under the protection of a current limiter (~10μA), continually charges the storage cap. The relatively long storage-cap recharge time between transmit pulses results in inherent sparsity. We exploit this sparsity to realize a new energy-efficient modulation scheme that conveys multi-rate trellis-coded bits in the form of sparse M-ary PPM. The TX baseband controller supports dynamically adjustable modulation parameters such as the pulse width, number of pulse repetitions, trellis-code rate (¼, ⅓, ½, 1, 2, 3, 4) for error correction, and PPM modulation size M.

In RX mode, we propose a Q-enhancement amplifier (QEA) technique, where the cross-coupled pair is biased in a non-oscillating region (<20μA) as opposed to the oscillation region (>100μA), as shown in Fig. 7.4.2. This raises the Q of the resonant tank to 300 (from 110 when QEA is disabled), resulting in 49dB voltage gain at 43μW (simulated). The QEA replaces the high-power LNA and bulky off-chip channel-select filter. It also avoids the re-radiation of a super-regenerative receiver [3]. The bias current of the cross-coupled pair can be digitally tuned with a tail transistor. Its output signal is further amplified by 17dB using a 2-stage amplifier consuming 870μA from the parallel-connected C_3 and C_4 with a 2V supply. The RX demodulator consists of a 32-stage passive rectifier, 4 S/H capacitors and 2 clocked comparators that collectively consume 250nA from a 1.2V supply. The RX uses binary PPM. The rectifier output is sequentially sampled on S/H capacitors. Once two capacitors (C_{s1} and C_{s2} or C_{s3} and C_{s4}) store the voltage for the 1st- and 2nd-half period of an incoming binary PPM symbol, an associated comparator ($Comp_1$ or $Comp_2$) generates a demodulated bit. This approach eliminates the need for an accurate reference voltage for the comparator.

Based on the 'sensor initiate protocol' [2], the sensor node starts communication by sending a 'header' that consists of multiple pulses with predefined pseudo-random intervals. The gateway tracks and compensates the baseband timing and carrier frequency offset by analyzing the header, then sends a return packet that is precisely synchronized to the sensor node's low-power timer and its carrier frequency. This frees the sensor node from the power-demanding timing and frequency synchronization, greatly lowering its complexity and power consumption. Using this synchronized return packet, the gateway can further notify the sensor node of the optimal modulation parameters (e.g., coding rate, pulse width, etc.), enabling a graceful tradeoff in link distance vs. data-rate. We realized a real-time, fully functional communication protocol using a gateway implemented on an USRP FPGA.

The transceiver chip (2.23×1.2mm²) was implemented in 0.18μm CMOS and integrated in a complete 3×3×3mm³ sensor node, including processor, PMU and memory. When operating using two 2μAh batteries, the stand-alone sensor achieved 20m wireless communication in actual indoor environments (Fig. 7.4.4). Measured waveforms show the header and data TX from the sensor node, packet detection by gateway, gateway transmission of a return packet, and sensor detection of the return packet. Figure 7.4.5 shows the performance of the transceiver chip measured wirelessly. EIRP of the sensor node when transmitting a continuous tone was measured using a horn antenna (LB-530-NF) at 2.17m away and ranged from -45.9 to -26.1dBm for 0.52-to-2mW TX power consumption. Sensor RX sensitivity was measured from wirelessly received packets after initially transmitting a sync header to the gateway and delaying for a predefined time (real-time protocol), where the available power at the sensor node antenna was measured using a reference antenna close to the sensor node. The receiver has a sensitivity of -93dBm for 10^{-3} BER, which can be tuned by varying the bias current, demonstrating the effectiveness of QEA. Frequency selectivity of the receiver was tested by measuring the degradation in BER of the 915MHz data transmission due to a blocker at 3, 5, and 10 MHz frequency offsets and shows the effectiveness of the QEA. Figure 7.4.6 shows the comparison with recent work. Figure 7.4.7 shows the die micrograph.

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[2] Y. Shi, et al.,"A 10mm³ Syringe-Implantable Near-Field Radio System on Glass Substrate," *ISSCC*, pp. 448-449, Feb. 2016.
[3] J. Bohorquez, et al., "A 350 μW CMOS MSK Transmitter and 400 μW OOK Super-Regenerative Receiver for Medical Implant Communications," *IEEE JSSC*, vol. 44, pp. 1248-1259, April 2009.

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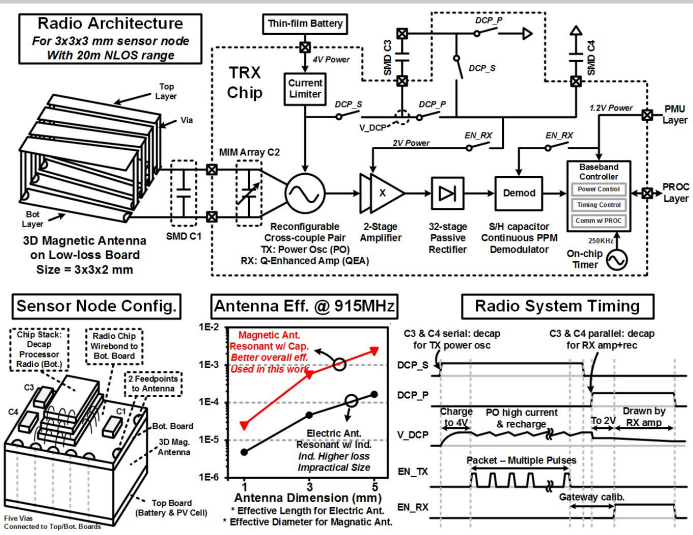

Figure 7.4.1: Architecture and timing of proposed 915MHz radio for 3×3×3mm³ sensor node.

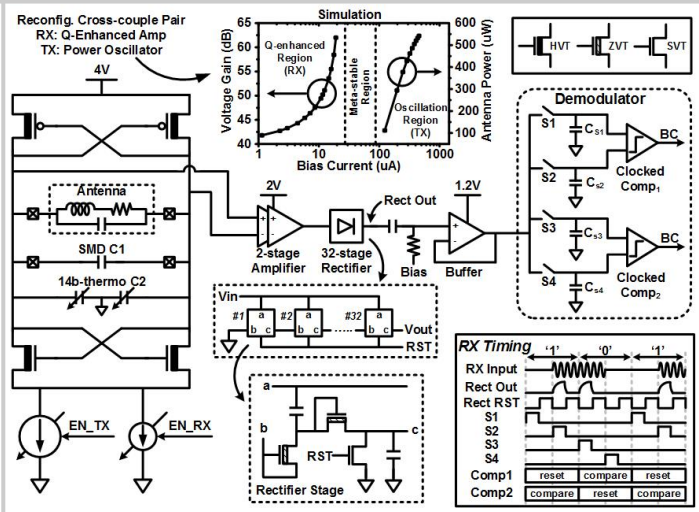

Figure 7.4.2: Transceiver circuits utilizing a re-configurable cross-coupled pair, which functions as power oscillator in transmit mode and Q-enhanced amplifier in receive mode.

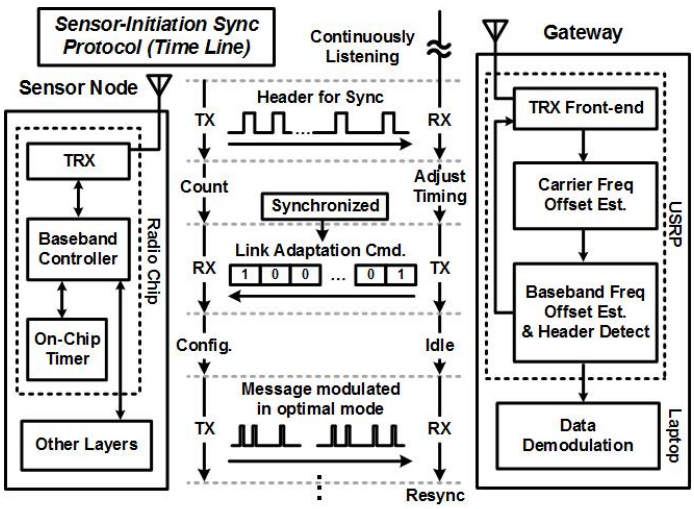

Figure 7.4.3: Adaptive sensor-initiation synchronization communication protocol.

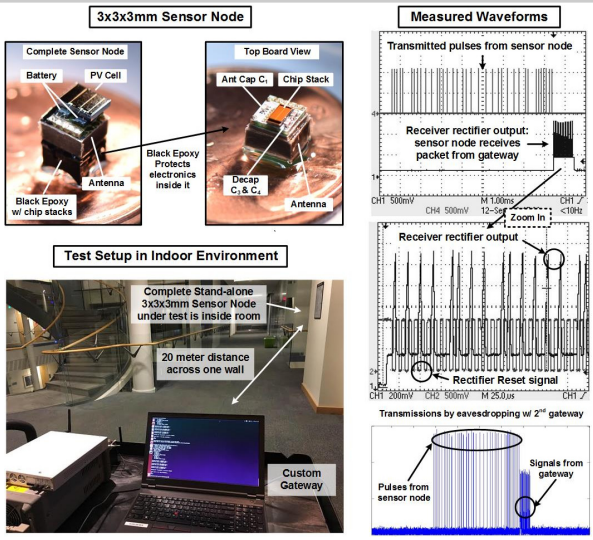

Figure 7.4.4: Measurement setup where complete 3×3×3mm³ sensor-node system communicates with custom gateway.

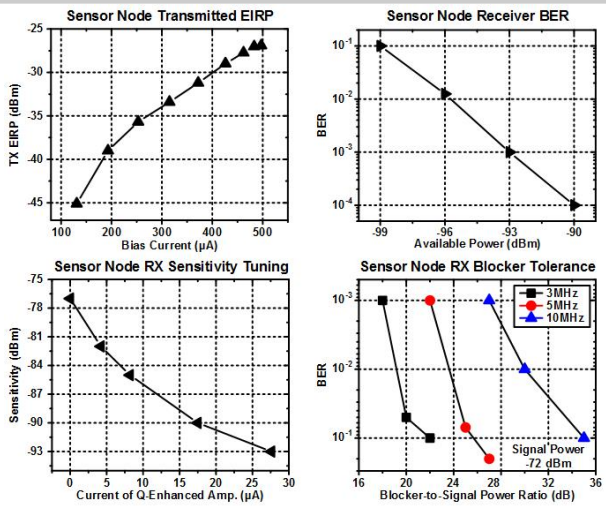

Figure 7.4.5: Wireless measurement results. TX EIRP was measured at 2.17m. RX sensitivity was measured after initially transmitting a header to the gateway and performing gateway synchronization.

		This Work	JSSC 2015 [1]	JSSC 2009 [3]
Technology		180 nm	65 nm	90 nm
Overall Dimension		3x3x3 mm³ Complete Sensor Node (incl. Radio Chip + 3D Ant.)	3.7x1.2 mm² Radio Chip + Integrated Ant.	2x1 mm² Radio Chip (not incl. Loop Ant.)
Antenna		3x3x2 mm³ 3D Magnetic Antenna	Integrated Antenna	2.3x2.4 cm² Loop antenna
Carrier Frequency		915 MHz (TRX)	60GHz (TX) 24GHz (RX)	402-405MHz (TRX)
Measured Range		20m (NLOS)	50 cm	N/A
TX	EIRP (Tone) Testing Method	-26.9 dBm Wireless Testing Incl. 3x3x2 mm³ Ant.	N/A	-37.4 dBm **** Wireless Testing Incl. 2.3x2.4 cm² Ant.
	Peak Power (Tone)	2 mW	11mW **	350 μW
	Efficiency	32.4% *	N/A	N/A
	Modulation	M-ary Pulse-Pos. Mod.	Multi. Pulse-Pos. Mod.	MSK
	Average Power	60.6 μW	N/A	350 μW
	Data Rate	30bps - 30.3kbps	1.2Mbps - 12Mbps	120 kbps
RX	Technique	Q-Enhanced Amplifier	Backscatter	Super-Regenerative
	Modulation	Binary Pulse-Pos. Mod.	Pulse-Pause Mod.	Sync. OOK
	Sensitivity Testing Method	-93 dBm Wireless Testing Incl. 3x3x2 mm³ Ant.	-10.5 dBm Wired Testing Signal Gen. as Input	-99 dBm Wired Testing Signal Gen. as Input
	Power	1.85 mW	1.5 μW ***	400 μW
	Data Rate	7.8kbps - 62.5kbps	6.5 Mbps	40 kbps

* Calculated based on measured results: -26.9dBm EIRP, 2mW TX power, antenna eff. 0.21% and directivity 1.5
** Calculated based on simulated results: 250pC total charge for 3 pulses (width 680ps) from 0.9V supply
*** Calculated based on measured results: -48dBm received power at 20 cm away at 406MHz
**** Measured stand-by power reported

Figure 7.4.6: Comparison with prior work.

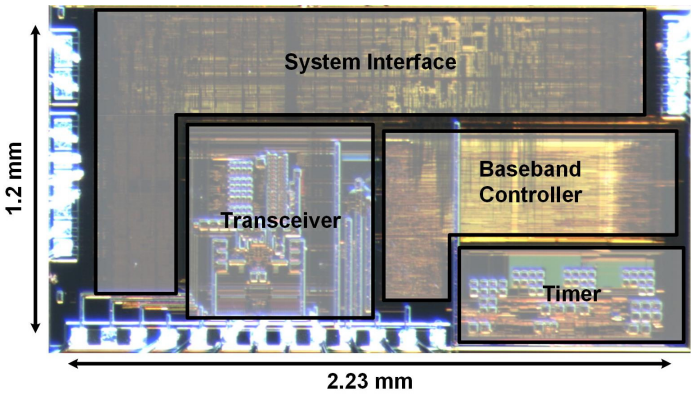

Figure 7.4.7: Die micrograph.

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