8.4 A 2.5ps 0.8-to-3.2GHz Bang-Bang Phase- and Frequency-Detector-Based All-Digital PLL with Noise Self-Adjustment

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Digital PLLs are popular for on-chip clock generation due to their small size and technology portability. Variability tolerance is a key design challenge when designing such PLLs in an advanced CMOS technology. Environmental variations, such as mismatch, process, supply voltage, and temperature (PVT) perturb device characteristics and result in performance changes, such as DCO gain and noise. Another consideration is the wide range of operating modes in which modern digital circuits (e.g., processors) operate. For instance, a clock generator for a processor may produce a range of frequencies from tens of MHz to several GHz depending on required processor performance. In low-frequency mode, the power consumption is more pronounced than the noise. Therefore, we seek to design a PLL that is both insensitive to environmental variations, as well as reconfigurable to changing noise and power specifications.

Conventional approaches [1-3] have focused on optimizing PLL loop bandwidth to minimize overall noise. In this way, the overall noise can be optimized within a given power level. However, with prior approaches, it was not possible to trade-off the power consumption with the noise specification. Furthermore, the period jitter, which is mostly governed by DCO noise, could not be optimized. A multiplying DLL (MDLL) is an attractive architecture to minimize integrated phase noise, but it suffers from limitations, such as a limited multiplication ratio and large peak-to-peak period jitter at the edge injection [4].

This paper introduces a nested frequency locked-loop (FLL) architecture, whose gain is accurately controlled by a capacitor ratio in order to keep the PLL bandwidth insensitive to variations. In addition, the noise of the FLL is independent of the delay cell, but dependent on a current reference so that the DCO noise is programmable independent of the oscillation frequency. A noise-detector block, using statistical characteristics of a bang-bang PFD (BBPFD) output, is employed to efficiently sense DCO noise. The PLL dynamically reconfigures the DCO noise from 2.5-15ps and self-adjusts its power from 1.7-5mW according to the noise specification.

Figure 8.4.1 shows the conceptual schematic of an oscillator using switched capacitor-based frequency feedback [5]. The frequency generated by a voltage-controlled oscillator (VCO) is sensed as the effective resistance of a switched capacitor. A feedback current (I_F) is generated by regulating the effective resistance with M1 (Fig. 8.4.1 bottom left). Then, I_F is compared with input current (I_{IN}), which is generated by regulating an on-chip resistor R_0 with M2. Finally, F_{OUT} is locked to a frequency that equalizes I_F to I_{IN}. Assuming the voltages on R_0 and C_{SW} are equal, the frequency becomes $1/R_0C_{SW}$. The noise of the FLL is also calculated in Fig. 8.4.1. The sampling switch with on-resistance of R_S generates noise whose power spectral density is (1). Due to the sampling operation, the noise is aliased and folded by the sub-sampling ratio, n. The equivalent current noise of the switched capacitor can be expressed as (4) and its fraction is delivered to M1 (5). Finally, the phase noise from the noise of the switched capacitor can be expressed by (6). As the VCO noise is high-pass filtered by the FLL loop bandwidth, the FLL output noise is dominated by the noise of R_0 and the switched-capacitor feedback circuit as in the following equation:

$$L(f) = \alpha^2 f^2_{OUT}(4kT\gamma + 4kT) / I_{IN}V_R f^2$$

Here k, T, γ, and V_R are Boltzmann's constant, temperature, transistor noise coefficient and voltage on R_0 and the switched capacitor. Also, α is the current division ratio at the branch of the source of M1 and M2. The phase noise of the proposed oscillator is inversely proportional to the input current, defined by V_R/R_0. Therefore, the key result is that the DCO phase noise can be reconfigured without impacting the oscillation frequency by changing R_0 and C_{SW}, while maintaining a constant R_0C_{SW} product.

In order to dynamically adjust DCO noise, a noise detector using statistical characteristics of a phase detector output is utilized, as shown in the block diagram of Fig. 8.4.2. Assuming a high resolution $\Delta\Sigma$ modulator, the DCO frequency is centered at $M \times F_{REF}$ and toggles by $K_{DCO}(K_P + K_I)$, which results in the limit cycle of the PLL. Therefore, the probability density function (PDF) of the phase error (ϕ_{err}) is composed of two Gaussian distributions of DCO noise separated by the phase limit cycle, as shown in the bottom left of Fig. 8.4.2. The shaded region of the PDF represents the possibility of generating an inverted BBPFD output owing to DCO noise. The presence of consecutive 1s or 0s at the output of the BBPFD is an indication of that possibility (since, in the absence of noise, the BBPFD output should alternate between 0 and 1 every reference cycle). The noise detector counts the number of consecutive 1s and 0s and accumulates the results over N reference cycles. The output of the noise detector, N_{CNT}, is compared with the input noise reference, N_{REF}, and the DCO noise controller adjusts R_0 and C_{SW} to lock N_{CNT} to N_{REF}. An example transient locking process is shown in Fig. 8.4.3. First, the phase and frequency of the proposed PLL locks to the target by tuning C_{SW} with C_{CON}. After phase lock is achieved, the noise-locking loop is enabled and invokes a binary search for the R_0, C_{SW} combination that matches N_{CNT} to N_{REF}. The amplifiers shown at bottom right of Fig. 8.4.2 set V_{GP} and V_{GN}. Their bandwidth is smaller than the PLL loop bandwidth so that their noise is filtered out by the PLL.

The frequency tuning curve of the proposed DCO is highly linear and invariant to supply and temperature changes since DCO frequency is explicitly defined by R_0 and C_{SW}. Fig. 8.4.4 shows the frequency tuning curve of the proposed DCO compared with the conventional DAC+VCO approach. Due to the non-linear frequency tuning curve of a current-starved VCO, the frequency tuning curve of DAC+VCO is highly non-linear despite of the linearity of the DAC. On the other hand, the proposed DCO provides a highly linear frequency tuning curve under a wide range of PVT variation, which helps to keep the loop bandwidth constant and enables accurate noise locking.

A test chip was fabricated in 28nm FDSOI with area of 0.049mm^2. The left of Fig. 8.4.5 shows the reconfiguration of phase noise when changing the power consumption from 1.7-5mW, yielding an integrated jitter ranging from 15-2.5ps. The function of the noise detector is validated by changing the DCO gain and noise as shown Fig. 8.4.5 (right). The increase in proportional path gain (C_{PROP}) increases ϕ_{Imt} and reduces N_{CNT}/N.

The phase noise graph of the proposed DPLL is depicted in Fig. 8.4.5 (bottom). Fig. 8.4.6 presents the performance summary and comparison to prior digital PLLs that use a ring oscillator. The proposed digital PLL provides wide range of power and phase noise configurability, and shows a competitive figure-of-merit. Note that while some prior art employs a >200MHz frequency reference, which helps in filtering the DCO noise, the proposed work uses a more cost effective 50MHz reference.

Acknowledgements:
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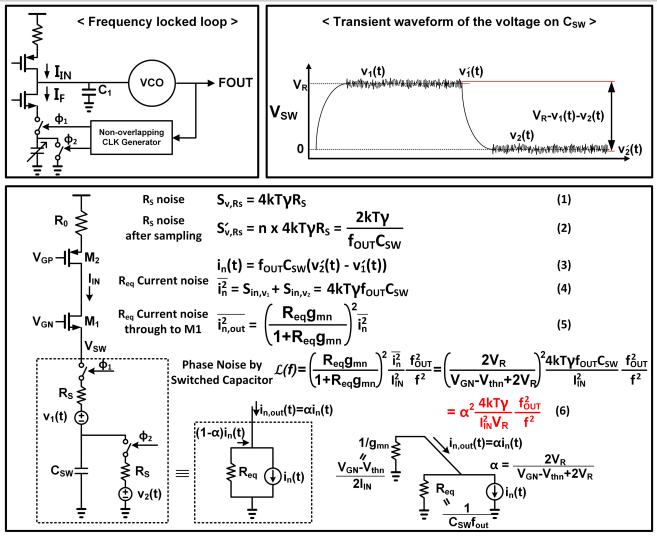

Figure 8.4.1: Frequency locked loop used as a noise reconfigurable DCO in the proposed digital PLL and its noise calculation.

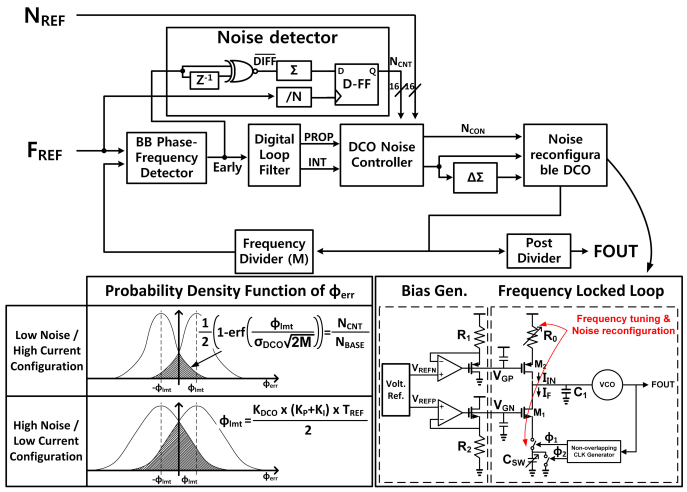

Figure 8.4.2: Block diagram of the digital PLL (top), schematic of the DCO (bottom right) concept of the noise detector using probability density function of the phase error (bottom left).

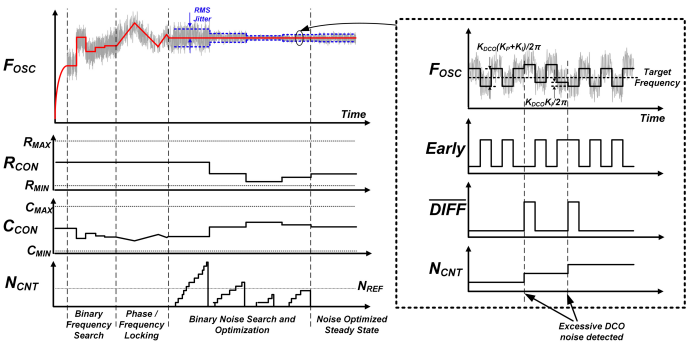

Figure 8.4.3: Locking transient of the DPLL (left) and signals in the noise detector during noise optimization phase (right).

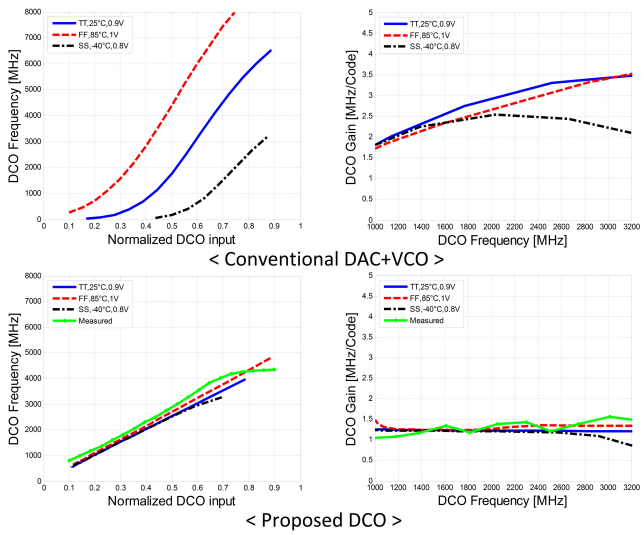

Figure 8.4.4: Measured and simulated DCO frequency tuning curve and gain of conventional DAC+VCO (top) and the proposed DCO (bottom).

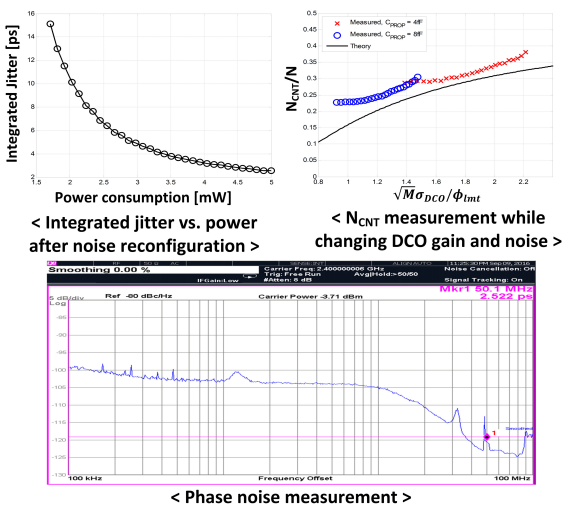

Figure 8.4.5: Integrated jitter after power and noise reconfiguration (top left), measurement results of noise detector output, while varying the DCO gain and noise (top right) and phase noise measurement result (bottom).

	This work	Yeh, ISSCC16	Huang ISSCC14	Kim VLSI15	Crossly CICC10	August ISSCC12	Elshazly ISSCC12		Kim ISSCC16
Output Frequency (GHz)	0.8-3.2	3.2	2.4	1.6	0.2-3.8	0.2-3.2	0.8-1.8		2.4
Oscillator Type	Ring	Ring	Ring	Ring	Ring	Ring	Ring	MDLL	MDLL
Reference Frequency (MHz)	50	200	26	266	300	N/A	375	375	75
RMS Integrated Jitter (ps)	3 @ 1GHz 2.7 @ 1.6GHz 2.52 @ 2.4GHz	3.85	2.418	2.8	2.13*	3.1-14	3.2	0.4	0.7
Integration Range (MHz)	0.1 – 100	N/A	0.01-40	0.01-2	N/A*	0.01-100	0.01-100	0.01-100	0.01-40
Power Consumption (mW)	2.5 @ 1GHz 3.8 @ 1.6GHz 5 @ 2.4GHz	2.915	6.4	2.7	1.98	0.7-3.4	0.9	0.6	0.43
Noise Reconfiguration	DCO Noise & Pwr	N/A	N/A	N/A	PLL Loop Bandwidth	N/A	N/A	N/A	N/A
Figure of Merit (dB)	-225.1-226.5	-224	-221.6	-226.7	-230.5	-224.8 ~ -218.6	-228.59	-248.7	-246.7
Area (mm²)	0.049	0.0216	0.013	0.019	0.026	0.017	0.2	0.2	0.024
Technology	28nm SOI	40nm	40nm	65nm	65nm	22nm	130nm	130nm	28nm

Figure 8.4.6: Performance summary of the proposed digital PLL and comparison to prior art using a ring oscillator or a multiplying DLL.

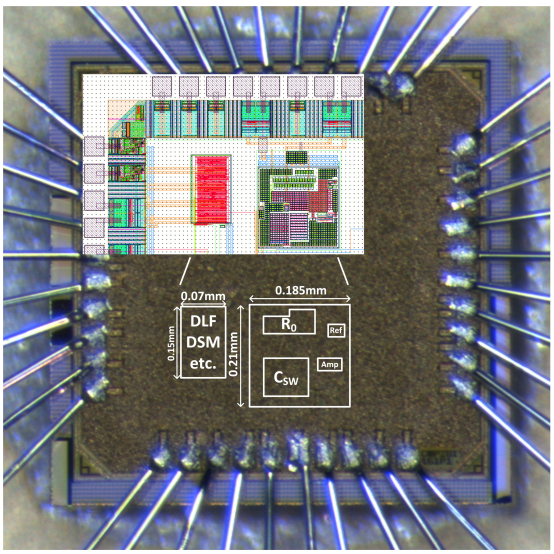

Figure 8.4.7: Die photo of the proposed digital phase-locked loop.

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