5.8 A 4.7nW 13.8ppm/°C Self-Biased Wakeup Timer Using a Switched-Resistor Scheme

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Miniaturized computing platforms typically operate under restricted battery capacity due to their size [1]. Due to low duty cycles in many sensing applications, sleep-mode power can dominate the total energy budget. Wakeup timers are a key always-on component in such sleep modes and must therefore be designed with aggressive power consumption targets (e.g., <10nW). Also, accurate timing generation is critical for peer-to-peer communication between sensor platforms [1]. Although a 32kHz crystal oscillator can provide low power [2] and accurate long-term stability, the requirement of an off-chip component complicates system integration for small wireless sensor nodes (WSNs).

As a result, conventional on-chip oscillators for WSN applications utilize RC time constants, which show relatively accurate frequency stability compared to transistor-delay-dominated ring oscillators. Conventional RC oscillators periodically reset a capacitor using an RC time constant and comparator [3,4]. However, a power-hungry fast continuous comparator is needed to render its own delay negligible compared to the RC time constant and ensure good frequency stability. A timer using a frequency-locking technique to allow an ultra-low-power amplifier to replace the comparator is proposed in [5]. However, oscillation frequency cannot be scaled down due to the resistor size, which limits the minimum power consumption. For example, even with a relatively large 55MΩ resistor occupying 0.2mm^2 in 0.18µm CMOS, the topology consumes 18.2nW at 1V switching amplitude.

To address this challenge and achieve a WSN timer with single-digit nW power consumption, we propose a new timer using a duty-cycled resistor scheme to increase resistance without impacting area. By generating the duty cycle using the frequency from the timer itself, an accurate on/off ratio is ensured. In addition, a current-reuse scheme is proposed to save power and also eliminates the need for chopping the bias current. Finally, a self-biasing technique is proposed to ensure stable operation and low power consumption across process-voltage-temperature (PVT) variations. Using these techniques, the timer achieves 13.8ppm/°C (–25 to 85°C) at 3kHz and consumes 4.7nW while showing less than 1.5× power variation across temperature.

Figure 5.8.1 explains the concept of the proposed timer. A voltage-controlled oscillator's (VCO) frequency is sensed using the effective resistance of a switched capacitor. This effective resistance is transformed to current (I_{SC}) by regulating it to a voltage generated by a series of 2-to-1 voltage downconverters (V_N). I_{SC} is then compared to a current generated by a temperature-compensated switched resistor (I_{SR}) referenced to V_P. The frequency-locked loop is stabilized when I_{SC} is equal to I_R, thereby defining the oscillation frequency (F_{OSC}) as $1/(M\times R_{SW}\times C_{SW})$ where M is the duty cycle of R_{SW} switching operation. Placing the switched resistor and switched capacitor in series effectively "reuses" current, reducing power consumption of this component by 2× compared to a conventional topology where they are placed in parallel.

Figure 5.8.2 shows the detailed circuit implementation. Amp1 and Amp2 regulate voltages on R_{SW} and C_{SW} through M_1 and M_2, respectively. C_{D1} and C_{D2} are connected in parallel with R_{SW} and C_{SW} to reduce the ripple arising from switching events. However, those capacitors can reduce the frequency of the second pole and make the regulation loops unstable. Furthermore, ultra-low-power design using subthreshold-biased devices exacerbates sensitivity to PVT variations, complicating the design. This work proposes a self-biasing scheme that uses a replica of I_{SC} to generate amplifier biasing currents. Assuming near 0dB gain of source follower M_2, the regulation-loop phase margin is defined by $\tan^{-1}(gm_1C_3/gm_{amp1}C_{D1})$ where gm_1, and gm_{amp1} are transconductances of M_1 and Amp1's differential pair, respectively. As the phase margin is determined only by the ratio of transconductance and capacitance, stability can be ensured across a wide range of PVT variation. Furthermore, self-biasing acts to maintain relatively constant power consumption of analog building blocks across temperature and removes the need to include an accurate current reference generator, thereby saving power and area.

Figure 5.8.3 shows transient signal behavior of the reference and control voltages. V_{DIV} is frequency divided from V_{OUT} and provides an accurate on/off ratio for the switched resistor. V_{SR} and V_{SC} are the voltages on R_{SW} and C_{SW} and are regulated by V_N and V_P, respectively, taken from the downconverter. Voltage ripple on V_{SR} and V_{SC} due to switching operation causes current ripple on I_{SR} and I_{SC} (Fig. 5.8.3, right). The difference of I_{SR} and I_{SC} is integrated by C_1 and creates a quadratic ripple on V_C. This ripple can perturb the duty cycle of V_{DIV}, creating temperature and supply-voltage sensitivity. To mitigate these non-ideal effects, a sampler is placed in front of the VCO so that the control voltage is constant within a divider cycle. Amp3 drives sampling-transistor body voltages to remove the drain junction leakage from the sampled voltage, $V_{C,S}$.

A key part of the proposed low-power scheme is the switched resistor. Resistor current ($I_{SR} = (V_{DD}-V_P)/(M\times R_{SW})$) can be reduced by either lowering the voltage across the resistor or increasing R_{SW}. The lower bound on voltage swing is determined by amplifier input offset. V_N is therefore selected to be 1/16th of the supply voltage in order to allow center-frequency adjustment after trimming R_{SW} and C_{SW} under wide variation of amplifier offset and process. The practical upper bound of R_{SW} is dictated by area requirements and set to 17MΩ, with resulting area of 0.065mm^2. The proposed resistor-switching scheme increases the resistor size without increasing area. A switched resistor is usually implemented by placing a switch in series with a resistor [6]. However, current can still flow from the non-disconnected port to parasitic capacitance in the resistor even when the switch is off. This reduces the equivalent resistance and makes it temperature dependent. This effect worsens quadratically with resistor size as the current injected into its parasitic capacitance grows linearly while the current flowing through the resistor reduces inversely with resistance. Instead, we disconnect both resistor terminals so that charges on the parasitic capacitors are only shared while the switch is off. This eliminates injection of additional current from the parasitic capacitor (Fig. 5.8.2, left).

Reference voltages V_N and V_P are generated using a series of switched-capacitor 2-to-1 downconverters clocked by the oscillator output. The stable oscillator frequency results in a constant current consumption across temperature (Fig. 5.8.4), especially compared to conventional diode stack-based voltage dividers as shown in Fig. 5.8.4, right. Even though the voltage mismatch between V_N and V_{DD}-V_P is larger, it is negligible compared to the overall TC of the proposed timer. Furthermore, the mismatch is more linear than that of the diode stack, thus it can be more easily tuned out by trimming TC of R_{SW}. The switching voltages are level-converted through coupling capacitors and a pair of cross-coupled transistors so that the clock feedthrough of each switching transistor is balanced and driving capability is constant regardless of the output voltage [7].

Figure 5.8.2 (bottom right) shows the schematic of the proposed VCO. The delay cell is composed of 1) low-leakage transistors (M_{D1}-M_{D4}) that toggle the output polarity, 2) high-leakage transistors (M_{D5}-M_{D8}) that provide leakage current to slowly charge/discharge the output, and 3) low-leakage tuning transistors (M_{D9}, M_{D10}) that provide delay tunability via the supply voltage. Simulation results shows that the proposed oscillator operates stably down to 630Hz, providing 4.3× lower frequency floor compared to an inverter-based VCO, which is limited in this respect by its small on/off ratio at low V_{DD}.

The proposed design was fabricated in 0.18µm CMOS with an area of 0.5mm^2. It uses only a single supply voltage and does not require additional voltage or current references. Measured results in Fig. 5.8.5 show that the design generates 3kHz while consuming 4.7nW with a temperature coefficient of 13.8ppm/°C measured from –25 to 85°C. Power consumption varies by <50% across this wide temperature range due to the self-biasing technique. Measured line sensitivity is 0.48%/V from 0.85V to 1.4V and Allan deviation is less than 63ppm. Figure 5.8.6 provides a comparison table with other wakeup timers and Figure 5.8.7 shows a die micrograph.

References:

[1] Y. Lee et al., "A modular 1mm^3 die-stacked sensing platform with optical communication and multi-modal energy harvesting," *ISSCC Dig. Tech. Papers*, 2012.

[2] D. Yoon et al., "A 5.58nW 32.768kHz DLL-assisted XO for real-time clocks in wireless sensing applications," *ISSCC Dig. Tech. Papers*, Feb. 2012.

[3] S. Jeong et al., "A 5.8 nW CMOS Wake-Up Timer for Ultra-Low-Power Wireless Applications," *IEEE J. Solid-State Circuits*, Aug. 2015.

[4] A. Paidimarri et al., "A 120nW 18.5kHz RC oscillator with comparator offset cancellation for ±0.25% temperature stability," *ISSCC Dig. Tech. Papers*, Feb. 2013.

[5] M. Choi et al., "A 99nW 70.4kHz resistive frequency locking on-chip oscillator with 27.4ppm/°C temperature stability," *IEEE Symp. VLSI Circuits*, 2015.

[6] M. Perrott et al., "A low-area switched-resistor loop-filter technique for fractional-N synthesizers applied to a MEMS-based programmable oscillator," *ISSCC Dig. Tech. Papers*, Feb. 2010.

[7] S. Bang et al., "A fully integrated successive-approximation switched-capacitor DC-DC converter with 31mV output voltage resolution," *ISSCC Dig. Tech. Papers*, Feb. 2013.

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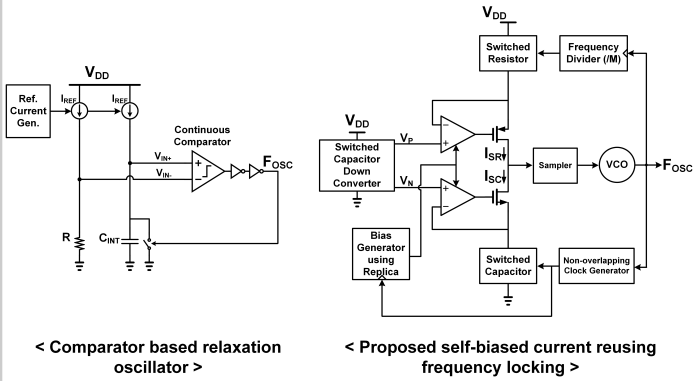


< Comparator based relaxation oscillator >

< Proposed self-biased current reusing frequency locking >

Figure 5.8.1: Block diagram of the conventional relaxation oscillator using a comparator and the proposed self-biased current-reusing frequency-locking scheme without using a current reference.

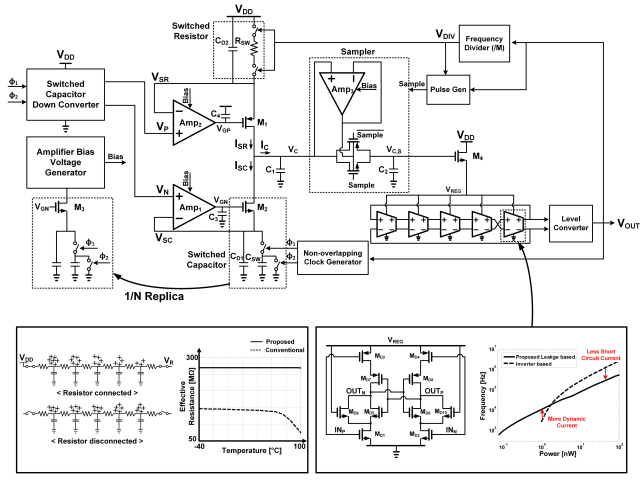


Figure 5.8.2: Circuit diagram of the proposed oscillator (top). At bottom left, the proposed approach of disconnecting both terminals of the resistor during off events enables wider temperature range operation (simulation results). At bottom right, the leakage-based delay cell used in the VCO.

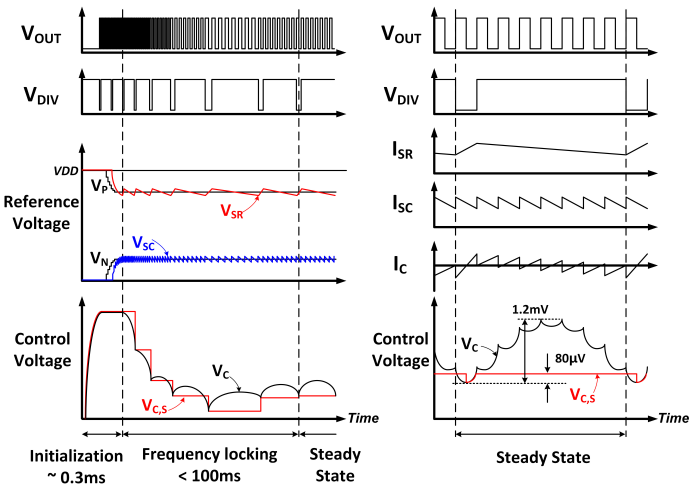


Figure 5.8.3: Transient locking behavior of the output frequency, reference voltages and control voltages of the proposed oscillator (left) and their steady-state behavior (right).

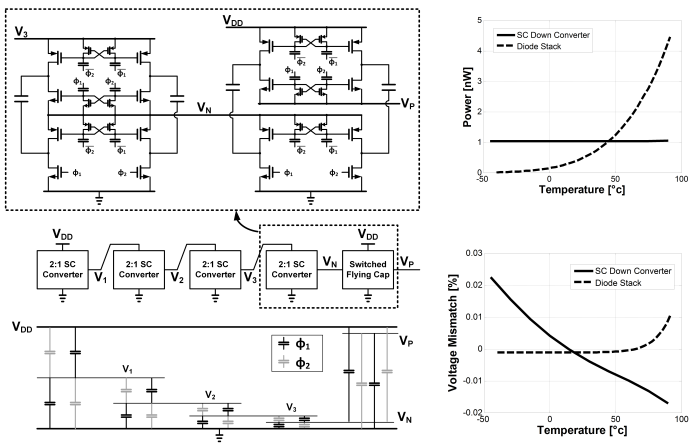


Figure 5.8.4: Reference voltage generation using switched capacitor based DC-DC converter (left) and simulation results of power and accuracy compared to a diode stack (right).

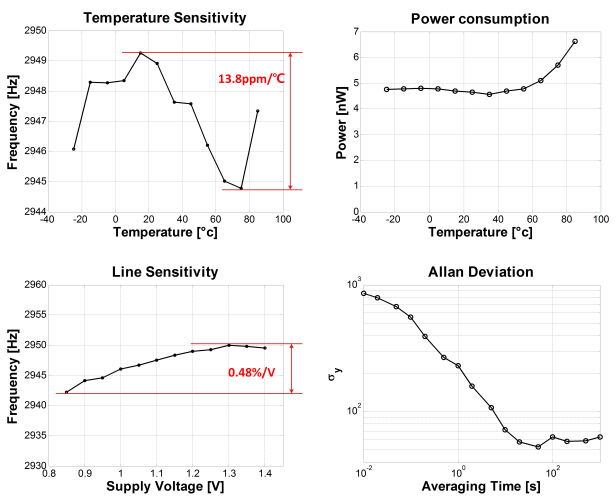
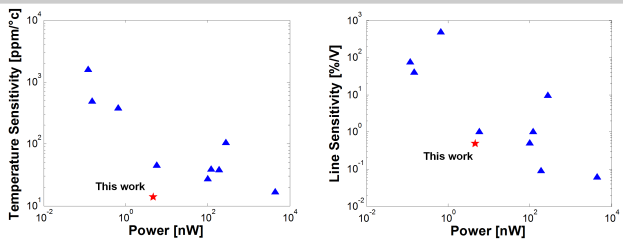


Figure 5.8.5: Measurement results of wakeup timer temperature coefficient (top left), power consumption (top right), line sensitivity (bottom left), and Allan deviation (bottom right).



	This work	JSSC 2015 [3]	ISSCC 2013 [4]	ISSCC 2014	VLSI 2015 [5]	VLSI 2012	VLSI 2012	ISSCC 2011
Process (nm)	**180**	180	65	65	180	60	90	130
Frequency (Hz)	**3000**	11	18,500	33,000	70,400	32,768	100,000	0.37
TC (ppm/°C)[1]	**13.8**	45	38.5	38.2	27.4	16.7	104.6	375(31[2])
Temp. Range (°C)	**-25 to 85**	-10 to 90	-40 to 90	-20 to 90	-40 to 80	-20 to 100	-40 to 90	-20 to 60
Line sensitivity (%/V)	**0.48**	1	1	0.09	0.5	0.006	9.4	490
Power (nW)	**4.7**	5.8	120	190	99.4	4,480	280	0.66[3]
Energy/Cycle (pJ/Cycle)	**1.6**	527.27	6.49	5.76	1.41	136.72	2.80	1,738.8
Area (mm^2)	**0.5**	0.24	0.032	0.015	0.26	0.048	0.12	0.015

[1] Calculated by $(f_{max} - f_{min})/f_{avg} \times 10^6$.
[2] With 10 point calibration using temperature sensor.
[3] Power consumption of temperature sensor is not included.

Figure 5.8.6: Performance summary and comparison to prior work in low-power wakeup timers.

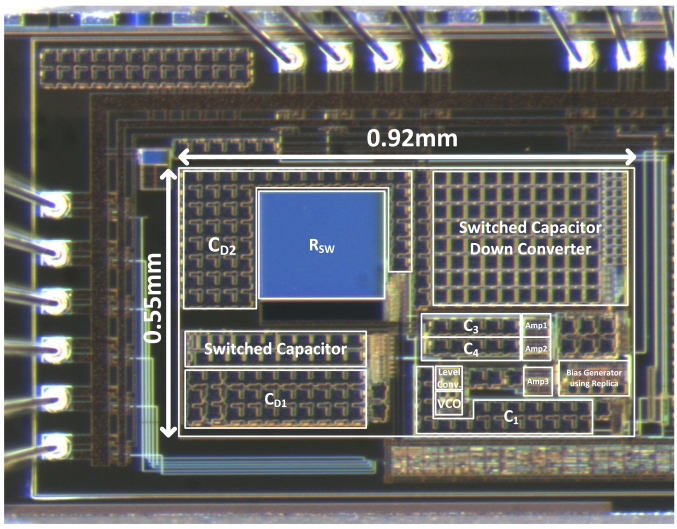


Figure 5.8.7: Chip micrograph of the proposed wakeup timer in 0.18µm CMOS.

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