21.4 A >78%-Efficient Light Harvester over 100-to-100klux with Reconfigurable PV-Cell Network and MPPT Circuit

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Energy harvesting is an attractive solution to extend system lifetime for internet of everything (IoE) nodes. Ambient light is a common energy source that can be harvested by photovoltaic (PV) cells. However, light intensity varies widely depending on location, ranging from ~10s of lux in dim indoor conditions to ~100klux under direct sunlight. Designing a fully integrated light harvester that spans such a wide range of light intensity with high efficiency is challenging, especially since typically low PV cell voltage requires a high upconversion ratio and PV-cell voltage/current characteristics change significantly with light intensity. Boost DC-DC converters are a typical energy-harvesting solution with high conversion efficiency, but they require a large off-chip inductor and hence cannot be fully integrated, increasing system size [1-3]. Recently, switched-capacitor (SC) DC-DC converters have been actively researched to enable fully-integrated energy harvesting using on-chip capacitors [4-6]. However, their efficiency has typically been limited to the 40-to-55% range at low input power levels (≤1μW) due to conduction/switching losses.

This paper presents a fully integrated light harvester that maintains >78% efficiency from 100lux to 100klux when charging a 1.5-to-2.5V battery with a 7.8mm^2 PV-cell network. Compared to a conventional SC DC-DC converter, the key approach lies in moving the voltage upconversion from SC circuits to the PV cells. This approach *directly* transfers energy from the PV cells to a battery using only DC switches and thus there is no energy conversion loss from switching capacitors or inductors. Also, the PV-cell network configuration is dynamically updated to adjust to varying light intensity and battery voltage conditions using a compact maximum-power-point tracking (MPPT) circuit.

Figure 21.4.1 compares a conventional SC DC-DC converter and the proposed light harvester. The SC DC-DC converter typically transfers charge from the low PV-cell voltage (typically 250 to 400mV) to the high battery voltage (typically 1.5 to 4V) by charging/discharging flying capacitors, which results in both conduction and switching losses. The proposed light harvester avoids this efficiency loss by entirely removing capacitance switching and instead directly connects the PV-cell network through DC switches to the battery. In order to match the MPPT voltage of the PV cells with the battery voltage, both of which can vary, the PV cells are periodically reconfigured into different series/parallel configurations by the MPPT circuit. As shown abstractly in Fig. 21.4.1, a strong light condition with a high optimal PV voltage results in the 12 PV cells being configured with 3 in series and 4 in parallel, while under a low-light condition, the same 12 cells are configured with 6 in series, 2 in parallel.

Figure 21.4.2 shows the implemented PV-cell network, which consists of 36 unit cells of 0.16mm^2. The 36 unit cells are grouped into one cell with 3×5 size, one cell with 1×5 size, one cell with 1×4 size, and twelve cells with unit size for a total of 15 separate cells. The switch matrix of the harvester chip enables five configurations that allow MPPT across battery and light conditions. Figure 21.4.2 (bottom, left) shows how switching between configurations enables >82% efficiency across light and battery voltage, despite efficiency drops at the cross-over points (simulation). By selecting a minimum unit PV-cell size of 1/36 of the total area, the lost area for configurations where there is an orphan cell (configurations 5×7 and 7×5, Fig. 21.4.2) is limited to 2.8%. An implementation with all unit-size PV cells that are connected to the harvesting chip individually requires 72 wires. However, we reduce this number to 30 through sub-grouping of PV cells. This also helps reduce area loss (from 14.1% to 5.0%) arising from additional wirebonding pads and trench isolation (10μm) between PV-cell groups that are potentially connected in series. Taken together, the total area penalty associated with using a reconfigurable PV-cell network rather than a single monolithic PV cell is 5.0% for the 3×12, 4×9, and 6×6 configurations and 7.7% for the 5×7 and 7×5 configurations. However, this area loss is easily overcome by the much greater harvesting efficiency of the approach.

Figure 21.4.3 shows the circuit diagram of the harvester chip. At <1.5V battery voltage, the power-on-reset generator holds reset, and the MPPT controller forces the PV-cell network to '4×9' mode. The harvester charges the battery to >1.5V for lighting conditions >100lux. Once the battery is charged to 1.5V, the low-power power-on-reset generator, which is based on a leakage-based voltage reference and modified Schmitt trigger, turns on the leakage-based oscillator that clocks the MPPT controller. The MPPT performs a hill-climbing algorithm by comparing the harvested current from two adjacent configurations. To measure harvested current, one unit-size PV cell is temporarily disconnected from the PV-cell network and used as a test cell. During this time, the PV-cell network loses one unit cell but continues to harvest. The test cell voltage $V_{MONITOR}$ is connected to a programmable pull-down current generator. The pull-down current is modulated by the MPPT controller by changing the voltage selected from the gate-voltage generator and by changing the number of enabled pull-down transistors in a unit and the number of pull-down units (Fig. 21.4.3).

To compare harvested power, the harvester compares the battery *current* assuming the battery voltage is constant during the comparison time (<2sec.). First, it finds the current sourced by a single PV cell in the first configuration and then forces a corresponding current in the second configuration onto the PV cell to determine if the PV voltage is higher or lower. To explain, we consider a comparison between configurations '4×9' and '5×7' (Fig. 21.4.4). First, the MPPT controller searches for the pull-down current configuration where $V_{MONITOR} = V_{BAT}/4$, since this replicates the voltage that would be seen by each PV cell in the 4×9 configuration (4 PV cells in series). For reasons that will become clear, it does so by fixing the number of enabled transistors in each pull-down unit to 7 and searching for the correct number of units and gate voltage (for simplicity of explanation, we assume the number of units is 1). Since the 4×9 configuration has 9 columns, the total battery current if the configuration was connected to the battery would be $I_{BAT\_4\times9} = 9\times7\times I_U$, where I_U is the current of a single transistor in the current generator. The MPPT controller now fixes the number of units and gate voltage but changes the number of enabled transistors in a unit to 9. It also changes $V_{DIV} = V_{BAT}/5$, to match the 5 PV cells in series in the 5×7 configuration. The current now forced on the PV cell is $9\times I_U = (1/7)\times I_{BAT\_4\times9}$. Since the 5×7 configuration has 7 columns, this corresponds to the condition where $I_{BAT\_5\times7} = I_{BAT\_4\times9}$. Hence, if the two configurations source equal battery-charging current, the forced current on the PV cell will result in $V_{MONITOR} = V_{DIV}$. Thus, if the comparator determines that $V_{MONITOR} > V_{DIV}$, it means $I_{BAT\_5\times7} > I_{BAT\_4\times9}$ and vice-versa. The advantage of this MPPT approach is that it is implemented by simple digital logic and involves only one search for the pull-down current configuration, followed by one final comparison to determine the superior configuration. Due to the low-power circuits used throughout the MPPT module and its compact design, the harvester chip only consumes 2nW (measured) at 2V battery voltage and 22Hz clock.

The proposed harvester is fabricated in 0.18μm CMOS and tested with individual diced PV cells as a prototype. The PV cells can also be fabricated as a single die with size of 2.6×3mm^2. To align the pad locations in order to shorten wire length, the harvester chip has an area of 2.75×3mm^2. Figure 21.4.5 shows typical end-to-end harvesting efficiency compared to the maximum power point of all PV cells connected in parallel, including circuit power overhead for continuous MPPT operation and 5.0% area loss from pads and trench isolation. The harvester enables charging of a 1.5V battery from as little as 7lux and maintains harvesting efficiency of >78% from 100lux to 100k lux and across a 1.5-to-2.5V battery voltage. Figure 21.4.6 shows a comparison table and Fig. 21.4.7 shows test-chip die photos and accompanying PV cells.

References:

[1] S. Bandyopadhyay et al., "A 1.1nW Energy Harvesting System with 544pW Quiescent Power for Next-Generation Implants," *ISSCC Dig. Tech. Papers*, pp. 396-397, Feb. 2014.

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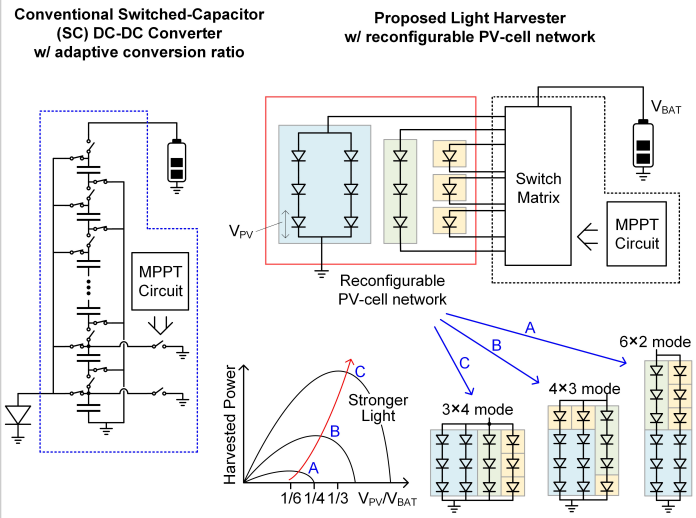

Figure 21.4.1: Conventional SC DC-DC converter (left) and the concept of the proposed light harvester (right).

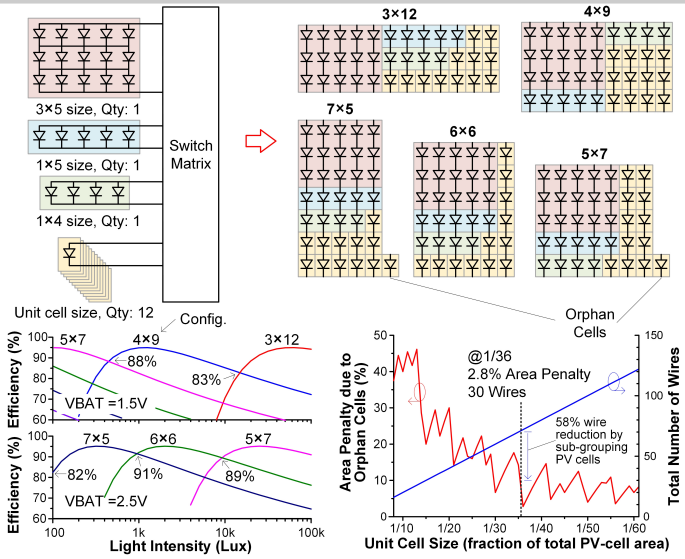

Figure 21.4.2: Proposed reconfigurable PV-cell network.

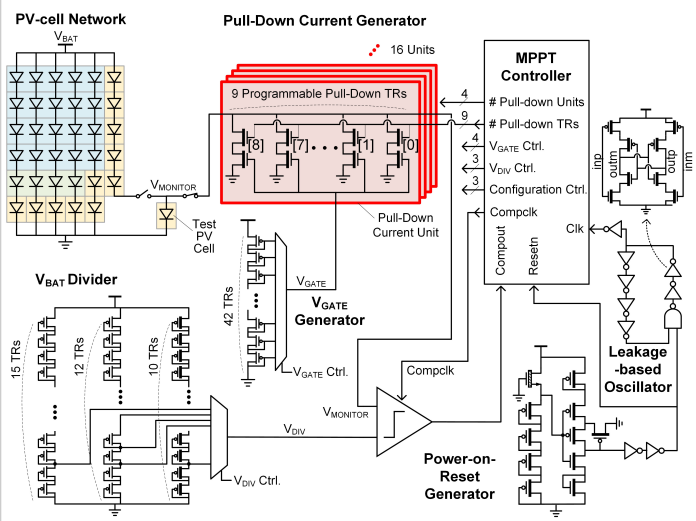

Figure 21.4.3: Circuit diagram for the proposed harvester.

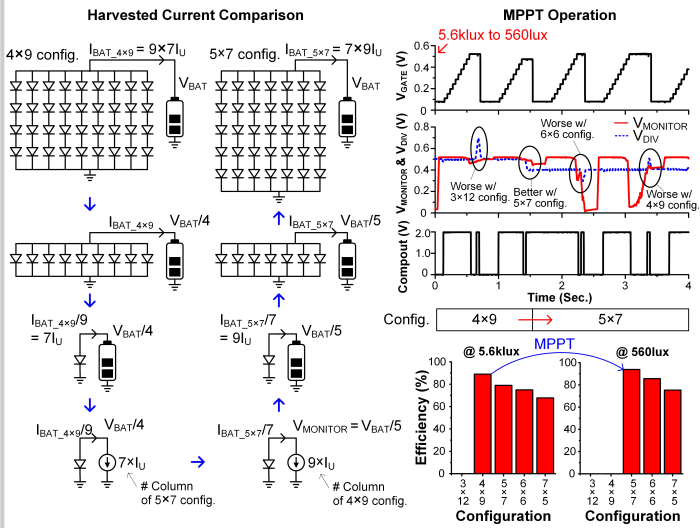

Figure 21.4.4: Example of MPPT operation between 4×9 and 5×7 configurations.

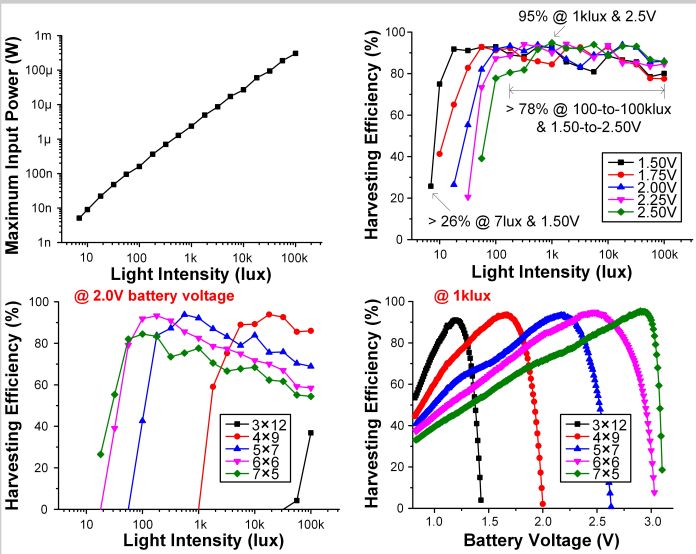

Figure 21.4.5: Measured light harvester.

	ISSCC 2014 [1]	ISSCC 2015 [2]	ISSCC 2015 [3]	ISSCC 2014 [4]	JSSC 2015 [5]	ISSCC 2015 [6]	This Work
Process	0.18μm CMOS	0.18μm CMOS	0.5μ CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Harvester Type	Boost + SC	Buck	Buck/Boost	SC	SC	SC	PV-Cell Network
Fully-Integrated	No	No	No	Yes	Yes	Yes	Yes
Output Power (W)	0.5n ~ 4n	35n ~10m	1μ ~ 15m	5n ~ 5μ	4μ ~ 21μ	1μ ~ 50μ	0.3μ ~ 0.3m
Demonstrated Light Intensity (lux) / PV cell size (mm^2)	N/A	N/A	400 / N/A	400(**) ~ 200k(***) / 0.84	150 ~ 600 / 250	N/A	**100 ~ 100k / 7.8**
Output Voltage (V)	1.5 ~ 1.9	0.45 ~ 0.5	1.0 ~ 3.3	2.2 ~ 5.2	3.3	3.3	1.5 ~ 2.5
Harvesting Efficiency (%)	47(**) ~ 56	47(**) ~ 92	76(**) ~ 93	40 ~ 50	37(**) ~ 86	55(**) ~ 81(***)	**78 ~ 95**†
MPPT	No	No	Yes	No	Yes	Yes	Yes
MPPT Power (W)	N/A	N/A	4μ	N/A	294n	2.9μ(****)	2n
Area (mm^2)	5.76 (1.50(*))	1.44	0.79 (0.50(*))	0.86	2.25	4.00	8.25 (0.19(*))

(*) Core area, (**) Estimated from the paper, (***) w/ controller, (****) Calculated from harvesting efficiency w/ and w/o controller
† 0.3μ~0.3mW corresponds to 100~100klux. Minimum harvesting condition: 1.4nW output power @ 7lux and 26%

Figure 21.4.6: Performance summary and comparison to previous work.

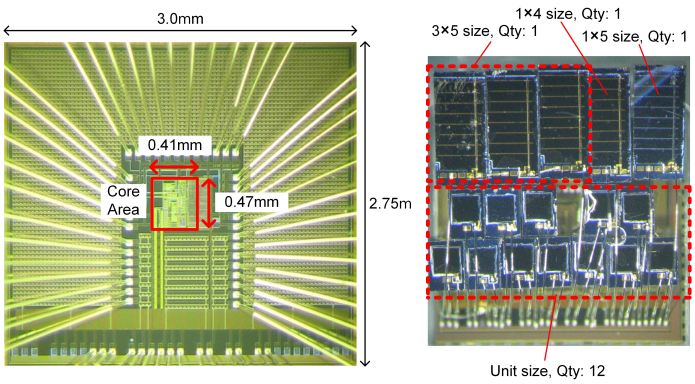

Figure 21.4.7: Die micrograph. Harvester chip (left). Stacked system with Individual diced PV cells (3mm×3mm) (right).

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